Contents

Chapter 3 Limits on Instruction-Level Parallelism

Chapter 4 Multiprocessors and Thread-Level Parallelism

Chapter 5 Memory Hierarchy Design

Chapter 6   **Storage Systems**

Appendix A   **Pipelining: Basic and Intermediate Concepts**

Appendix B   **Instruction Set Principles and Examples**

Appendix C   **Review of Memory Hierarchy**

Companion CD Appendices

Appendix D   **Embedded Systems**
Updated by Thomas M. Conte

Appendix E   **Interconnection Networks**
Revised by Timothy M. Pinkston and José Duato

Appendix F   **Vector Processors**
Revised by Krste Asanovic

Appendix G   **Hardware and Software for VLIW and EPIC**

Appendix H   **Large-Scale Multiprocessors and Scientific Applications**

Appendix I   **Computer Arithmetic**
by David Goldberg

Appendix J   **Survey of Instruction Set Architectures**

Appendix K   **Historical Perspectives and References**

Online Appendix (*textbooks.elsevier.com/0123704901*)

Appendix L   **Solutions to Case Study Exercises**