Weekly Report

Names and Roll no: Ch. Sai Nived (AP18110020174) A. Rohit Kumar (AP18110020168) P. Jithendra (AP18110020164) A. Kaushik Sai (AP18110020156)
Guide: Siva Sankar Yellampalli
Place of Execution: HDL(Verilog), Xilinx., EDA playground.
Project Title: Implementation of the communication protocols SPI using a FPGA by the HDL-Verilog language.
Week Starting Date: March 8 2021
Week Ending Date: March 13 2021

1. **Literature Studied During the Week:**
   Papers studies:
   - An introduction to I2C and SPI protocols
2. **Details of Work Carried out:**

The internal architecture of SPI mainly consists of two modules, master module and slave module as shown in figure 1. The SPI module allows a full duplex, synchronous, serial communication between the micro controller unit (MCU) and peripheral devices. It is enabled by setting the SPI enable (SPE) bit in SPI Control Register. The SPI communicates using two data lines, a control line, and a synchronization clock.

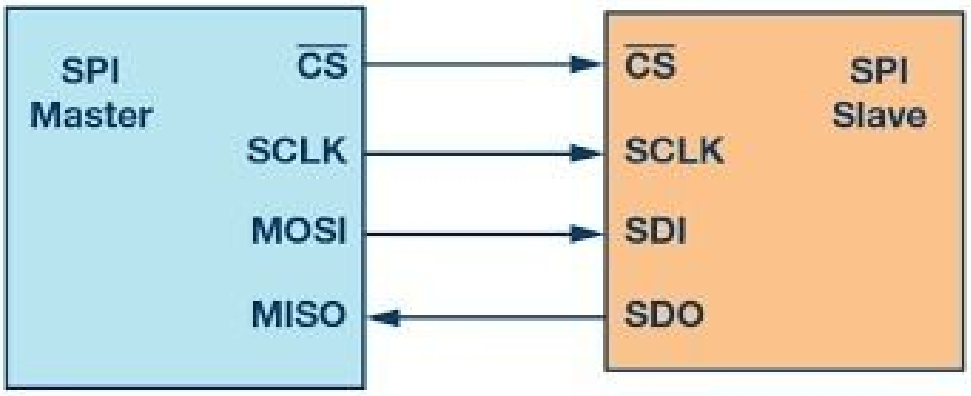

figure 1

- Master out Slave in (MOSI) - Output data from the master to the inputs of the slaves.
- Master in Slave out (MISO) - Output data from a slave to the input of the master.
- Serial Clock (SCLK) - Clock driven by the master to slaves, used to synchronize the data bits.
- Slave Select (SS) - Select signal driven by the master to individual slaves, used to select the target slave.

Master Mode Operation: The SPI operates in master mode when the MSTR control bit is set. The transmission begins by writing to the master

SPI Transmit Data Register. If the shift register is empty, the byte immediately transfers to the shift register. Once the byte is transferred from the SPI transmit register to the shift register, the SPTE control bit is set indicating that another byte can be written to the SPI transmit data register. In master mode, before transmission SS pin is connected to VDD if the single slave module is used. Then the byte begins shifting out a bit at a time on the MOSI pin synchronized with the master serial clock. The data transmission will continue for 8 clock cycles, transferring all 8-bits. The transmission ends when the whole byte is shifted out of the master SPI shift register into the slave SPI shift register. The slave shift register is then automatically transferred to the slave SPI receive data register if it is empty. The SPRF control bit is set indicating that the SPI receive register is full and waiting to be read.

Slave Mode Operation: The SPI operates in slave mode when the MSTR control bit is clear. In slave mode, the function of serial data output pin MISO and serial data input pin MOSI. The serial clock is input to the slave from master. And the SS pin is the slave select input. Before a data transmission the SS pin is connected to ground if the single slave module is used. Once the byte is transferred from the SPI transmit register to the shift register, the SPTE control bit is set indicating that another byte can be written to the SPI transmit data register. The byte of data shifting a bit at time on the MISO pin synchronized with the master serial clock. The master shift register is then automatically transferred to the master SPI receive data register if it is empty.

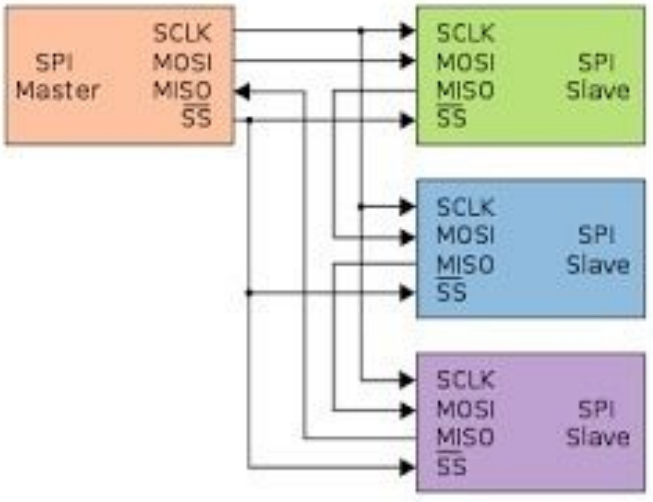

figure 2

Data Transmission

To begin SPI communication, the master must send the clock signal and select the slave by enabling the CS signal. Usually, chip select is an active low signal; hence, the master must send a logic 0 on this signal to select the slave. SPI is a full-duplex interface; both master and slave can send data at the same time via the MOSI and MISO lines respectively. During SPI communication, the data is simultaneously transmitted (shifted out serially onto the MOSI/SDO bus) and received. The serial clock edge synchronizes the shifting and sampling of the data. The SPI interface provides the user with flexibility to select the rising or falling edge of the clock to sample and/or shift the data. Please refer to the device data sheet to determine the number of data bits transmitted using the SPI interface.

Clock Polarity and Clock Phase

In SPI, the master can select the clock polarity and clock phase. The CPOL bit sets the polarity of the clock signal during the idle state. The idle state is defined as the period when CS is high and transitioning to low at the start of the transmission and when CS is low and transitioning to high at the end of the transmission. The CPHA bit selects the clock phase. Depending on the CPHA bit, the rising or falling clock edge is used to sample and/or shift the data. The master must select the clock polarity and clock phase, as per the requirement of the slave. Depending on the CPOL and CPHA bit selection, four SPI modes are available. Table 1 shows the four SPI modes.

SPI Mode	CPOL	CPHA	Clock Polarity in Idle State	Clock Phase Used to Sample and/or Shift the Data
0	0	0	Logic low	Data sampled on rising edge and shifted out on the falling edge
1	0	1	Logic low	Data sampled on the falling edge and shifted out on the rising edge
2	1	1	Logic high	Data sampled on the falling edge and shifted out on the rising edge
3	1	0	Logic high	Data sampled on the rising edge and shifted out on the falling edge

Table 1

Problems faced during Execution:

- How data transmission works
- Clock Phases
- Clock Polarities

Work Carried out to be Next week:

- What is state diagram?
- What is timing diagram?
- Benchmarks used to measure SPI?