PrimeLib by Synopsys

Note:

1: The Liberty file (.lib) generated here will be used in your final project (project 6)

2: You should use PrimeLib to characterize the cells one by one, then combine all the output .lib files.

PrimeLib is a software tool that generates a library in Liberty (.lib) format from a set of SPICE models, cell functional descriptions and associated netlists. The generated library can be used for timing, power and noise analysis with compatible tools such as Library Compiler, IC Compiler, Design Compiler and PrimeTime.

Before you begin, you should have finished the DRC/LVS/PEX/HSPICE simulation of the cells in your library. You need to verify the HSPICE results, if they are incorrect, this tool will fail.

Library Characterization for INV

Go to your gf65 working directory first:

```
cd ~/cad/gf65
```

Create a working directory for PrimeLib:

```
mkdir primelib_gf65
```

Go to your PrimeLib working directory first:

```
cd primelib_gf65
```

Source the synopsys profile for running PrimeLib:

```
. /proj/cad/startup/profile.synopsys_2018
```

Note: Make sure that you change all "vdd!" into "VDD" and all "gnd!" into "VSS".

Start the PrimeLib tool:

```
primelib
```

```
{txace3:~/cad/gf65/primelib_gf65} primelib
Reading  /proj/cad/synopsys/synopsys_2021/primelib/T-2022.03-SP1/etc/sis.err...done

                                PrimeLib (R)

          Version T-2022.03-SP1 for linux64 - Apr 12, 2022 13:01:04

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PID : 23497
User: vks160030
Dir : /home/eng/v/vks160030/cad/gf65/primelib_gf65
Host: txace3.utdallas.edu

UT Dallas, Department of Engineering

Malibu mode 2 activated
Thu Oct  6 13:07:55 2022: Establishing connection to license server
[SCL] INFO: Spanning checkout functionality enabled.
Thu Oct  6 13:07:56 2022: Testing server connection using feature PrimeLib_CHAR
Thu Oct  6 13:07:56 2022: License server connection established
Thu Oct  6 13:07:57 2022: Checked out license FEATURE PrimeLib_CHAR v2022.03 on PORT 1700@engdmv.utdallas.edu
Command-line: /proj/cad/synopsys/synopsys_2021/primelib/T-2022.03-SP1/linux64/bin/primelib
pl_cci>
```

To create a .lib file for INV, follow the steps given in this document. These steps should be repeated to create .lib file for other cells (NAND2, NOR2, XOR2, …)

Type the below command to create a working directory for INV:

```
create -legacy INV
```

Open **another** terminal/ konsole to check if you have below shown folders in your INV directory:

```
cd ~/cad/gf65/primelib_gf65/INV

ls
```

```
{txace3:~} cd ~/cad/gf65/primelib_gf65/INV
{txace3:~/cad/gf65/primelib_gf65/INV} ls
config  control  etc  models  netlists  reports  results  runtime
{txace3:~/cad/gf65/primelib_gf65/INV}
```

```
cd config

ls
```

1. You need replace the existing *configure.tcl* file with a new file given in eLearning. (you can use gedit to replace the file)
   The *configure.tcl* is GF 65nm configuration file. This file is technology specific file, it has details such as VDD, VSS (gnd) values, etc.

   Repeat this step for all the cells in your library.

```
cd ../control
ls
```

2. This folder is empty, you need to copy *INV.inst* file from eLearning.
   The *.inst* file consists of input, output, inout port details, and functionality details. Make sure you change these parameters when you working on other cells.

   Changes to be made:

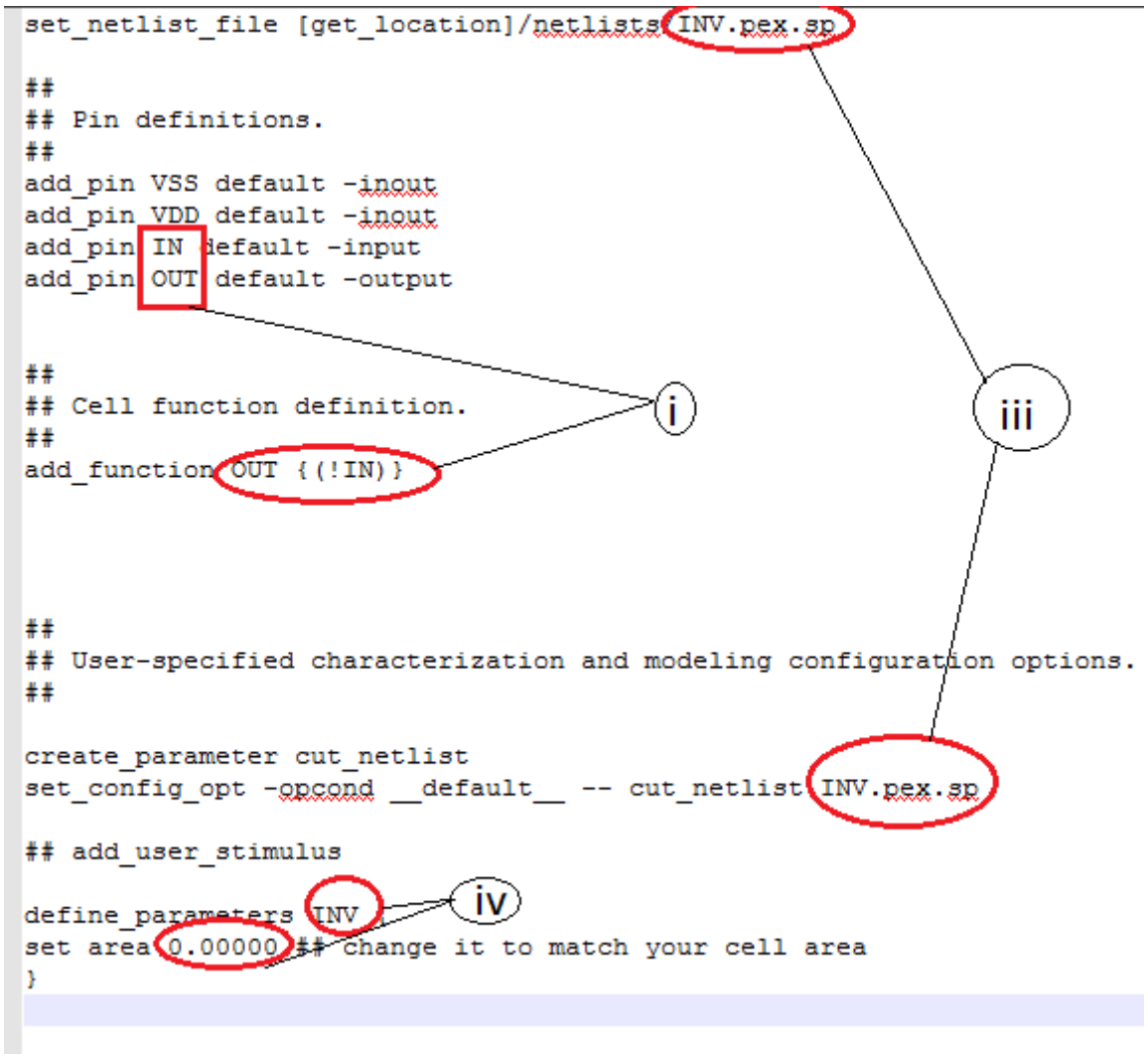
   i. Functionality of the cell, input port names, and output port name. In the example shown below in the image is that of an INV, the input port name is IN, and output port name is OUT.

      Different cell functions are shown below, OUT is output port name. A, B, C, D, and S are input port names. If you have different names, then make necessary changes to match your input and output port names.

      - `NAND2: OUT {(!(A&B))}`
      - `NOR2: OUT {(!(A+B))}`
      - `XOR2: OUT {(((!A)&B)+((!B)&A))}`
      - `MUX2:1: OUT {(((!S)&A)+(S&B))}`
      - `AOI21: OUT {(!((A&B)+(C)))}`
      - `OAI22: OUT {(!((A+B)&(C+D)))}`
      - `AOAI211: OUT {(!(((A&B)+C)&(D)))}`

      The *.inst* file for INV is given, but you need to create your own *.inst* files for other cells.

   ii. Rename the .inst filename to match the name of the folder (INV, NAND2, NOR2,…)
   iii. In *.inst* file change the name of the file in the paths.
   iv. At the bottom while defining the parameters (area) make sure you add in the name same as cell name. Add in your area of the cell (vertical distance: top of VDD to bottom of GND, horizontal distance: JX/ JZ/ prboundary to JX/ JZ/ proboundary).

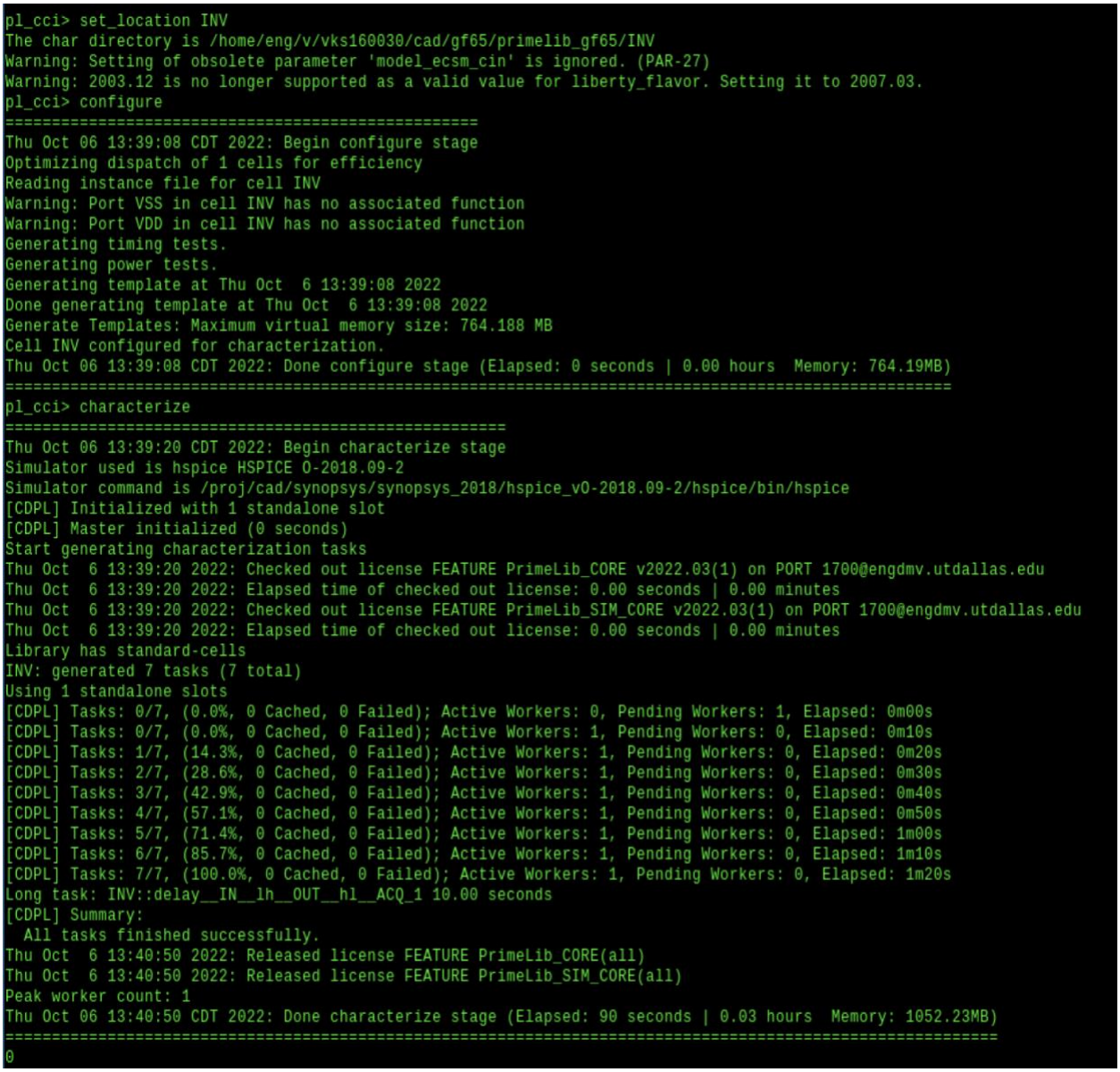



```
cd ../netlist
ls
```

3. This folder is empty too, you need to copy your 3 parasitic extracted files INV.pex.sp, INV.pex.sp.pex, INV.pex.sp.INV.pxi (remember to replace vdd! To VDD, and gnd! to VSS before copying the files)

Go back to the PrimeLib terminal now, and type the following commands:

```
set_location INV
configure
characterize
```



```
pl_cci> set_location INV
The char directory is /home/eng/v/vks160030/cad/gf65/primelib_gf65/INV
Warning: Setting of obsolete parameter 'model_ecsm_cin' is ignored. (PAR-27)
Warning: 2003.12 is no longer supported as a valid value for liberty_flavor. Setting it to 2007.03.
pl_cci> configure
================================================
Thu Oct 06 13:39:08 CDT 2022: Begin configure stage
Optimizing dispatch of 1 cells for efficiency
Reading instance file for cell INV
Warning: Port VSS in cell INV has no associated function
Warning: Port VDD in cell INV has no associated function
Generating timing tests.
Generating power tests.
Generating template at Thu Oct  6 13:39:08 2022
Done generating template at Thu Oct  6 13:39:08 2022
Generate Templates: Maximum virtual memory size: 764.188 MB
Cell INV configured for characterization.
Thu Oct 06 13:39:08 CDT 2022: Done configure stage (Elapsed: 0 seconds | 0.00 hours  Memory: 764.19MB)
================================================================================================
pl_cci> characterize
================================================
Thu Oct 06 13:39:20 CDT 2022: Begin characterize stage
Simulator used is hspice HSPICE O-2018.09-2
Simulator command is /proj/cad/synopsys/synopsys_2018/hspice_vO-2018.09-2/hspice/bin/hspice
[CDPL] Initialized with 1 standalone slot
[CDPL] Master initialized (0 seconds)
Start generating characterization tasks
Thu Oct  6 13:39:20 2022: Checked out license FEATURE PrimeLib_CORE v2022.03(1) on PORT 1700@engdmv.utdallas.edu
Thu Oct  6 13:39:20 2022: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Thu Oct  6 13:39:20 2022: Checked out license FEATURE PrimeLib_SIM_CORE v2022.03(1) on PORT 1700@engdmv.utdallas.edu
Thu Oct  6 13:39:20 2022: Elapsed time of checked out license: 0.00 seconds | 0.00 minutes
Library has standard-cells
INV: generated 7 tasks (7 total)
Using 1 standalone slots
[CDPL] Tasks: 0/7, (0.0%, 0 Cached, 0 Failed); Active Workers: 0, Pending Workers: 1, Elapsed: 0m00s
[CDPL] Tasks: 0/7, (0.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m10s
[CDPL] Tasks: 1/7, (14.3%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m20s
[CDPL] Tasks: 2/7, (28.6%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m30s
[CDPL] Tasks: 3/7, (42.9%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m40s
[CDPL] Tasks: 4/7, (57.1%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 0m50s
[CDPL] Tasks: 5/7, (71.4%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 1m00s
[CDPL] Tasks: 6/7, (85.7%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 1m10s
[CDPL] Tasks: 7/7, (100.0%, 0 Cached, 0 Failed); Active Workers: 1, Pending Workers: 0, Elapsed: 1m20s
Long task: INV::delay__IN__lh__OUT__hl__ACQ_1 10.00 seconds
[CDPL] Summary:
  All tasks finished successfully.
Thu Oct  6 13:40:50 2022: Released license FEATURE PrimeLib_CORE(all)
Thu Oct  6 13:40:50 2022: Released license FEATURE PrimeLib_SIM_CORE(all)
Peak worker count: 1
Thu Oct 06 13:40:50 CDT 2022: Done characterize stage (Elapsed: 90 seconds | 0.03 hours  Memory: 1052.23MB)
================================================================================================
0
```

```
model
```

```
pl_cci> model
================================================
Thu Oct 06 13:48:15 CDT 2022: Begin model stage
Creating new libraries.
Warning: ground supply has not been properly defined
info: order {ntin nvolt} ntin {1.0 2.0 3.0 4.0 5.0}
info: order {ntin nvolt} ntin {1.0 2.0 3.0 4.0 5.0} nvolt {1.0 2.0}
================================================
Thu Oct 06 13:48:15 CDT 2022: Begin write library
Creating Liberty file "/home/eng/v/vks160030/cad/gf65/primelib_gf65/INV/models/liberty/cells/INV_op_cond.lib".
Thu Oct 06 13:48:15 CDT 2022: Done write library (Elapsed: 0 seconds | 0.00 hours  Memory: 1052.23MB)
================================================================================================
Merging cell level models...
================================================
Thu Oct 06 13:48:15 CDT 2022: Begin merge stage
Merging 1 cell models in /home/eng/v/vks160030/cad/gf65/primelib_gf65/INV/models/liberty/cells
Merged Liberty model created /home/eng/v/vks160030/cad/gf65/primelib_gf65/INV/models/liberty/liberty_op_cond.lib.
Thu Oct 06 13:48:16 CDT 2022: Done merge stage (Elapsed: 1 seconds | 0.00 hours  Memory: 1052.23MB)
================================================================================================
Thu Oct 06 13:48:16 CDT 2022: Done model stage (Elapsed: 1 seconds | 0.00 hours  Memory: 1052.23MB)
================================================================================================
```

The characterization of INV is done!!

If you get any error it means that you haven't followed the steps correctly.

The characterized file is stored at:

```
cd ~/cad/gf65/primelib_gf65/INV/models/liberty
```

with an extension of .lib

Generate .lib files for all the cells and combine all the output .lib files into a single .lib file. While combining, make sure your .lib file has only one set of all look up tables (LUTs) followed by cell information.

After combining all the .lib files, replace the word "op_cond" with "library"

Proceed to Library Compiler step next where you convert the .lib (library characterized) file to .db (database) file.