# Design of An Open Source Power Analysis Tool

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***Abstract*—The electronic devices are achieving tremendous growth since few decades due to advancement of large-scale integration. As the technology increases, VLSI focuses on the shrinkage of size with lower power and better performance. There are many constraints that challenges the design and the prime one is power. The total power consumption is the most important parameter which has impact on every stage of the design flow. The accurate power analysis tool is required which can be used at any stage in the design flow. This paper aims to design an open source power analysis tool which can perform total power analysis due to leakage and average switching activity**

***Index Terms*—power analysis, leakage power, average switching power, total power consumption**

## I. INTRODUCTION

Simulation software operating at different levels of the design process is the key factor for any VLSI system design. Power is an energy that is dissipated in any device in a unit time. In VLSI chip, electrical energy is converted to heat energy while performing operations. The rate at which the energy converts to heat is the power dissipation. Analysis focuses mainly about the reliable estimation of power or energy dissipation at different phases of the design process. Analysis serves as the foundation for design optimization[1]. Power analysis in CMOS gate is based mainly on the current consumption. The speed requirements of the device also results in the production of large power density. The power dissipation of CMOS circuit is mainly dominated by the dynamic dissipation that occurs due to charging and discharging capacitances.

## II. TYPES OF POWER DISSIPATION

The total power is made of two major power dissipations such as static power dissipation and dynamic power dissipation.

Ptotal=Pstatic+Pdynamic

Also, power analysis can also be differentiated viz. Simulation power analysis and probabilistic power analysis. The simulation power analysis focuses on power estimation at each stages abstraction levels and it is based on the predictable power model. The probabilistic power analysis has better computation efficiency and it is mainly developed for gate level abstraction.

### *A. Static power dissipation*

The static power dissipation occurs in the form of leakage current when the system is not on or is in standby mode. In circuits, there are several sources of leakage current including subthreshold leakage, diode leakages around transistors and on. It is also considered to be as leakage power. The leakage power of a CMOS circuit does not depend on input transitions or externa load capacitance and thus it remains constant for a logic cell.

### *B. Dynamic power dissipation*

The dynamic power dissipation inside the logic cell is called the internal power, which consists of short circuit power and charging or discharging of internal nodes. The dynamic energy dissipation events not only depend on the Boolean function of the gate, but also the implementation of the gate. It is caused by switching activities of the circuits. The capacitances are not only the external capacitors but also the internal capacitances due to parasitic effects.

## III. POWER ANALYSIS

The power analysis in any ASIC flow can be done in different stages such as the average power analysis can be done before synthesizing any module or after writing RTL, after synthesizing, to the gate level netlist produced and after placement. Similarly, the peak power analysis can be done after placement, after clock tree synthesis and post layout.

## IV. NEED FOR POWER ANALYSIS

The main need for power analysis tool is to estimate the power dissipated at each stages of design process in order to analyse the stage which consumes more power. The power is estimated at every stage so that if the power consumption is very high at particular stage, we can reduce it by applying any power reduction techniques. Such power analysis can be used in any VLSI circuits. It has vast impact in analog circuit designs too.

## V. FLOW OF POWER ANALYSIS

Any power analysis will follow certain methodology or flow of work. The following illustrates about the flow of power analysis which is more efficient.

Verilog→VCD→SAIF→Toggle rate→Switching activity →Average power.

Similarly, for peak power analysis we can estimate by running the waveforms. Also, peak power analysis is efficient only in gate level whereas average power analysis can be done even for user defined values and default values.

## VI. Applications Of Power analysis

The power analysis has widespread applications everywhere in VLSI domain as all VLSI circuits is focused on obtaining very low power. Lower the power better the performance. Lower power is very much needed when we approach for architectural or macro level design. For example, if we consider 8-Bit RISC architecture we can write code in any HDL language and can obtain synthesized report after simulation.

Power dissipated as heat will reduce the speed of the system. If we obtain the total power as high, we can optimize it by making some changes in tcl file as the tcl commands helps to calculate power as well as to optimize it. Our prime aim in this paper is to create a tool in TCL in order to state the accurate power and also ways to optimize it.Power analysis find its applications in the following domains.

- Early power estimation will help in meeting the design specifications.
- Power analysis helps in deciding power distribution network.
- Also helps in deciding the size of power supply.
- Helps in characterizing the chip based on Quiescent current.

## VII. Power analysis in VLSI Interconnect

As technology scales, signals may reach less chip area within one clock cycle, leading to multi-cycle paths. One solution is to pipeline such signals, on account of pipeline throughput. However, pipeline structures can consume energy. the matter is finding the optimal tradeoff between energy and throughput in determining pipeline architecture.

to know this property, consider a pipelined signal with minimum latency. Here, each register-to-register path within the pipeline necessarily has zero timing slack. a rise in pipeline clock frequency would yield a like increase in throughput, but it's impossible to extend pipeline clock frequency here because each pipeline stage may be a critical timing path. With repeated RC wire, the throughput of a sign is that the inverse of its latency, and a discount in critical path latency enhances throughput because the system clock are often run faster.

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## VIII. Power analysis of digital CMOS technologies

The expanded design space required for low power has further increased the complexity of an already non-trivial task. Low power design basically involves two concomitant tasks: power estimation and analysis and power minimization. These tasks need to be carried out at each of the levels in the design hierarchy, namely, the behavioral, architectural, logic, circuit and physical levels. Using high threshold transistors at the place of low threshold leakage control transistors, result in more leakage power reduction as compared to LCT (leakage control transistor) technique but at the scarifies of area and delay.Also, there are many methods implemented in cmos logic.

## IX. Power analysis of Processors

The RISC has a complete instruction set, program and data memories, general purpose registers and a simple Arithmetical Logical Unit (ALU) for basic operations. In this design, most instructions are of uniform length and similar structure, arithmetic operations are restricted to CPU registers and only separate load and store instructions access memory. The analysis of any processor will give us wide view of power analysis of any circuits.[5]

## X. Conclusion

Any VLSI circuit will focus mainly on its trade-off factirs such as power, speed and area. The main factor which determines the performance of such circuit is power. The lower the power should be made. We cannot simply add any power reduction hardware into our design as it will lead to increase in area. Our paper focuses on designing a software tool which can analyze the system power also the optimization

## References


[1] Gary Yeap, " Practical l*ow-power digital VLSI Design*", Springer science business media,LLC,1998,pp. 4-81.

[2] Thursday, 3 July 2014, Accessed on May20,2020[Online] Available in*http://mantravlsi.blogspot.com/2014/07/power-analysis-in-vlsi-chip-dynamic.html*

[3] K. Gomina, J. Rigaud, P. Gendrier, P. Candelier and A. Tria, "*Power analysis methodology for secure circuits*," 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Karlovy Vary, 2013, pp. 102-107, doi: 10.1109/DDECS.2013.6549797.

[4] Synopsys proprietary "*Primetime PX methodology for power analysis*" version1.2, Aug,2006

[5] R. Uma "*Design and Performance Analysis of 8-bit RISC Processor using Xilinx Tool*" International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 2, Issue 2, Mar-Apr 2012, pp.053-058

[6] Jins Davis Alexander" *Simulation Based Power Estimation For Digital CMOS Technologies*"2008.

[7] Kaur, Kanika and Arti Noor. "POWER ESTIMATION ANALYSIS FOR CMOS CELL STRUCTURES." (2012).

[8] D. Brooks, V. Tiwari and M. Martonosi, "Wattch: a framework for architectural-level power analysis and optimizations," Proceedings of 27th International Symposium on Computer Architecture (IEEE Cat. No.RS00201), Vancouver, BC, Canada, 2000, pp. 83-94.