Wilkinson power divider

Microwave Design and Measurements (EERF 6396)
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Submitted By

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1. Introduction

Objectives:

- Design, simulate and build 3dB Wilkinson power divider with f_o = 2.5 GHz on 1.57-mm thick FR-4 material using AWR MWO (Axiem).
- Compare the measurement results and Axiem simulation results.

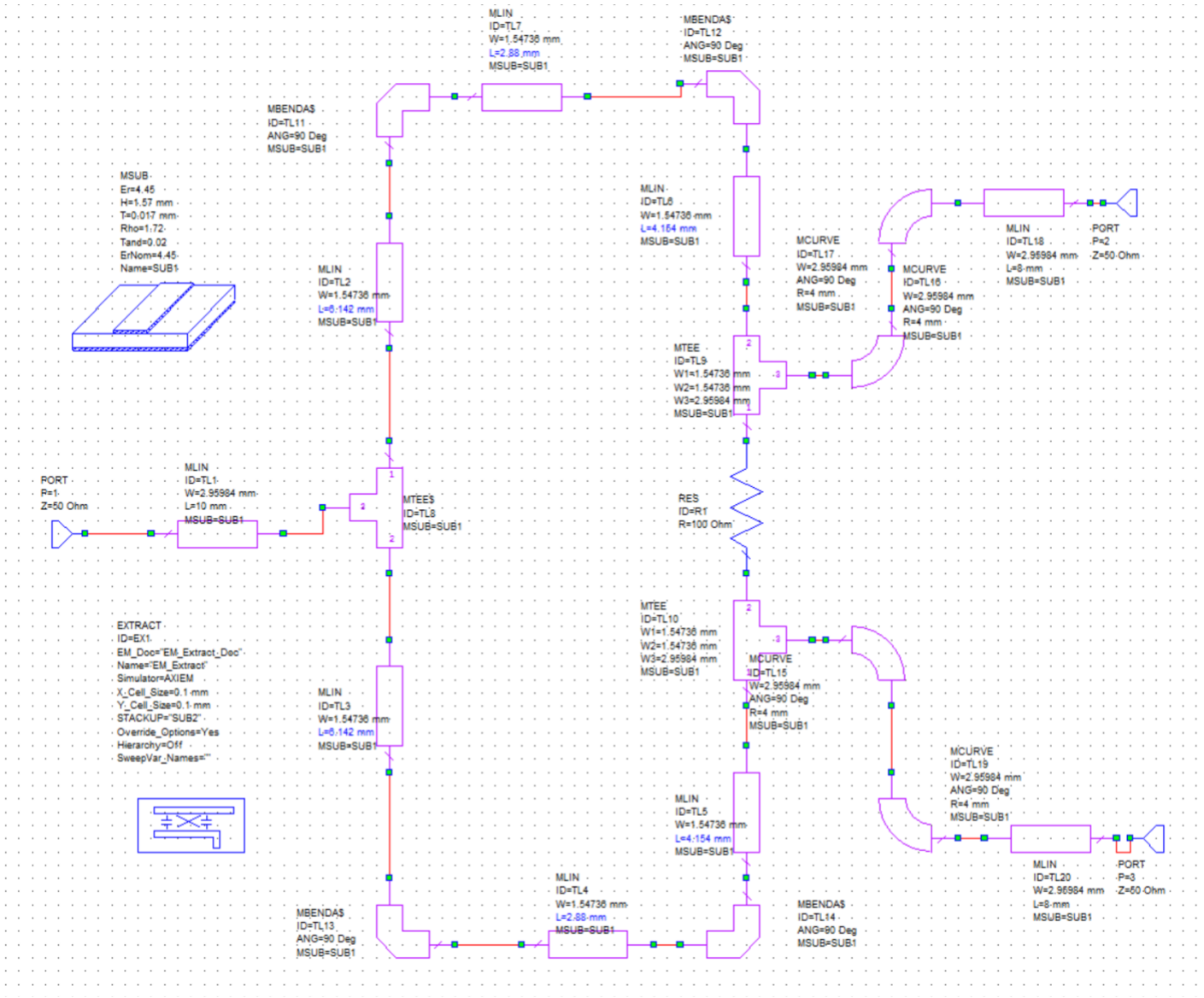
2. Design

A. Design Process

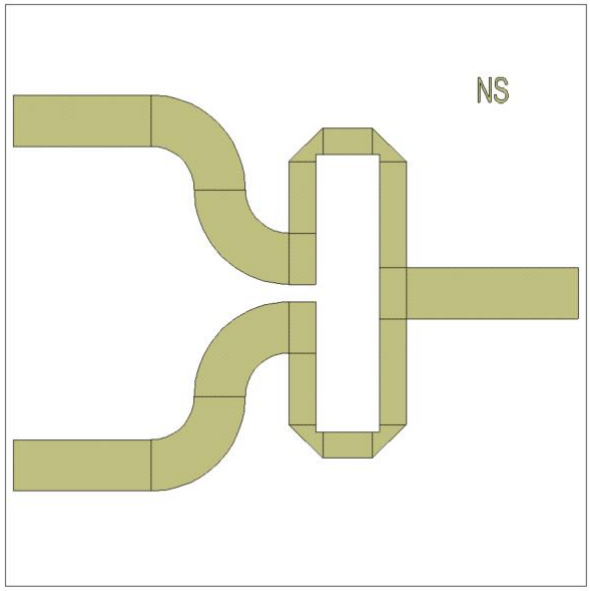
- 3-dB Wilkinson power divider is to be designed to work as an equal splitter.
- Tx line tool in AWR MWO was used to calculate the width, length and λeff values.
- In order to make it work as equal splitter, the length of microstrip lines from port 1(input port) to port2(output port) and port 1(input port) to port 3(output port) should be equal i.e. quarter wave length and impedance should be $\sqrt{2}\ Z_0$, which was calculated using Tx line tool.
- 100 Ω chip resistor (0603 case size) is used between two arms of power divider to give high isolation. The output lines in layout are separated quickly from 2 Z_0 resistor to avoid coupling between output lines.
- Distance between two arms of power divider is kept as per resistor size mentioned in data sheet as it is to be soldered in between two arms.
- Design was tuned in AWR MWO to achieve all design goals at f_o = 2.5 GHz.
- Axiem mesh was build and performance was recorded.
- S-parameters of the build circuit were measured in lab.

B. Figures related to design:

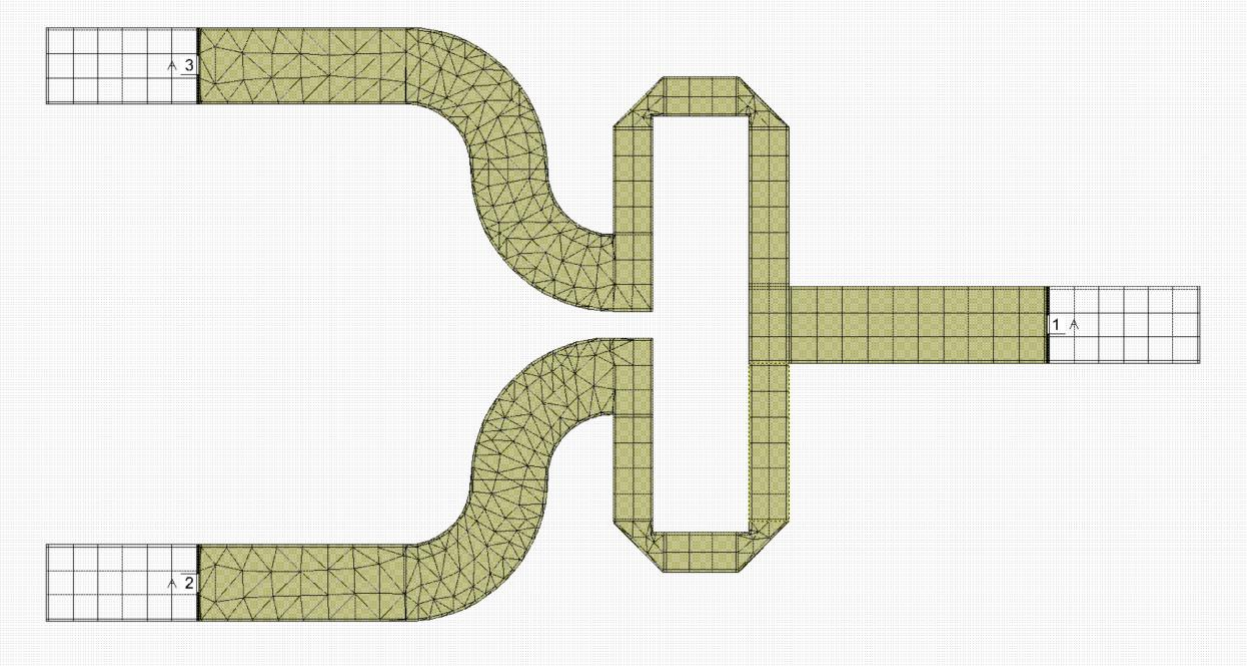
Circuit Schematic:



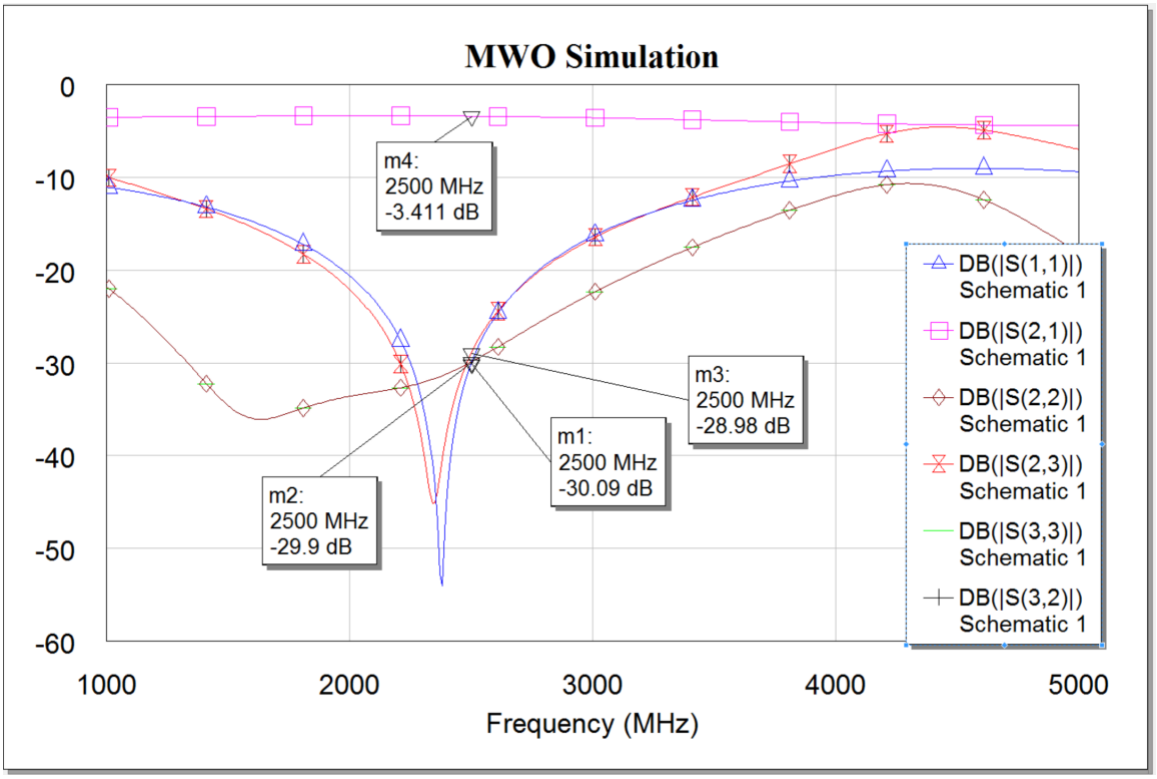
Layout:



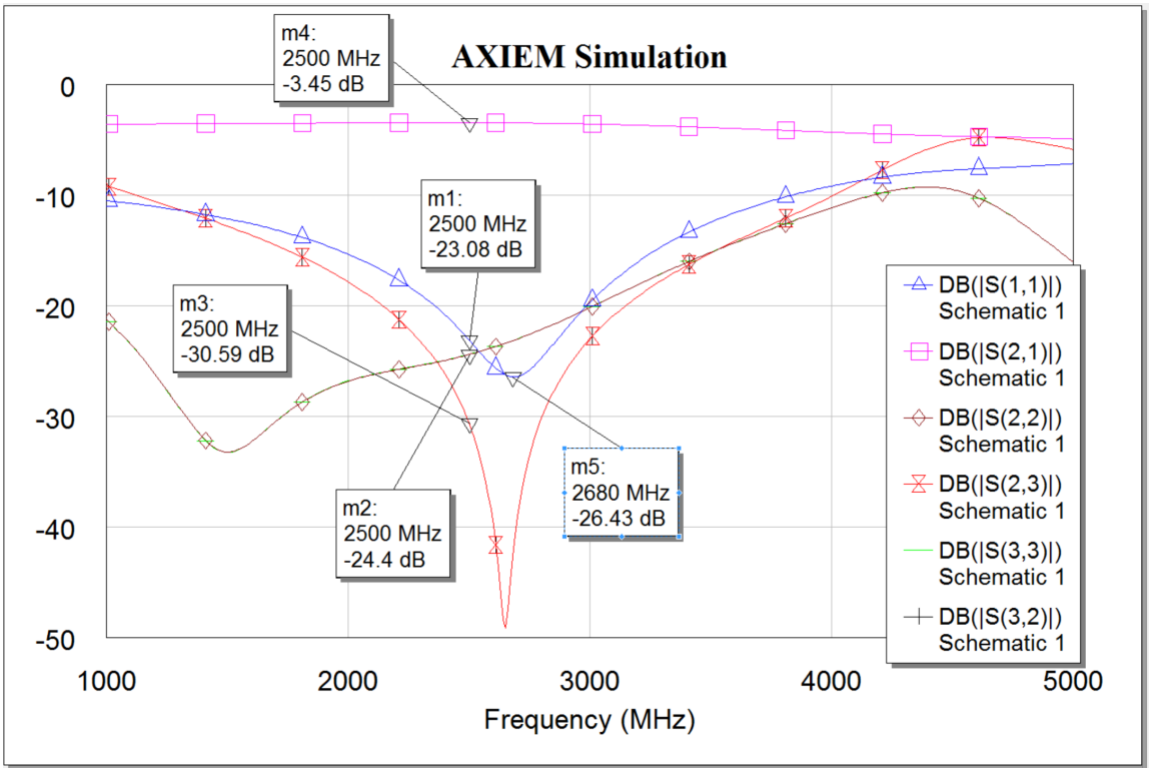
AXIEM Layout:



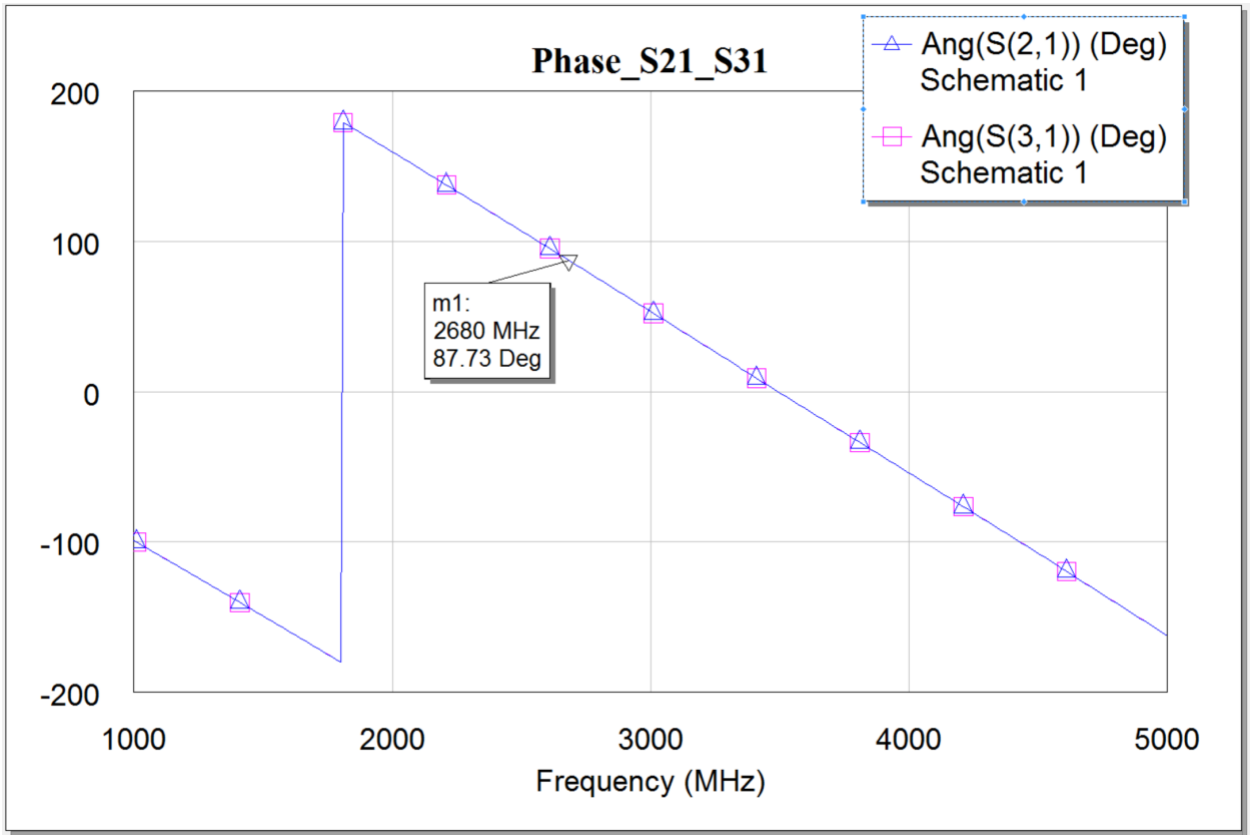
MWO Simulation:



AXIEM Simulation:

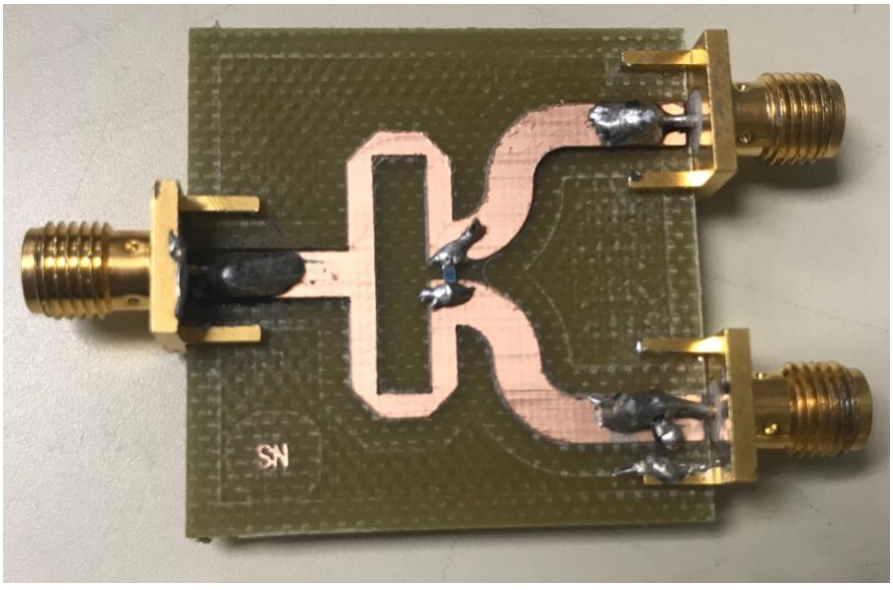


AXIEM S21 and S31 Phase Plot:

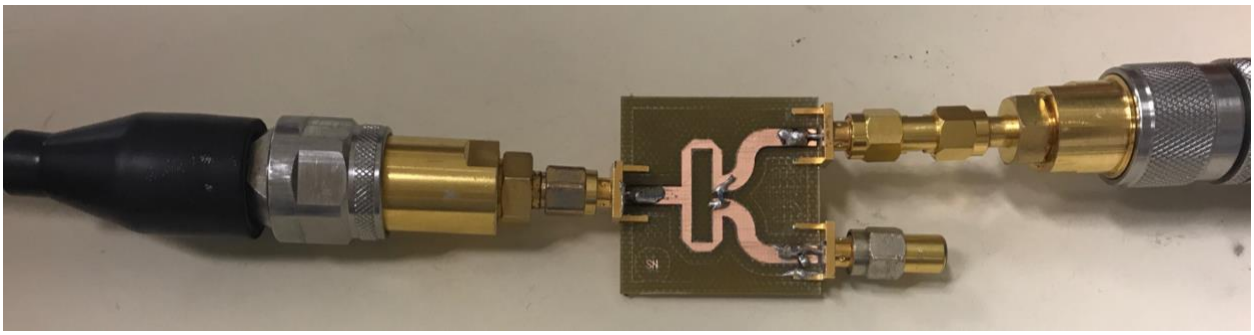


3. Measurement

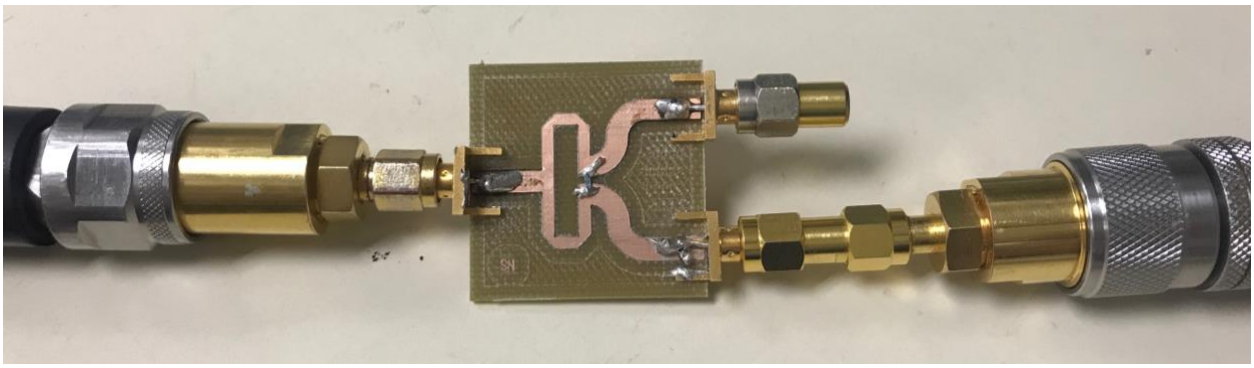
A. **Photographs of measured circuit:**



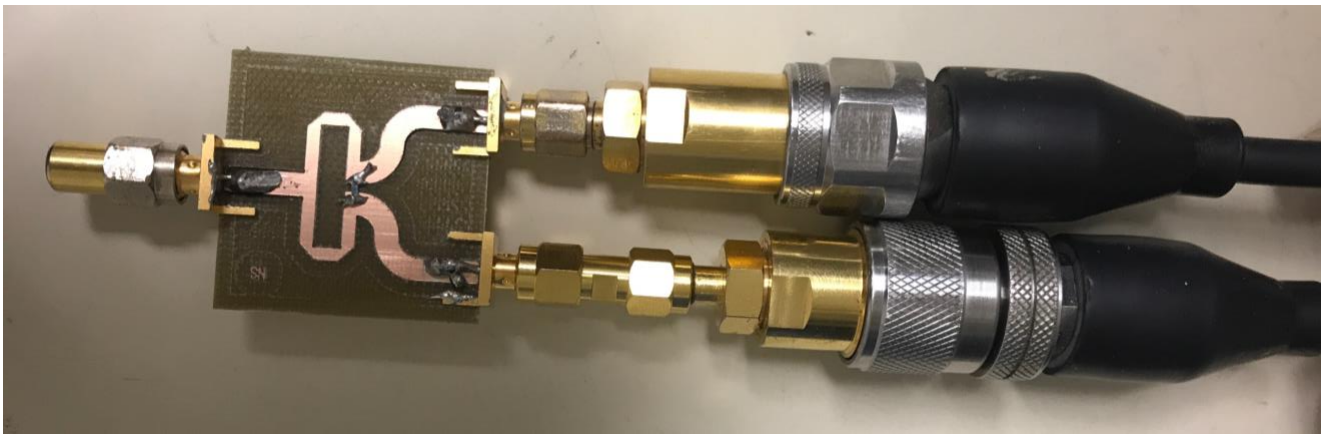
Input port-1, Output port-2, Port-3 is connected to 50-ohm load:



Input port-1, Output port-3, Port-2 is connected to 50-ohm load:

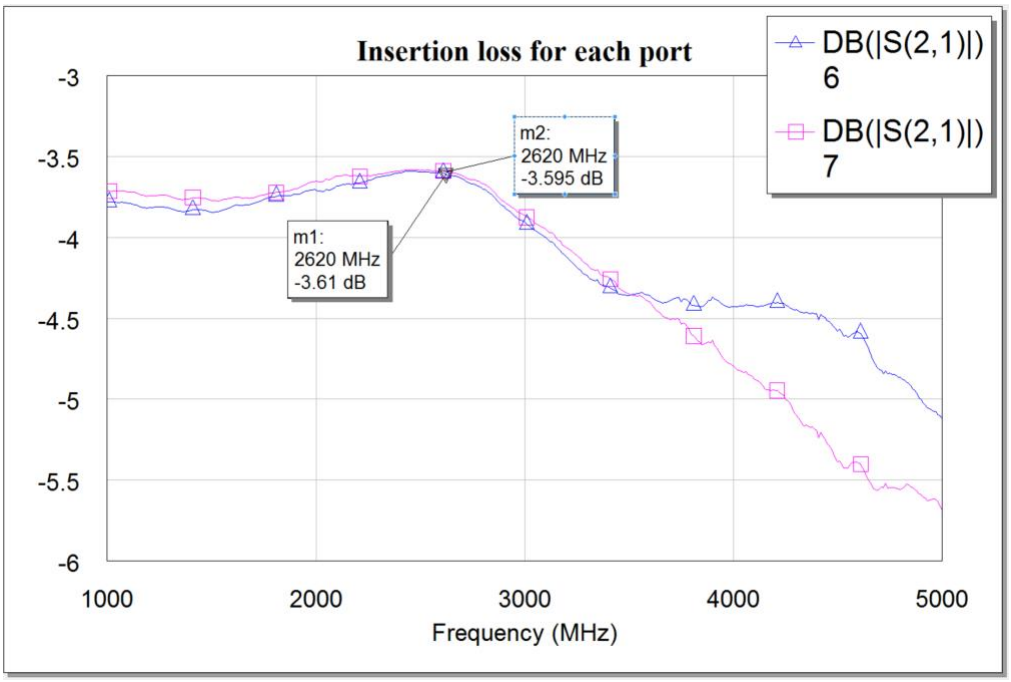


Input port-2, Output port-3, Port-1 is connected to 50-ohm load.



B. **Plots of Measured Data**

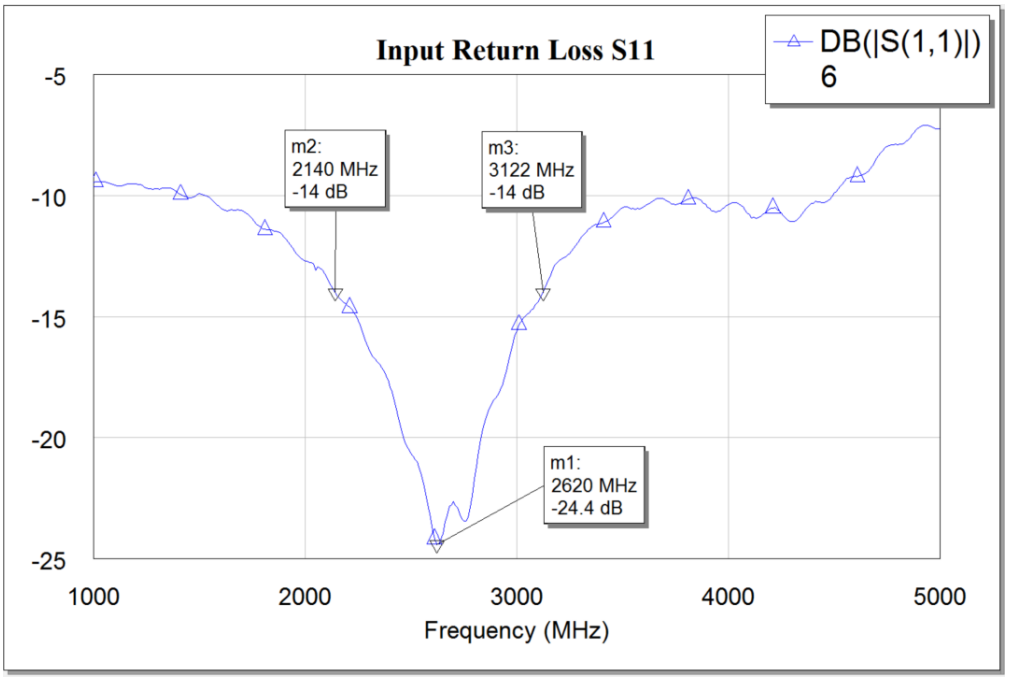
1. Insertion Loss for each Plot



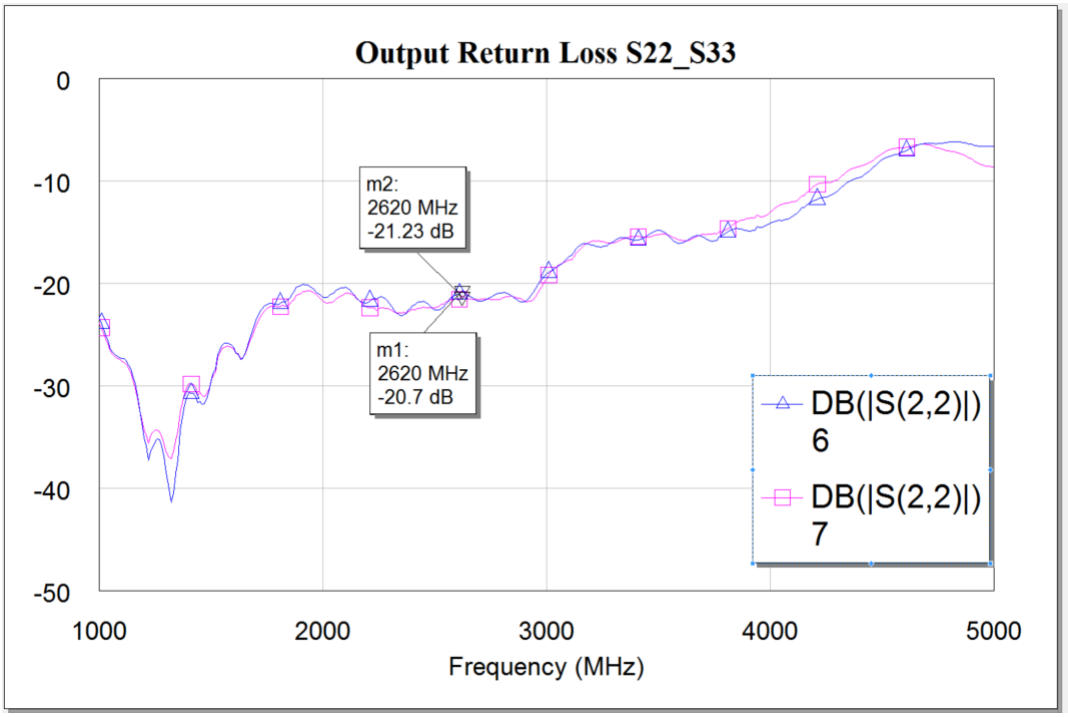
From the above plot, S21 = -3.61dB and S31 = -3.595 dB.

2. Return Loss

Input Return Loss:

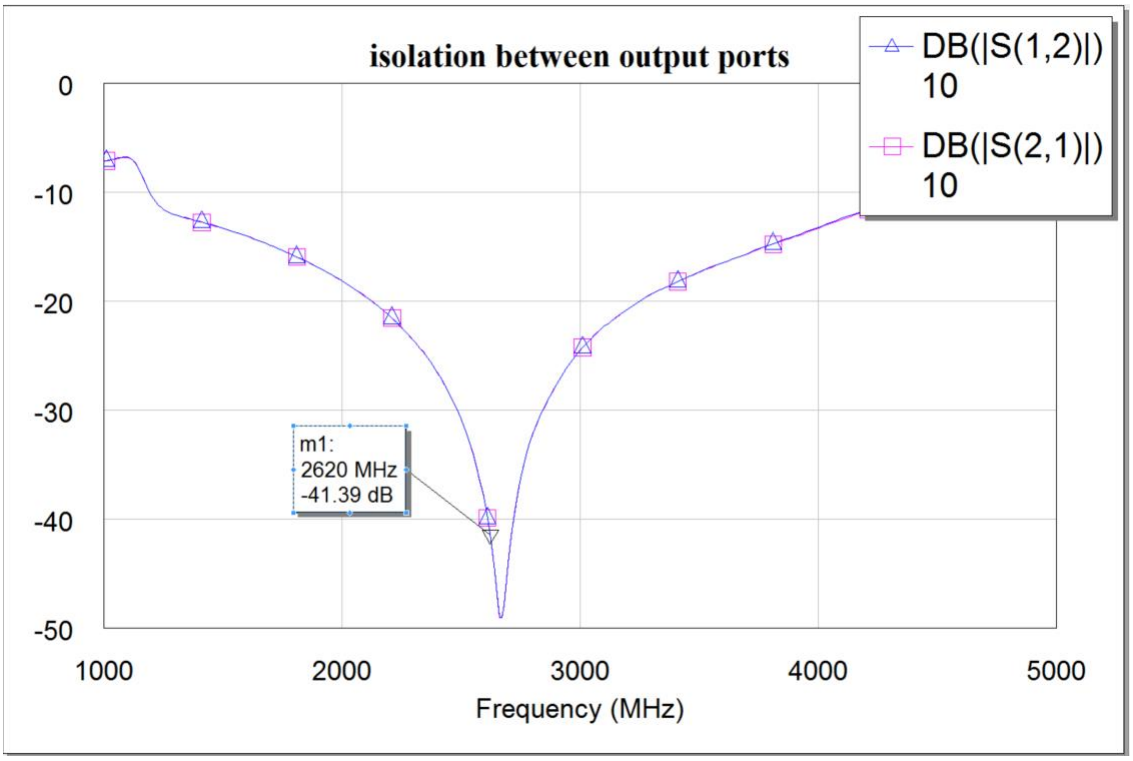


Output Return Loss:

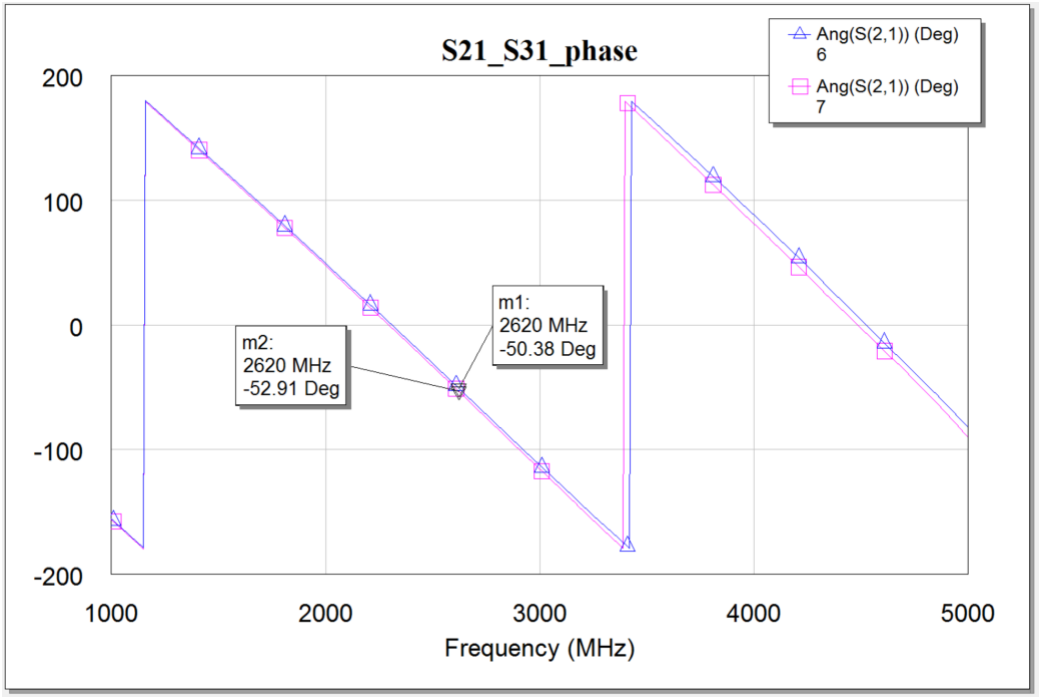


From the above plots, S11 = -24.4 dB, S22 = -20.7 dB, S33 = -21.23 dB.

3. Isolation between output ports

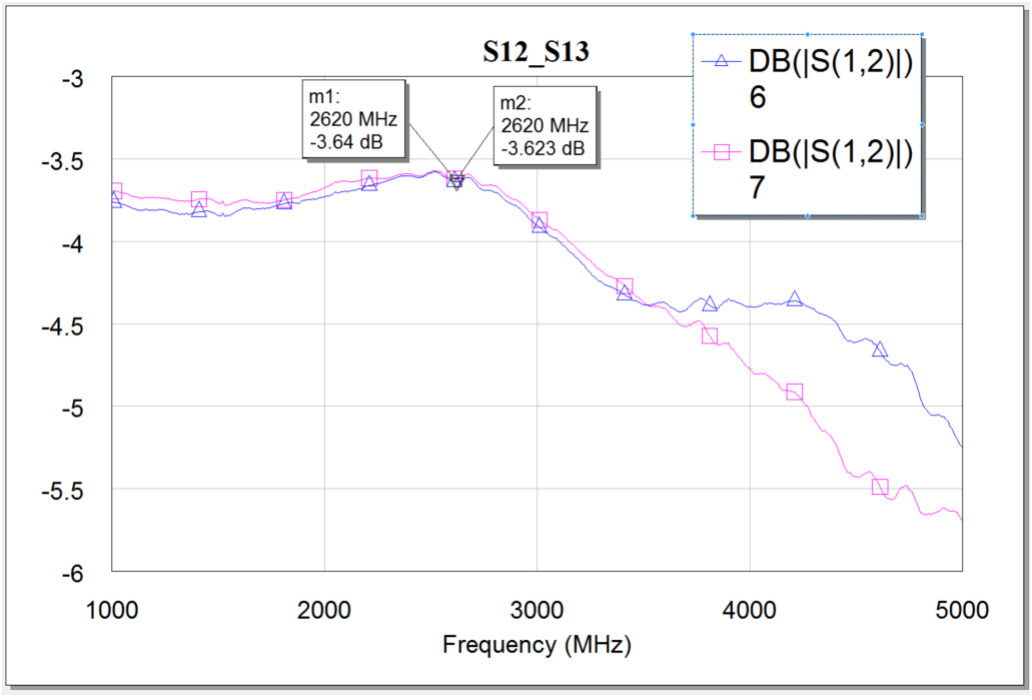


4. (S21 Angle) – (S31 Angle)



From the above plot, S21_phase = -50.38 deg, S31_phase = -52.91 deg.

5. S12 and S13



From the above plot, S12 = -3.64 dB, S13 = -3.623 dB.

C. **Summary**

Board Size = 33.6 mm x 33.6 mm

Board Thickness = varied from 1.5 mm to 1.6 mm.

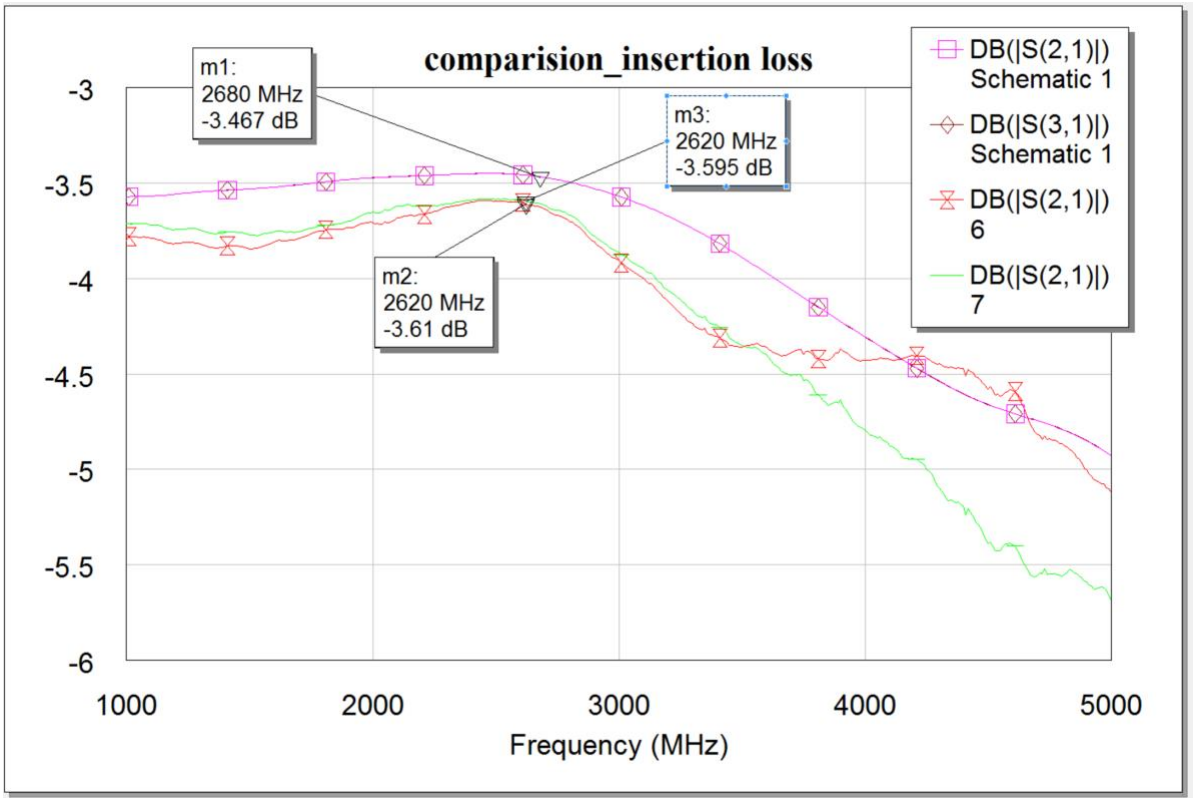
All the design goals were met for the resonant frequency 2.62 GHz (within +/- 5%).

The insertion loss between port 1 and port 2 is 0.61 dB and insertion loss between port 1 and port 3 is 0.595 dB. Input return loss and output return loss at port 2 and port 3 were greater than 20 dB. Isolation between output ports was 41.39 dB.

4. Analysis

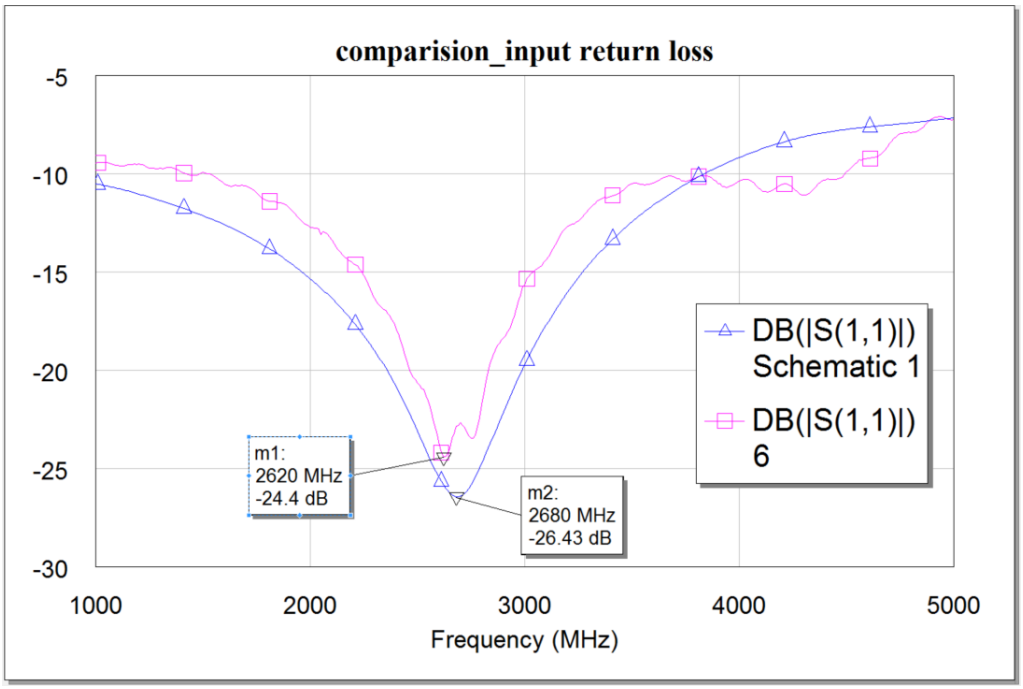
A. Comparison graph of predicted and measured graph

1. Insertion Loss for each Plot

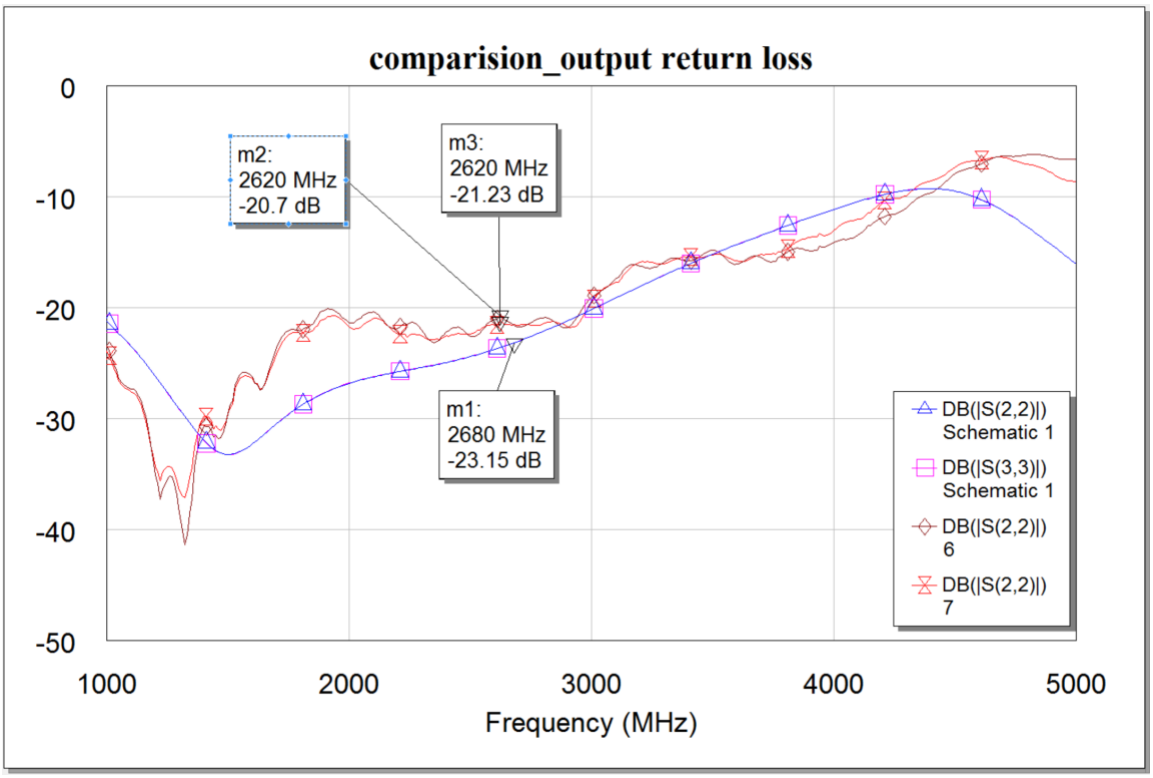


2. Return Loss

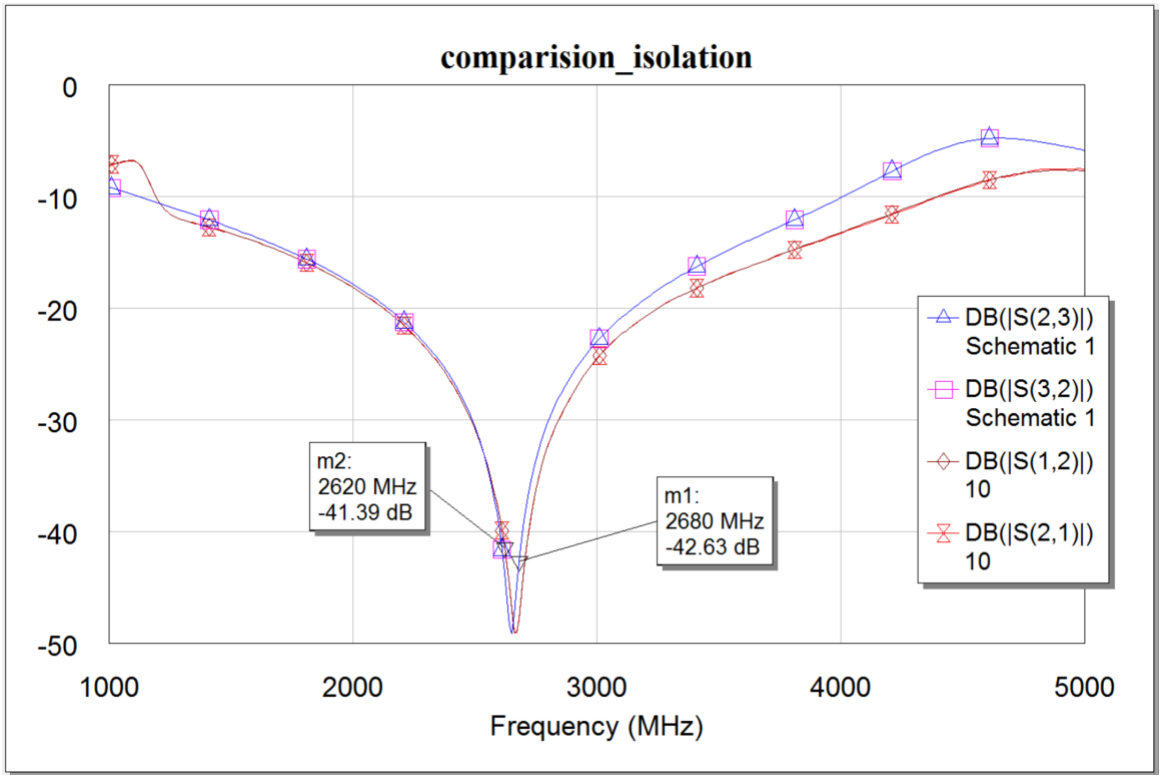
Input Return Loss:



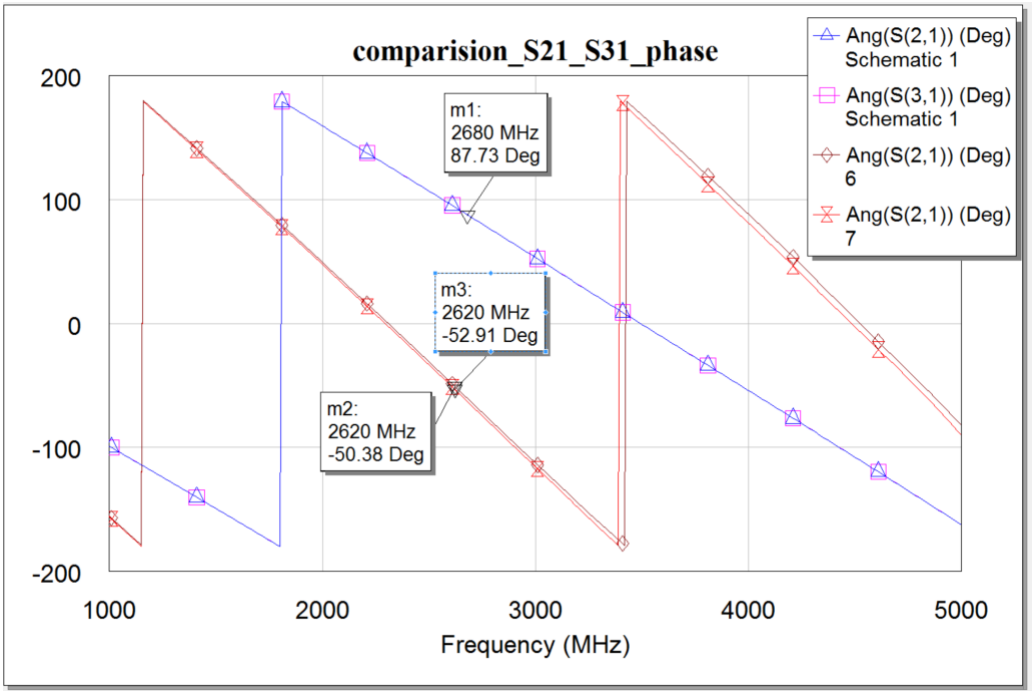
Output Return Loss:



3. Isolation between output ports



4. (S21 Angle) – (S31 Angle)



B. **Compliance matrix**

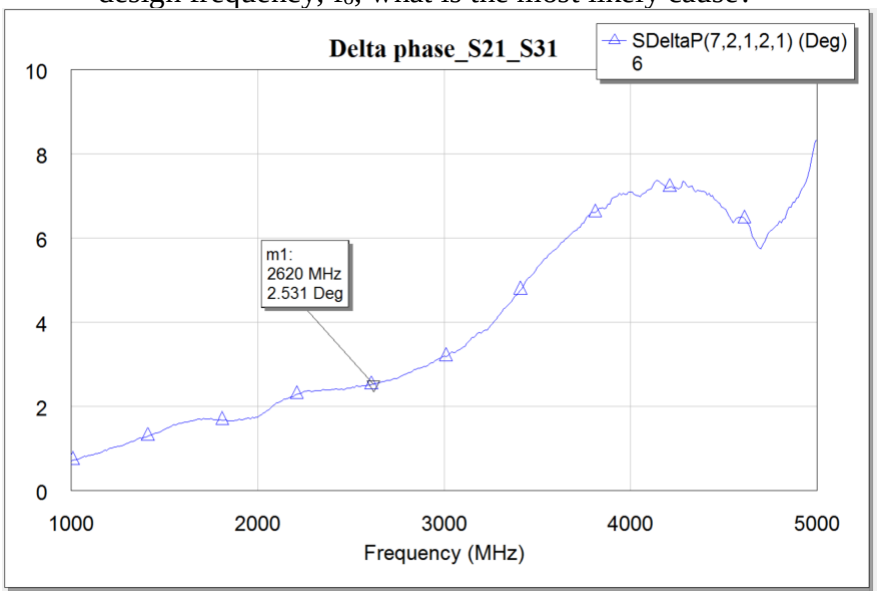
Parameter	Goal	Predicted	Measured	Complaint (+/- 5%)
Center Frequency (GHz)	2.5	2.68	2.62	Yes
Insertion Loss @ f_o at output port 2 (dB)	<1.0	0.467	0.61	Yes
Insertion Loss @ f_o at output port 3 (dB)	<1.0	0.467	0.595	Yes
Relative Phase (between output ports) (deg)	0	0	2.53	No
Input Return Loss @ f_o (dB)	>20	26.43	24.4	Yes
Output Return Loss at port 2 @ f_o (dB)	>20	23.15	20.7	Yes
Output Return Loss at port 3 @ f_o (dB)	>20	23.15	21.23	Yes
Isolation between output ports @ f_o (dB)	>20	42.63	41.39	Yes

C. **Summary**

1. Knowing that you designed your divider to have an intentional 3-dB split, what is the actual insertion loss in <u>each</u> arm of your divider (over and above your 3-dB split)?

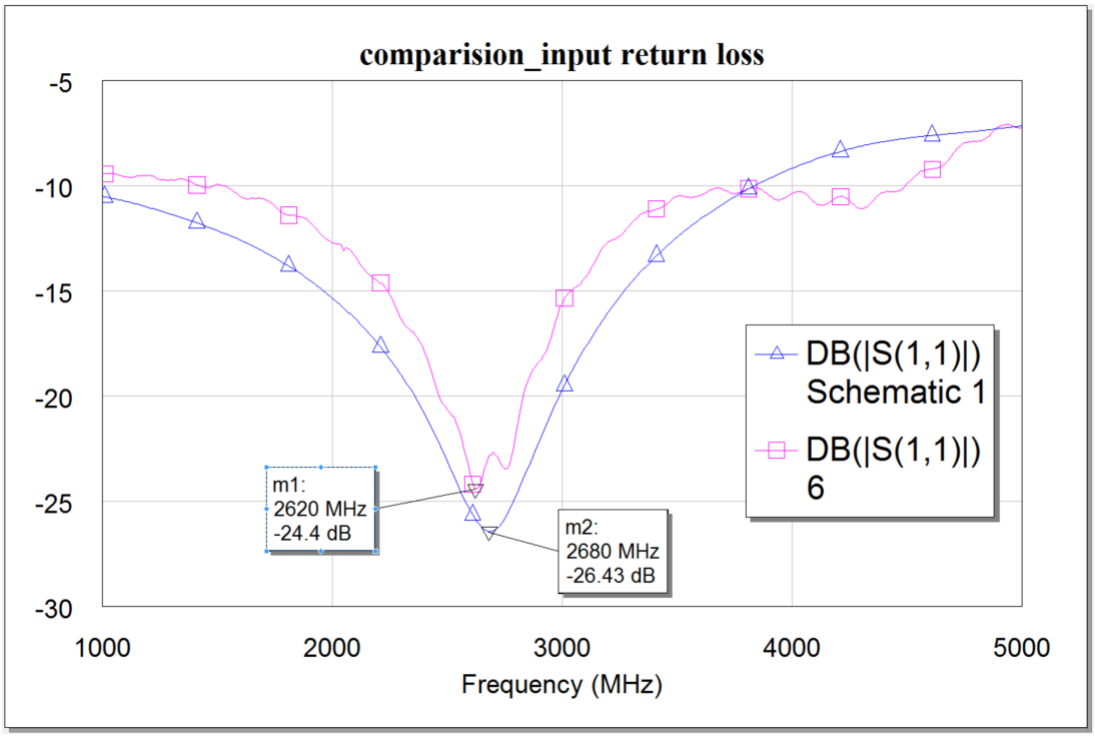
- From the measurement plots, S21=-3.61 dB and S31= -3.595 dB.
- Insertion loss for port 2 is 0.61 dB and insertion loss for port 3 is 0.595 dB.

2. Similar question regarding phase: we know this should be an equal-phase power divider. What is the delta phase between S21 phase and S31 phase? If it is not within +/- 3º at the design frequency, f_o, what is the most likely cause?



Delta phase between S21 and S31 is 2.531 deg which is within +/- 3 deg at design frequency.

3. At what frequency, did you measure the greatest return loss (in dB)? If it is not at the design frequency, f_o, what is the most likely cause of the shift?

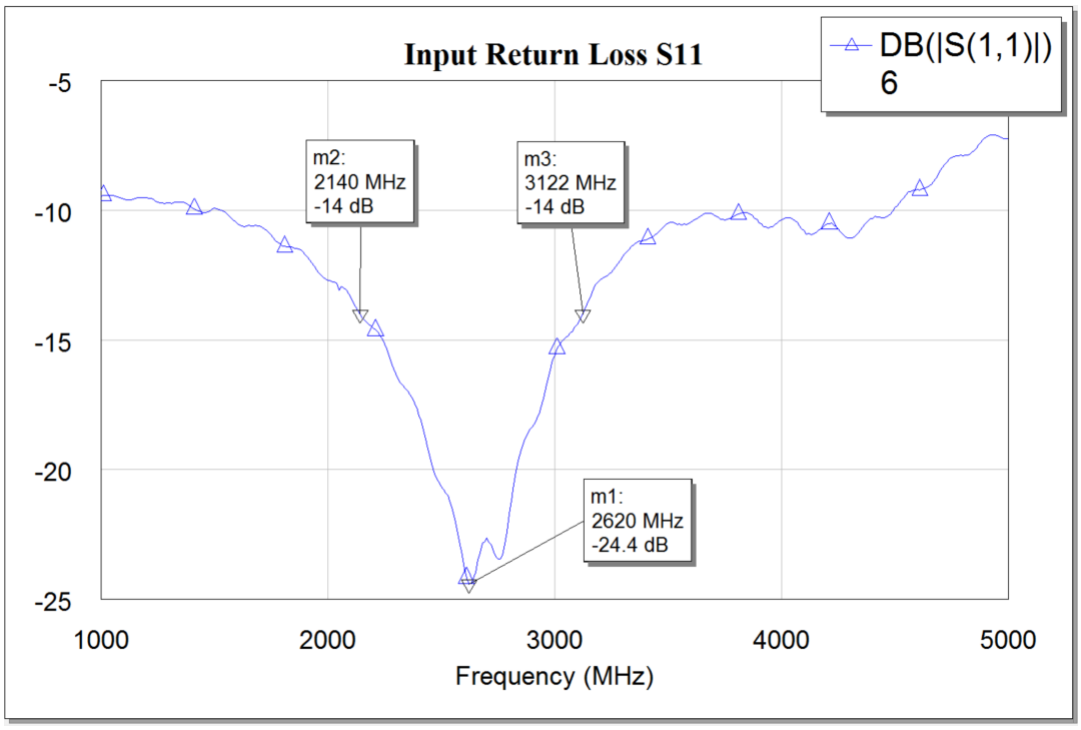


- As seen from the graph, greatest return loss (24.4 dB) is measured at 2.62 GHz.
- Design was tuned to have highest return loss at 2.68 GHz in AWR and measured highest return loss is at 2.62 GHz.
- The difference in predicted and measured values could be due to lossy nature of FR-4 substrate.

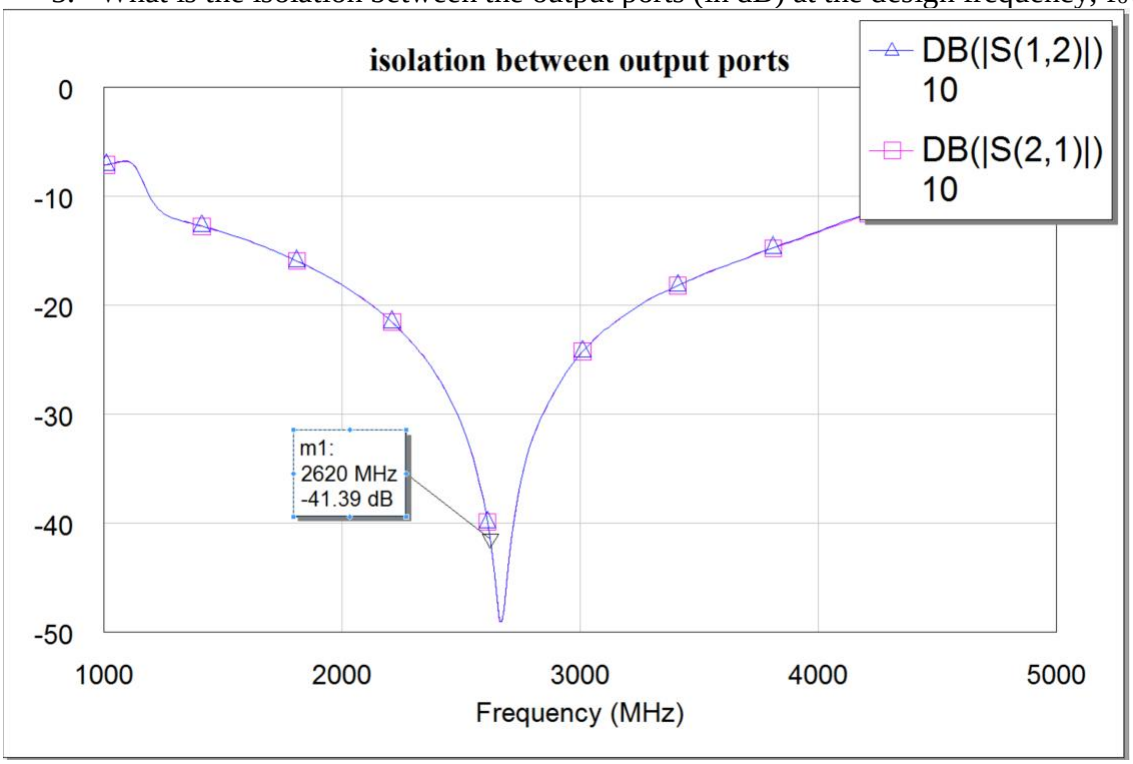
4. Using 14dB as the allowable worst-case measured return loss, what is the useable bandwidth for this power divider in absolute frequency (GHz) and percentage bandwidth (%)?

From the plot below:

- For 14 dB as the allowable worst-case measured return loss, the useable bandwidth for this design: Low cut off frequency = 2.140 GHz and high cut off frequency = 3.122 GHz.
- Absolute Bandwidth = 3.122 – 2.140 = 0.982 GHz.
- Percentage bandwidth = 37.48 %.



5. What is the isolation between the output ports (in dB) at the design frequency, f_o?



The isolation between the output ports is 41.39 dB. S23 = S32 = -41.39 dB

6. Construct a 3-port S-parameter matrix for your power divider

S[dB] = [-24.4 -3.64 -3.623

-3.61 -20.7 -41.39

-.3595 -41.39 -21.23]

5. Conclusion

A. Was the design successful? Why or why not?

All the design parameters were met except for relative phase between two output ports. Measured center frequency was at 2.62 GHz, which is within +/-5% of the design frequency (2.5 GHz). The insertion loss between port 1 and port 2 is 0.61 dB and insertion loss between port 1 and port 3 is 0.595 dB. Input return loss and output return loss at port 2 and port 3 were greater than 20 dB. Isolation between output ports was 41.39 dB.

B. What lessons did you learn from the lab?

From this lab, I learned that effective dielectric constant plays a great role in practical performance of circuit. As FR-4 has lossy nature, we need to take that into consideration while tuning the circuit in MWO.