

# DESIGN AND DEVELOPMENT OF DIGITAL CONTROLLER FOR GROUND BASED RADIOMETER USING FPGA

A PROJECT REPORT

*Submitted by*

SANANDIYA NIYATI HARJIVANBHAI (120170111059)

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VGEC, AHMEDABAD-382424

**Gujarat Technological University, Ahmedabad**

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Sanandiya Niyati H.

(Enrollment no.-120170111059)

VGEC, Chandkheda

## **Abstract**

In our day to day life, we are surrounded by numerous natural radiations present in the environment. The natural radiations are the result of emissions from resources like land, forests, rivers, oceans, deserts, etc. The study of these radiations plays an important role in climate predictions. Ground Based Radiometer (GBR) is a passive sensor which detects the natural emissions occurring in the environment and measures their intensity. Embedded Controller consists of a Digital Controller and Analog Front End (ADC). Digital Controller is a key block which performs functions like Control Signal Generation, Data Acquisition, Data Processing and Telecommand/Telemetry Interfacing. The end results of Digital Controller is used for weather forecast, agriculture, water resource management and disaster alerts.

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## **Acronyms**

FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
VHDL	Very High Speed Integrated Circuit Hardware Description Language
FSM	Finite State Machine
UART	Universal Asynchronous Receiver Transmitter
TSG	Timing Signal Generator
DSO	Digital Storage Oscilloscope
ISRO	Indian Space Research Organization
SAC	Space Applications Centre
MSDG	Microwave Sensors Digital Electronic Group
MSDPD	Microwave Sensors Data Acquisition & Processor Division
JTAG	Joint Test Action Group
PCB	Printed Circuit Board
UART	Universal Asynchronous Receiver/Transmitter

# **Chapter 1**

## **Introduction**

### **1.1 Organization Profile**

#### **Indian Space Research Organization (ISRO)**

Indian space research organization is the primary body for space research under the control of the Government of India, and one of the leading space research organizations in the world. Space activities in the country started at 15 August 1969 with the scientific investigation of the upper atmosphere and ionosphere over the magnetic equator. Dr. Vikram Sarabhai, the visionary leader envisioned that this powerful technology could play a meaningful role in national development and solving the problems of common man. Since inception, the Indian space program has been structured well and had three distinct elements such as, satellites for communication and remote sensing, the space transportation system and application programs.

Thus, the Indian Space program in the country, concentrated on achieving self-reliance and developing capability to build and launch communication satellites for television broadcast, telecommunications and meteorological applications; remote sensing satellites for management of natural resources.

#### **Space Applications Centre (SAC)**

Space Applications Centre is one of the major centre of the Indian Space Research Organization (ISRO). It is a unique center dealing with a wide variety of disciplines comprising design and development of payloads, societal applications, capacity building and space sciences, thereby creating a synergy of technology, science and applications. It is engaged in the research, development and demonstration of applications of space technology in the field of telecommunications, remote sensing, meteorology and satellite navigation (Sat Nav). This includes research and development of on-board systems, ground systems and end user equipment hardware and software.

Several national level application programs in the area of natural resources, weather and environmental studies, disaster monitoring/mitigation etc. also carried out. It is playing an important role in harnessing space technology for a wide variety of applications for societal benefits. The organizational structure continues to remain dynamic, responding to the needs of the hour. Some of the achievements of the Space Applications Centre include development of communication and meteorological payloads for INSAT satellites, optical and microwave payloads for IRS satellites.

### **Microwave Sensors Digital Electronic Group (MSDG)**

This is a group under MRSA area and is responsible for:

- Development of high speed high precision data acquisition system for active and passive microwave payloads.
- Development of payload controllers for autonomous operation of payloads such as phased array radar real time processors for payload such as SAR and Scatterometers.
- ASIC development for payload controller data acquisition system and on board processing.

### **Microwave Sensors Data Acquisition & Processor Division**

MSDPD is responsible for the design and development of:

- High speed high precision data acquisition system
- High speed waveform signal generator subsystems
- Onboard and ground based real time signal processing systems
- Field programmable gate array (FPGA) based digital designs
- Ground check out units for the onboard digital subsystems
- Software quality assurance related activities for real time signal processing software

## 1.2 Objective

*“How many times have you left home without an umbrella and got stuck in rain? Often, right!”*

So, weather forecast can help one for better day planning. In today's world, mankind is threatened by adverse effects of global warming such as floods, hurricanes, storms etc. The recent examples of these adverse effects are Uttarakhand floods and Jammu and Kashmir floods. The damage caused due to these natural disasters can be reduced to great extent with help of climate prediction system. Thus, climate prediction can help entire mankind leading to a brighter future.

## 1.3 Basic System Model

Input

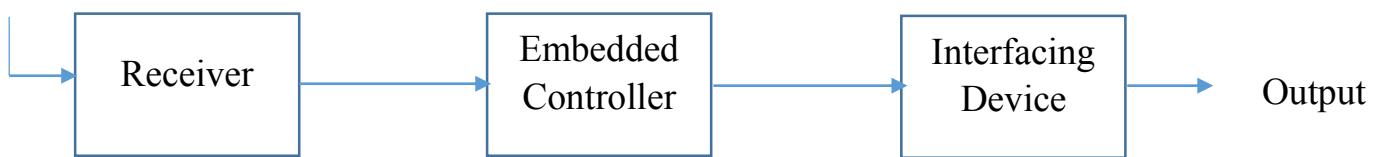


Figure No.:1.1 Basic System Model

- The system mainly consists of a Receiver, Embedded Controller and the Interfacing part.
- The input signals are analog signal emitted by natural resources which is to be converted to digital format for processing purpose.
- Receiver is the device that receives the radiations and converts them into usable form.
- Here, receiver used has intermediate frequency equals to 1 kHz.
- The Receiver is used to absorb the natural radiations from the environment surroundings and gives it as input to Embedded Controller.
- The Embedded Controller is used for controlling the entire system and data processing.
- The interfacing device is use to extract data from the system to data storage device such as laptop or PC.

## 1.4 Block Diagram

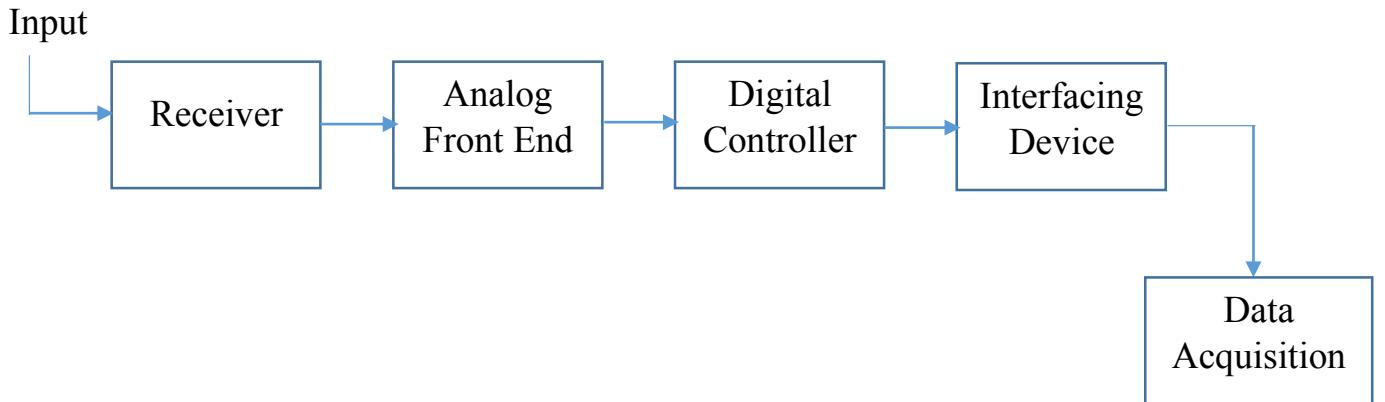


Figure No.:1.2 Block Diagram

- The input signals are analog signal emitted by natural resources which is to be converted to digital format for processing purpose.
- The receiver output is given as input to embedded controller.
- The Embedded Controller consists of two main blocks: Analog Front End and Digital Controller.
- The Analog Front End is the Analog to Digital Converter (ADC), as shown in the block diagram.
- The natural radiations from various natural sources like trees, oceans, deserts, lakes, etc. are in analog format.
- Due to the advantages of digital signal processing these radiations are converted into digital format using Analog to Digital Converter (ADC).
- The Digital Controller performs functions like Control Signal Generation, Data Acquisition, Data Processing and Telecommand/Telemetry Interfacing.
- The interfacing part is used for data acquisition for information display.
- The interface is the path for system output to equipment terminal through serial communication.
- Here, RS-232 interface is used to connect system output to PC USB terminal.

## **1.5 Features**

- High Accuracy
- Less Human Errors
- Reliable
- No human resource required
- Easy data access

## **1.6 Limitations**

- High Implementation cost
- Variations in the output due to atmospheric optical properties
- No mobility

## **1.7 Applications**

- Weather Forecast
- Agriculture purpose
- Water resource management
- Disaster alerts
- Better information on wind patterns can provide accurate forecast of a hurricane's track.
- Airline dispatchers would have enough time to reroute their airplanes appropriately.

## **Chapter 2**

### **System Working**

#### **2.1 Operation**

- Weather predictions or forecast for rain or storms are made by using parameters obtained from the natural radiations.
- Natural radiations are emitted by natural sources like land, forests, rivers, oceans, deserts, etc.
- Ground Based Radiometer is a device which detects and measures the intensity of radiations in the surrounding environment.
- Different types of sensors are used for detecting these natural radiations.
- There are two types of radar sensors: active radar sensors and passive radar sensors.
- Ground Base Radiometer is basically a passive sensor which detects and measures radiations occurring in environment.
- The radiations received by sensor are analog signals which need to be converted to digital by using Delta-sigma, Analog to Digital Converter (ADC).
- Delta-sigma ADC uses oversampling principle because of which aliasing effect can be avoided and information is not lost. Thus it increases the overall accuracy of the system.
- The digital output of ADC is given to FPGA module which works as integrator and controller.
- Timing and Control Signal Generator
- Digital filter will be implemented on FPGA so that noise can be filtered out and high stability is obtained.
- The digital output of FPGA module is then obtained through RS-232 interface which connects the output to PC USB terminal.

## 2.2 Functional Block Diagram

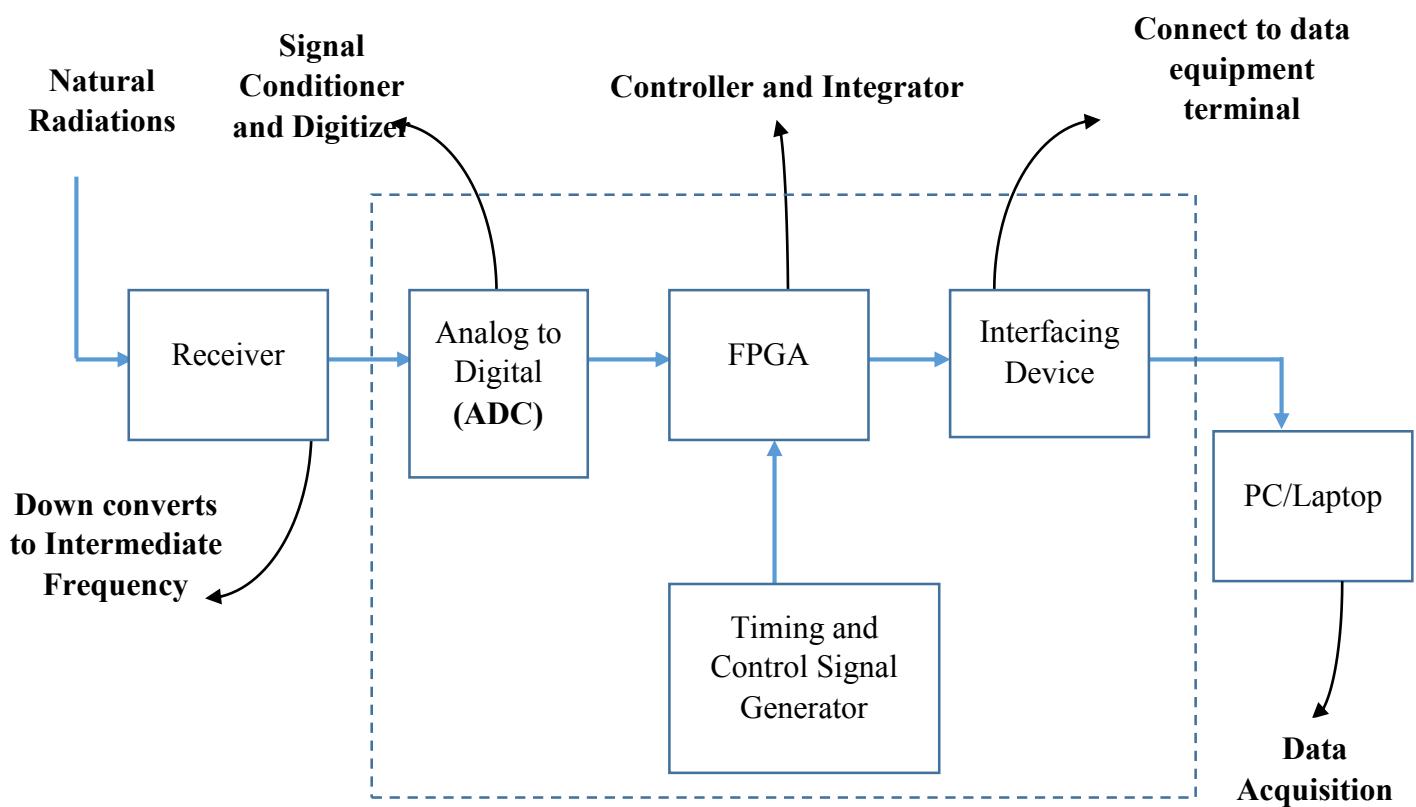


Figure No.:2.1 Functional Block Diagram

### 2.3 Working Flowchart

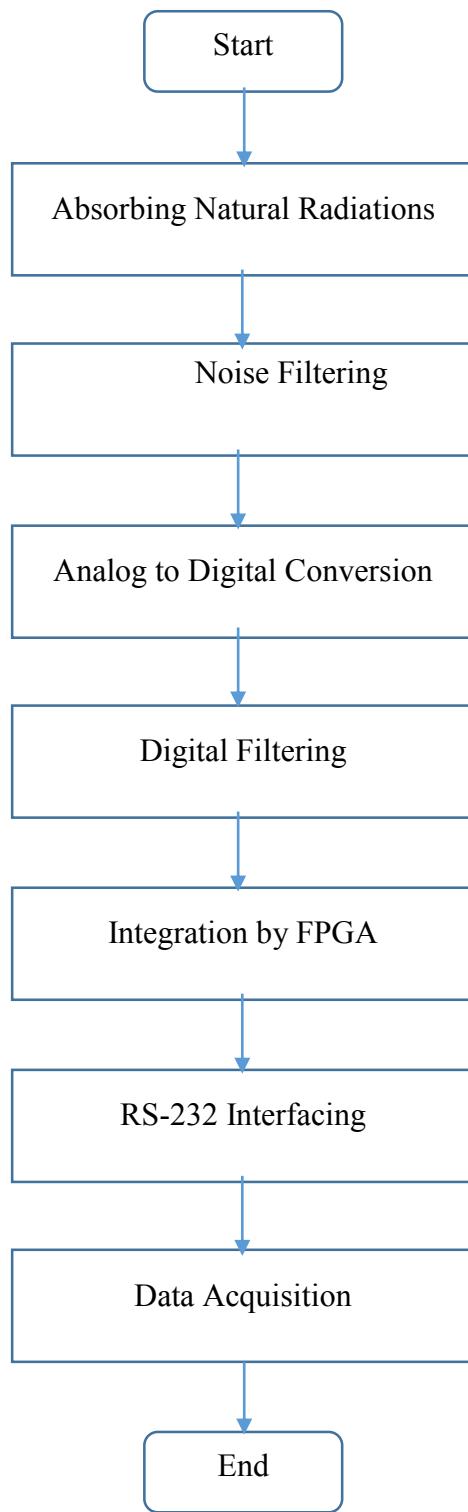


Figure No.:2.2 System Flow Chart

## 2.4 Modules and Tools

JTAG (Joint Test Action Group):

- Processors use JTAG for providing access to their debug/emulation function.
- FPGAs and CPLDs need JTAG to provide access to their programming functions.



Figure No.: 2.3 JTAG Connector

RS-232 Interface:

- It is used in serial communication for data transmission.
- Computers do not have RS-232 port so we have to use USB to Rs-232 port connector.
- It can be termed as Data Communication Equipment (DCE) or Data Terminal Equipment (DTE).



Figure No.:2.4 Rs-232 Interface

PC/Laptop:

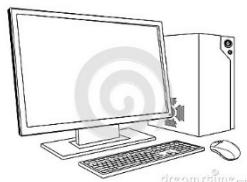


Figure No.:2.5 PC/Laptop

- The digital output generated by FPGA has to be interfaced with data equipment terminal.
- Here PC/Laptop is used for Data Acquisition or Information Display

DC Voltage Source:



Figure No.:2.6 DC Voltage Source

- A voltage source is a two terminal device which can maintain a fixed voltage.
- An ideal voltage source maintains constant voltage across its output terminals.
- Here, we are using Dc source to provide input to ADC.

Lambda Power Supply:



Figure No.:2.7 Lambda Power Supply

- TDK-Lambda, one of the world's leading power supply manufacturers, is offering wide selection of reliable AC-DC power supplies, DC-DC converters, DC-AC and so on.
- Here, we are using Lambda power supply to provide digital voltage to GBR board.

Field Programmable Gate Array (FPGA):



Figure No.:2.6 FPGA Module

- Semiconductor devices that consists of matrix of configurable logic blocks (CLBs) connected by programmable interconnects are called Field Programmable Gate Arrays (FPGAs).
- They contain hundreds of small blocks with flip-flops, combinational logic and memory.
- FPGA Architecture generally consists of array of logic blocks (known as configurable Logic Blocks, routing channels and I/O pads.

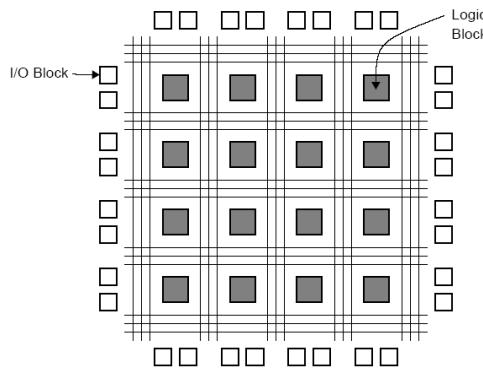


Figure No.:2.7 FPGA Architecture

Major Manufacturers:

- Xilinx
- Altera
- Lattice Semiconductor
- Microsemi
- SiliconBlue Technologies
- Archronix
- Quicklogic

Xilinx FPGA Families History:

1985	XC2064
1988	XC3020
1991	XC4000
1992	XC3100
1992	XC3200
1994	XC5000
1995	XC8100
1995	XC6200
1998	Virtex
1998	Spartan

1999	Virtex-E
2000	Spartan-II
2000	Virtex-EM (1 Mb memory on-chip)
2001	Virtex-II
2002	Virtex-II Pro (PowerPC hard core)
2003	Virtex-II Pro X (Rocket PHY)
2005	Virtex-IV
2005	Spartan-3E
2006	Virtex-5
2007	Spartan-3A(N)
2008	Virtex-5 FXT
2009	Virtex-6, Spartan-6
2010	Xilinx 7: Virtex, Artix, Kintex

Table No.: 2.1 Xilinx FPGA Families History

Advantages:

- Short time to market
- Fast and efficient systems
- Real time applications
- Parallel data processing
- Low cost
- Long time maintenance
- High reliability
- Better performance
- Easy to design
- High flexibility

Applications:

- Aerospace
- Defense
- Cryptography
- Wireless Communications
- Image Processing
- Software defined radio
- Medical purpose
- Bioinformatics

- Security systems
- Metal detection
- Industrial applications
- Computer hardware emulation
- Data Storage
- Broadcast
- Automotive
- ASIC prototyping
- High speed signal processing
- Speech recognition
- Radio astronomy

### **Spartan-3AN features:**

- Connect to DDR2 memory for rapid data transfer using proven memory interface controller.
- Prototype countless applications with support for 26 single-ended and differential I/O standards.
- Multiboot pre-programmed reference designs in a single session.
- Safeguard your designs
- Shorten development time with pre-verified design files and schematics.
- Flexible power management modes.

### **Delta-sigma ADC:**



Figure No.:2.8 Delta-sigma ADC (ADS1278)

### **Key Features:**

- Simultaneously Measure Four/Eight Channels
- Up to 144kSPS Data Rate
- Linear Phase Digital Filter

- SPI™ or Frame-Sync Serial Interface
- Low Sampling Aperture Error
- Modulator Output Option (digital filter bypass)
- Analog Supply: 5V
- Digital Core: 1.8V
- I/O Supply: 1.8V to 3.3V
- AC performance:
  - 70kHz Bandwidth
  - 111dB SNR (High-Resolution Mode)
  - 108dB THD
- DC Accuracy:
  - 0.8 $\mu$ V/°C Offset Drift
  - 1.3ppm/°C Gain Drift

Selectable Operating Modes:

High-Speed: 144kSPS, 106dB SNR

High-Resolution: 52kSPS, 111dB SNR

Low-Power: 52kSPS, 31mW/ch

Low-Speed: 10kSPS, 7mW/ch

Advantages:

- High Resolution
- High Accuracy
- High Speed
- Good tradeoff between speed and cost
- Low power
- High stability
- Digital Filtering

Disadvantages:

- Low speed due to over sampling principle
- Cycle latency

## Chapter 3

### Printed Circuit Board (PCB)

#### 3.1 Introduction

- A printed circuit board (PCB) mechanically supports and electrically connects electronic components using conductive tracks, pads and other features etched from copper sheets laminated onto a non-conductive substrate.
- PCBs can be single sided (one copper layer), double sided (two copper layers) or multi-layer (outer and inner layers). Conductors on different layers are connected with vias. Multi-layer PCBs allow for much higher component density.
- There are many three types of PCBs:
  - i. Single-sided PCB
  - ii. Double-sided PCB
  - iii. Multi-layer PCB

#### Terminology:

- **Annular ring** - the ring of copper around a plated through hole in a PCB.
- **DRC** - design rule check. A software check of your design to make sure the design does not contain errors such as traces that incorrectly touch, traces too skinny, or drill holes that are too small.
- **Drill hit** - places on a design where a hole should be drilled, or where they actually were drilled on the board. Inaccurate drill hits caused by dull bits are a common manufacturing issue.
- **Finger** - exposed metal pads along the edge of a board, used to create a connection between two circuit boards. Common examples are along the edges of computer expansion or memory boards and older cartridge-based video games.
- **Pad** - a portion of exposed metal on the surface of a board to which a component is soldered.
- **Panel** - a larger circuit board composed of many smaller boards which will be broken apart before use. Automated circuit board handling equipment frequently has trouble with smaller boards, and by aggregating several boards together at once, they process can be sped up significantly.

- **Plane** - a continuous block of copper on a circuit board, define by borders rather than by a path. Also commonly called a “pour”.
- **Silkscreen** - the letters, number, symbols and imagery on a circuit board. Usually only one color is available, and resolution is usually fairly low.
- **Slot** - any hole in a board which is not round. Slots may or may not be plated. Slots sometimes add to add cost to the board because they require extra cut-out time.
- **Solder mask** - a layer of protective material laid over the metal to prevent short circuits, corrosion, and other problems.
- **Solder jumper** - a small, unwanted blob of solder connecting two adjacent pins on a component on a circuit board.
- **Surface mount** - construction method which allows components to be simply set on a board, not requiring that leads pass through holes in the board. This is the dominant method of assembly in use today, and allows boards to be populated quickly and easily.
- **Thermal** - a small trace used to connect a pad to a plane. If a pad is not thermally relieved, it becomes difficult to get the pad to a high enough temperature to create a good solder joint. An improperly thermally relieved pad will feel “sticky” when you attempt to solder to it, and will take an abnormally long time to reflow.
- **Thieving** - hatching, gridlines, or dots of copper left in areas of a board where no plane or traces exist. Reduces difficulty of etching because less time in the bath is required to remove unneeded copper.
- **Trace** - a continuous path of copper on a circuit board.
- **V-score** - a partial cut through a board, allowing the board to be easily snapped along a line.
- **Via** - a hole in a board used to pass a signal from one layer to another. *Tented* vias are covered by solder mask to protect them from being soldered to. Vias where connectors and components are to be attached are often *untended* (uncovered) so that they can be easily soldered.

### 3.2 PCB Designing Steps

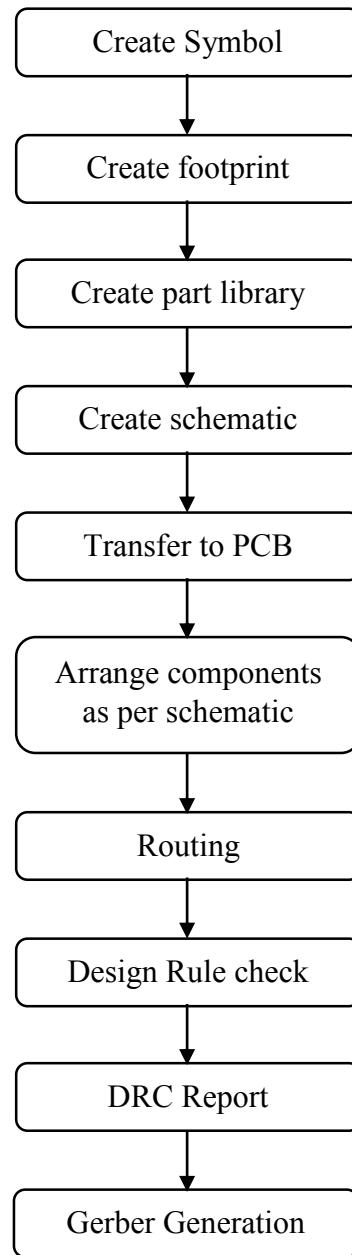


Figure No.:3.1 PCB Designing Steps

### 3.3 PCB Fabrication Steps

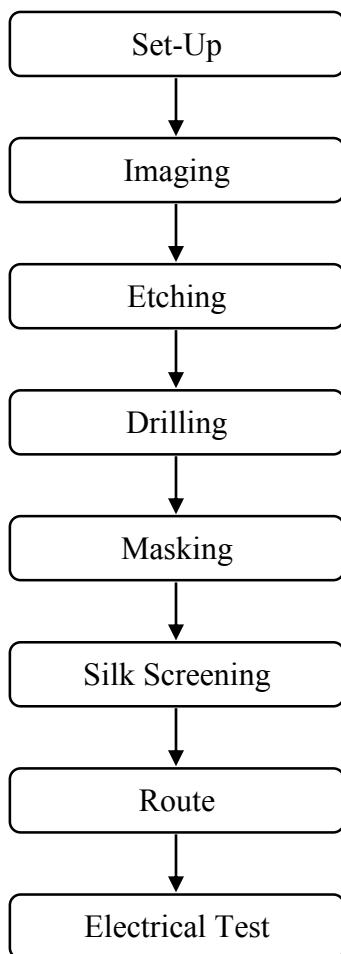


Figure No.:3.2 PCB Fabrication Steps

## **3.4 Power Supply Check**

### **3.4.1 Output Calculations**

#### **Module U11 (for ADC):**

Output Required: 1.8V

$$\mathbf{V_{OUT} = 1.25 (1 + (R_2/R_1))}$$

- $V_{OUT} = 1.25 (1 + (180/470))$
- $V_{OUT} = 1.728V$

#### **Module U12 (for ADC, op-amp, VREF):**

Output Required: 5V

$$\mathbf{V_{OUT} = 1.25 (1 + (R_2/R_1))}$$

- $V_{OUT} = 1.25 (1 + (220/68))$
- $V_{OUT} = 5.294V$

#### **Module U13 (for ADC):**

Output Required: 3.3V

$$\mathbf{V_{OUT} = 1.25 (1 + (R_2/R_1))}$$

- $V_{OUT} = 1.25 (1 + (56/33))$
- $V_{OUT} = 3.371V$

### **3.4.2 Test Result**

#### **Module U11 (for ADC):**

- Input Voltage: 12.1V
- Output Voltage: 1.71V

#### **Module U12 (for ADC, op-amp, VREF):**

- Input Voltage: 12.1V
- Output Voltage: 5.22V

#### **Module U13 (for ADC):**

- Input Voltage: 12.1V
- Output Voltage: 3.34V

#### **Module U14 (for FPGA):**

- Input Voltage: 12.1V
- Output Voltage: 1.19V

### 3.5 Impedance Check

Voltage	Pin connection	Impedance value (ohm)
+12V	K3- pin no. 12,13	11.56M
+5VA	Pin no. 2 of U12	263.3
+1.2V	Pin no. 2 of U14	49.2
+1.8V	Pin no. 2 of U11	64.9
3.3VA	Pin no. 2 of U13	83.8
+3.3VD	Pin no. 2 of L5	85.1
+3.3V_ZB	Pin no. 2 of L6	83.8

Table No.:3.1 Impedance Check

### 3.6 Hardware Problems and Solutions

- i. During power supply check, error was detected in output of U13 module. Voltage regulator IC (lm1085) not functioning properly.

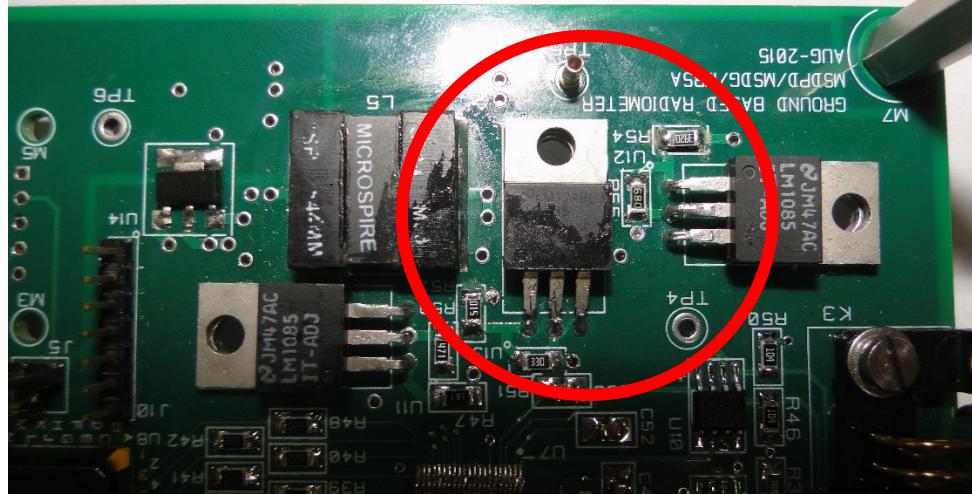


Figure No.:3.3 Hardware Problem (1)

Solution: The ground of voltage regulator IC was not shorted to common GND. The error was corrected by soldering this connection properly.

ii. The connection loose between C60 and C65.

Solution: External wire connection was used for this connection.

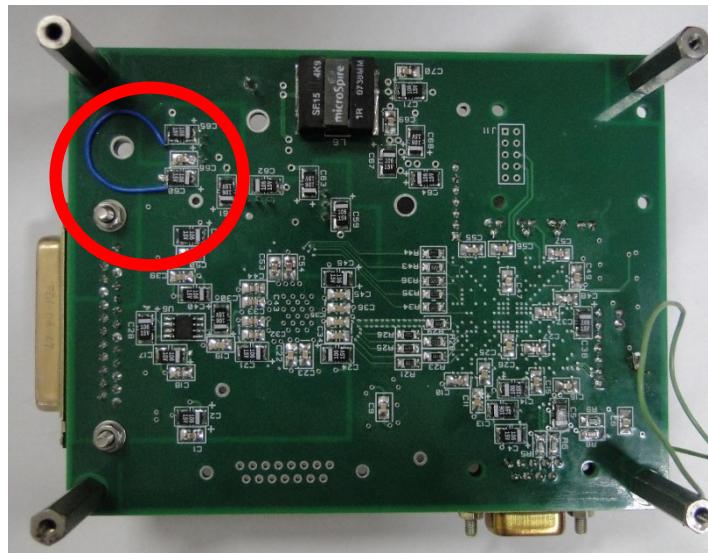


Figure No.:3.4 Hardware Problem (2)

iii. Footprint of crystal oscillator was not according to the component.

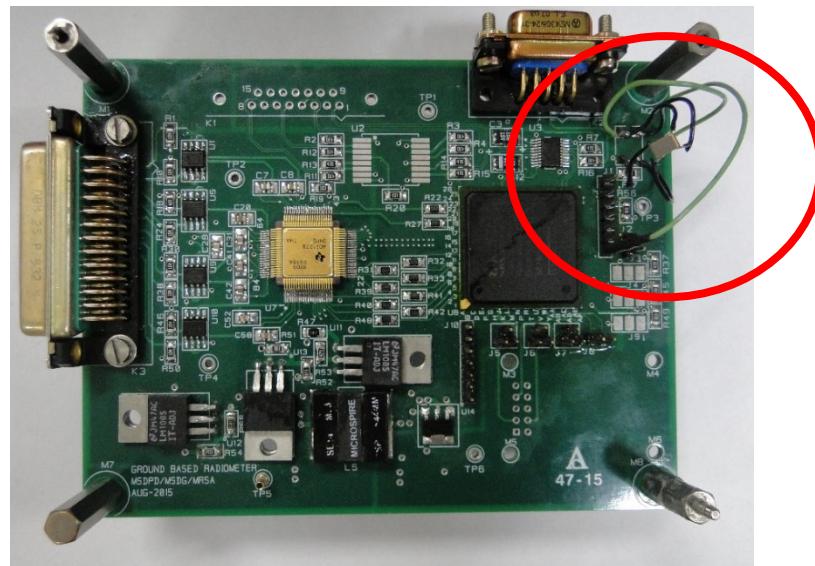


Figure No.:3.5 Hardware Problem (3)

Solution: The X1 crystal oscillator was connected with external wire connection.

iv. X1 crystal oscillator was not getting input voltage and hence it was not working.

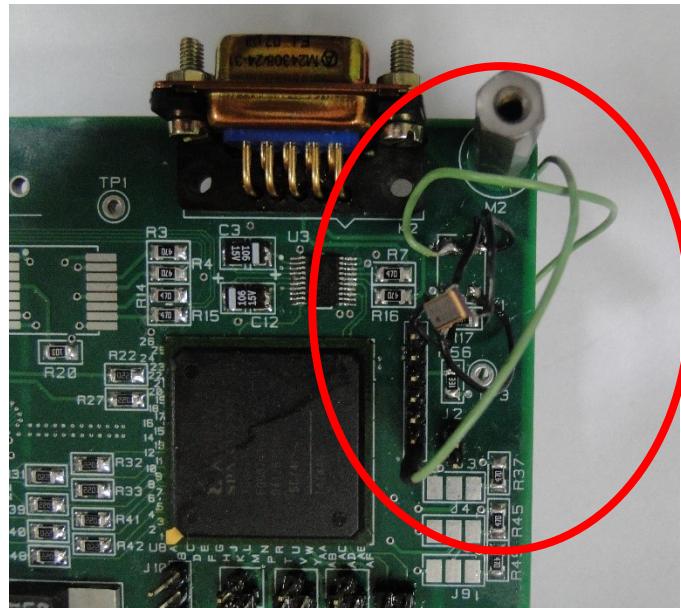


Figure No.:3.6 Hardware Problem (4)

Solution: The input voltage was given to crystal oscillator through external connection.

### 3.7 GBR Board

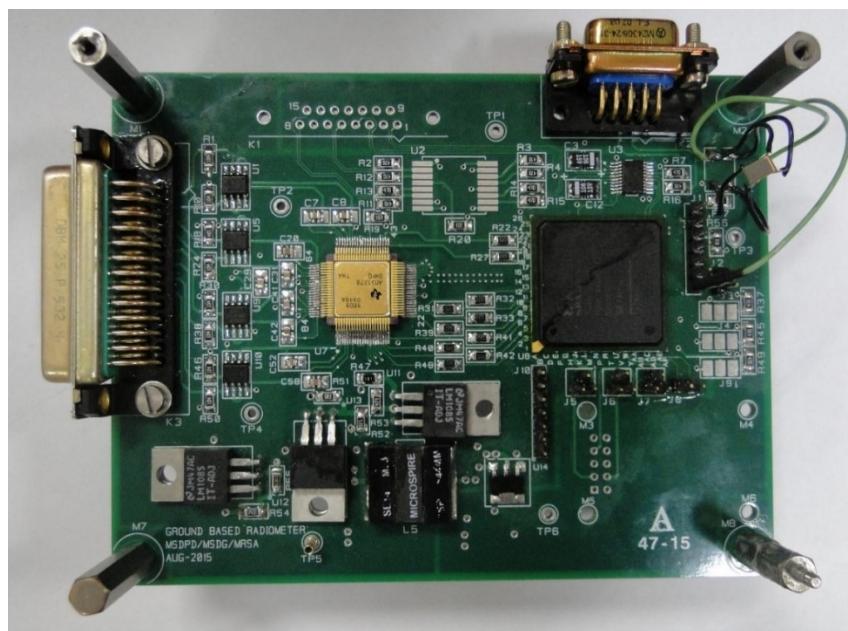


Figure No.: 3.7 GBR Board Top Side

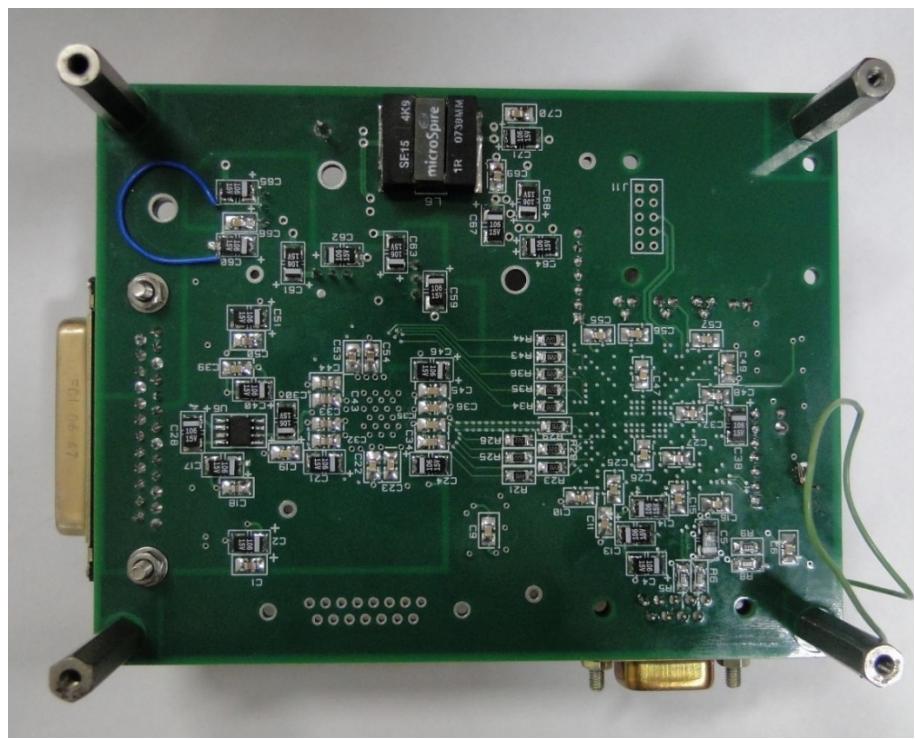


Figure No.: 3.8 GBR Board Bottom Side

# Chapter 4

## Implementation

### 4.1 Baud-Rate Generator

#### 4.1.1 Detail Description

- The baud rate is a sample per second which are generated on the clocks generated according to the calculations.
- The different baud rates are 600, 1200, 4800, 9600, 14400, 19200, 28800, 38400, 56000, 57600, 115200, 12800 and 256000.
- If proper baud rate is not generated, then the correct output is not generated. It gives the random output, which generate the errors in the output.
- Baud Rate Generator is used to provide the clock frequency to the UART Transmitter and UART Receiver. It is developed to set the 9600 baud rate.

$$\text{Count} = (\text{clock frequency}/ \text{baud rate}) * 32$$

#### 4.1.2 Simulation Result

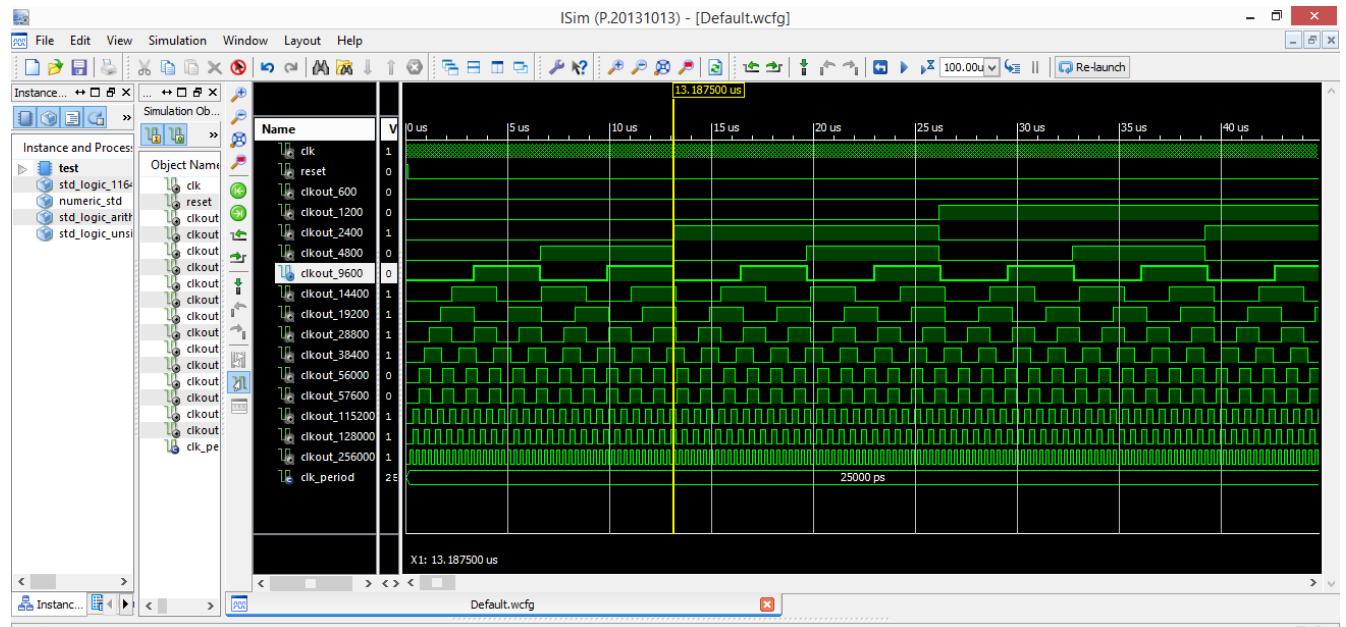


Figure No.:4.1(1) Baud-Rate Generator Simulation

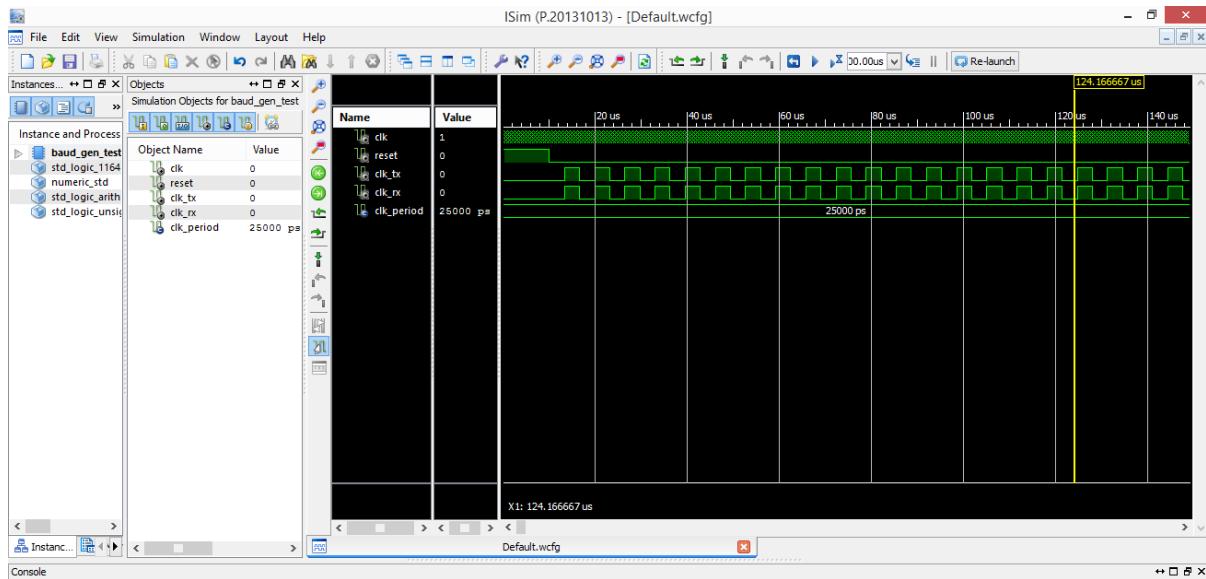


Figure No.:4.1(2) Baud-Rate Generator Simulation

## 4.2 Universal Asynchronous Receiver and Transmitter (UART)

### 4.2.1 Introduction

- Universal asynchronous receiver and transmitter (UART) is a circuit that sends parallel data through a serial line.
- UARTs are frequently used in conjunction with the EIA (Electronic Industries Alliance) RS-232 standard, which specifies the electrical, mechanical, functional, and procedural characteristics of two data communication equipment.
- Because the voltage level defined in RS-232 is different from that of FPGA I/O, a voltage converter chip is needed between a serial port and an FPGA's I/O pins.
- A UART includes a transmitter and a receiver.
- The transmitter is essentially a special shift register that loads data in parallel and then shifts it out bit by bit at a specific rate.
- The receiver, on the other hand, shifts in data bit by bit and then reassembles the data.
- The serial line is '1' when it is idle. The transmission starts with a start bit, which is '0', followed by data bits and an optional parity bit, and ends with stop bits, which are '1'.
- The number of data bits can be 6, 7, or 8. The optional parity bit is used for error detection.
- For odd parity, it is set to '0' when the data bits have an odd number of 1's.

- For even parity, it is set to '0' when the data bits have an even number of 1's. The number of stop bits can be 1, 1.5, or 2.

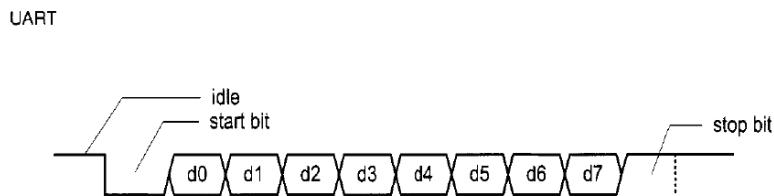


Figure No.:4.2 UART Transmission

#### 4.2.2 Symbol

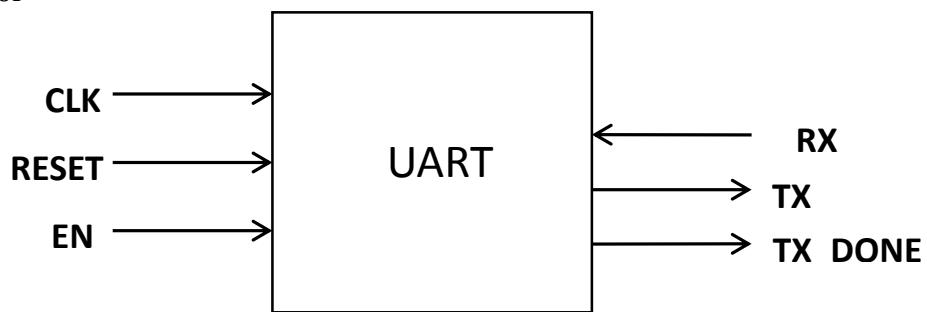


Figure No.:4.3 UART Symbol

#### 4.2.3 Port I/O Description

Name	Direction	Description
Clk	Input	System clock
en	Input	System clock enable
Reset	Input	Asynchronous reset
RX	Input	Serial data in
TX	Output	Serial data out
TX_DONE	Output	Transmission complete pulse

Table No.:4.1 UART I/O Description

#### 4.2.4 Modules Hierarchy

The UART hierarchy is as shown below. The top module is UART. UART module has three sub-modules: 1) baud\_gen 2) uart\_rx 3) uart\_tx.

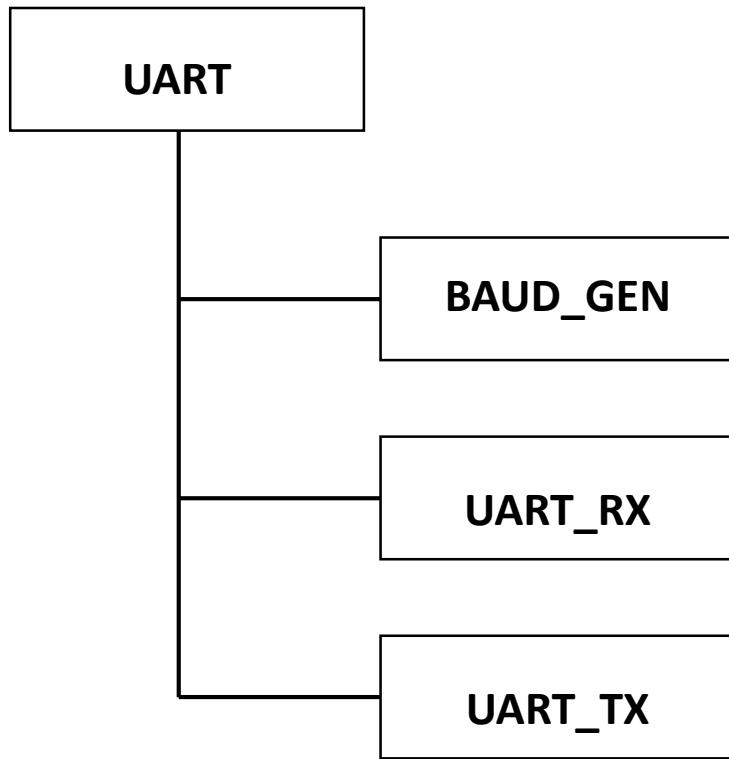


Figure No.:4.5 UART Modules Hierarchy

#### 4.2.5 Detail Description

The block diagram of the Universal Asynchronous Receiver Transmitter (UART) is as shown in the figure below. There is a baud rate generator module and two sub-modules: uart\_rx and uart\_tx which are instantiated in a UART. Baud rate generator module produces separate clock for uart\_tx module and uart\_rx module. Uart\_rx module requires clock (clk\_rx), serial input (rx) and enable bit (en). Uart\_tx module requires clock (clk\_tx), 8-bit parallel input (din), enable bit (en) and tx\_start. There is an 8-bit buffer register which holds data values for uart\_rx module and uart\_tx module. Uart\_rx converts the serial input (rx) into 8-bit parallel data (dout). The completion of the conversion process is indicated by rx\_done pulse. The 8-bit parallel output of uart\_rx module is given to uart\_tx as input (din), controlled by rx\_done pulse. The uart\_tx module provides serial data output (tx). Tx\_done pulse indicates completion of the process.

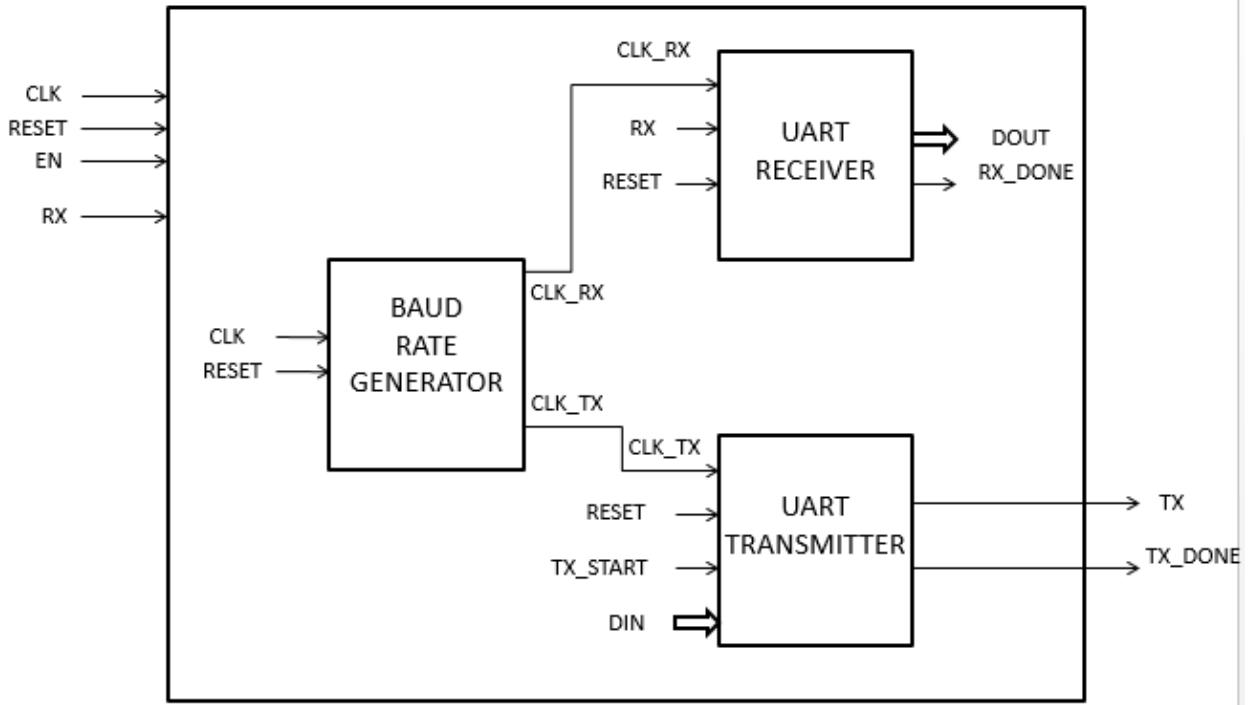


Figure No.:4.6 UART Block Diagram

#### 4.2.6 UART Receiver

##### 4.2.6.1 Detail description

- UART Receiver is module which accepts serial data input and converts into 8-bit parallel data output.
- The UART Receiver uses oversampling for locating middle position of the transmitted bits. The oversampling rate used in UART Receiver is 16 times the baud rate.
- UART Receiver is implemented as a Finite State Machine with four states (idle, start, data, stop) as shown in the figure below.
- On reset FSM is on idle state and if it receives zero bit ( $Rx = 0$ ), it jumps to start state. On start state, counter register ( $cnt\_reg$ ) is enabled and it jumps to data state when counter register reaches 7 ( $cnt\_reg = 7$ ) and reset the counter register.
- On data state, each transmitted data bit is shifted into buffer register when counter register reaches 15 ( $cnt\_reg = 15$ ) and counter register is reset ( $cnt\_reg = 0$ ).
- When received register ( $R\_BITS\_REG$ ) equals to data width, it jumps to stop state, else received register is incremented.
- On stop state, when counter register reaches 15 ( $cnt\_reg = 15$ ), rx\_done pulse indicates completion of conversion.

#### 4.2.6.2 Flowchart

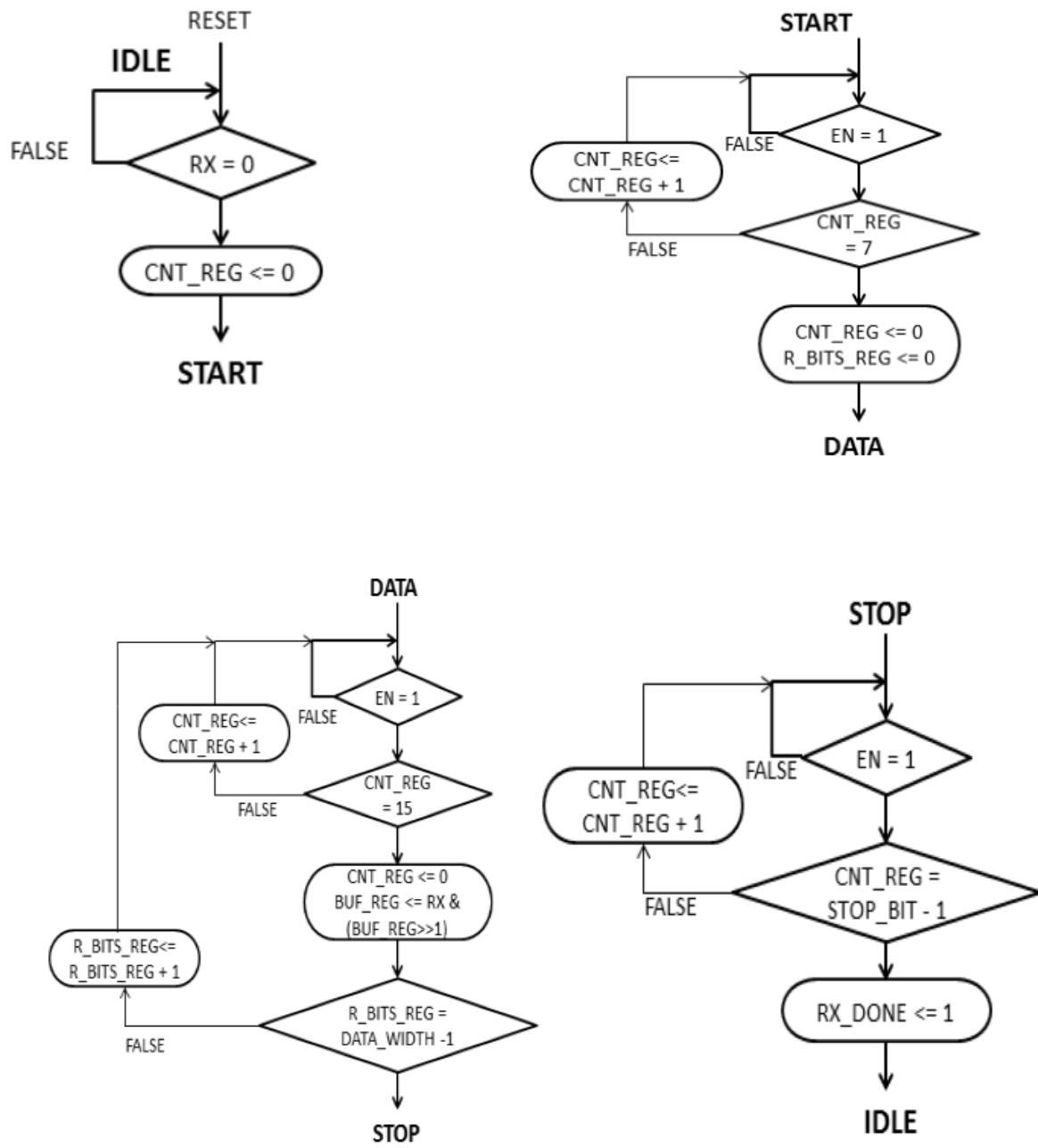


Figure No.:4.7 UART Receiver Flowchart

#### 4.2.6.3 Finite State Machine

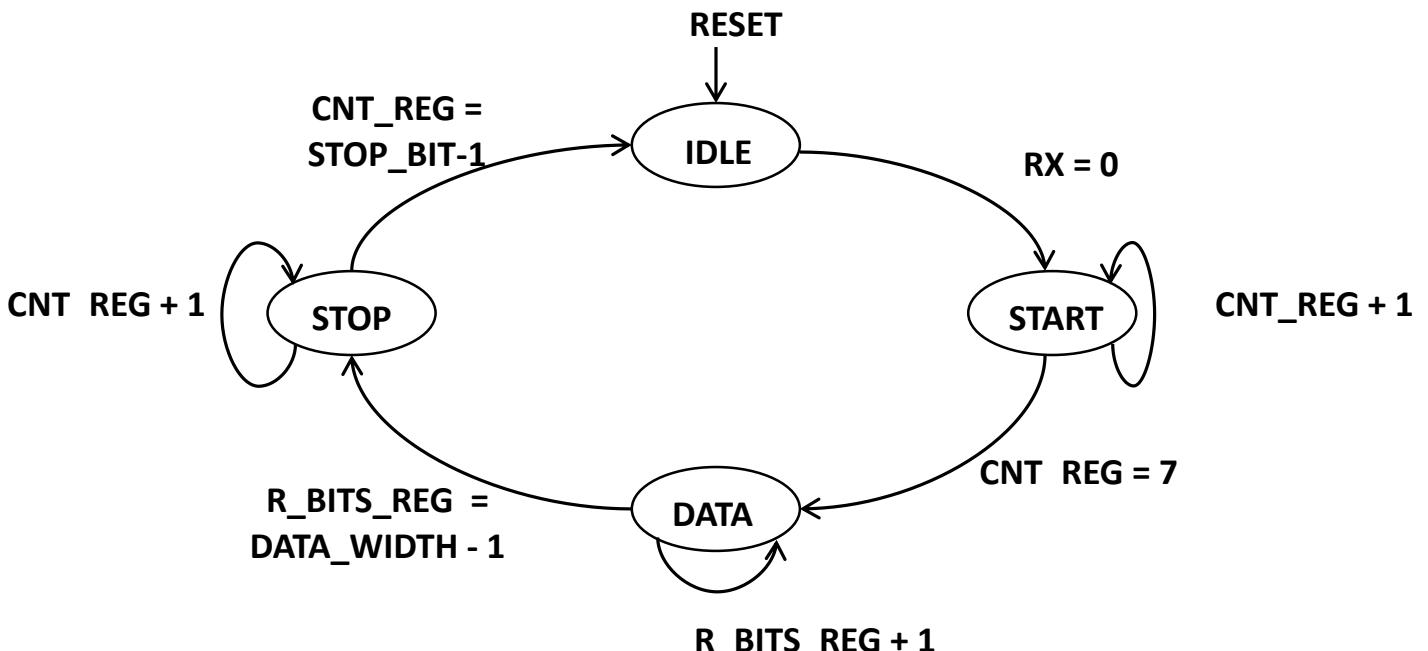


Figure No.: 4.8 UART Receiver FSM

#### 4.2.6.4 Simulation Result

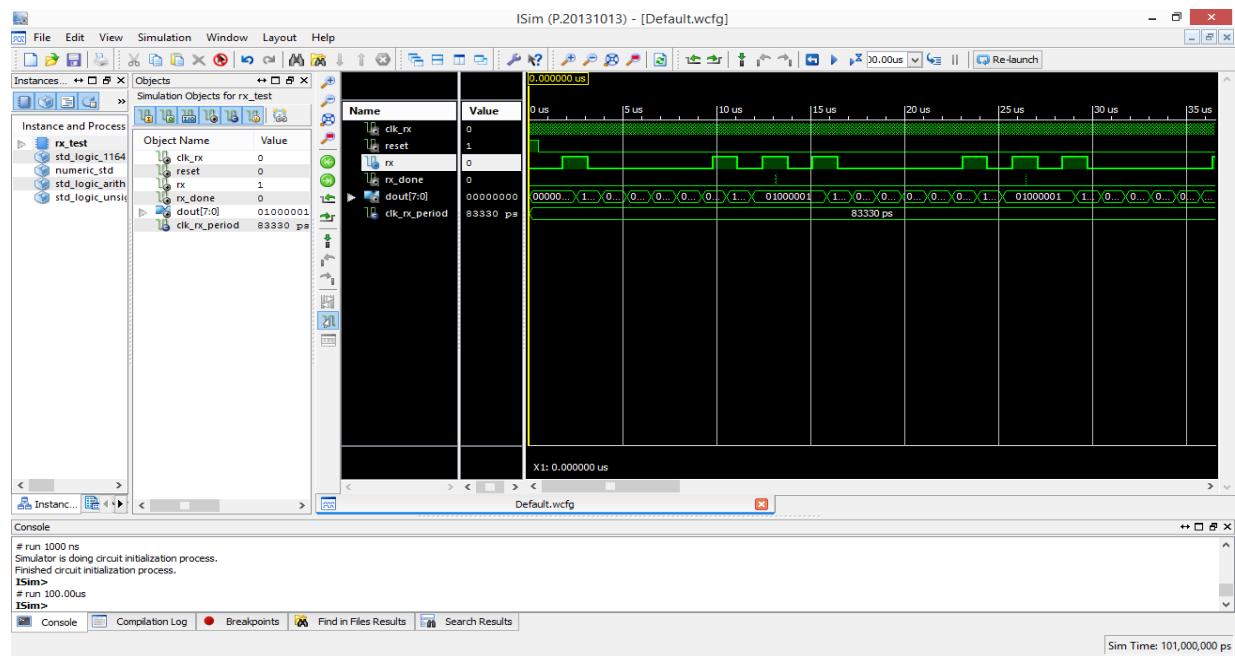


Figure No.:4.9(1) UART Receiver Simulation Result

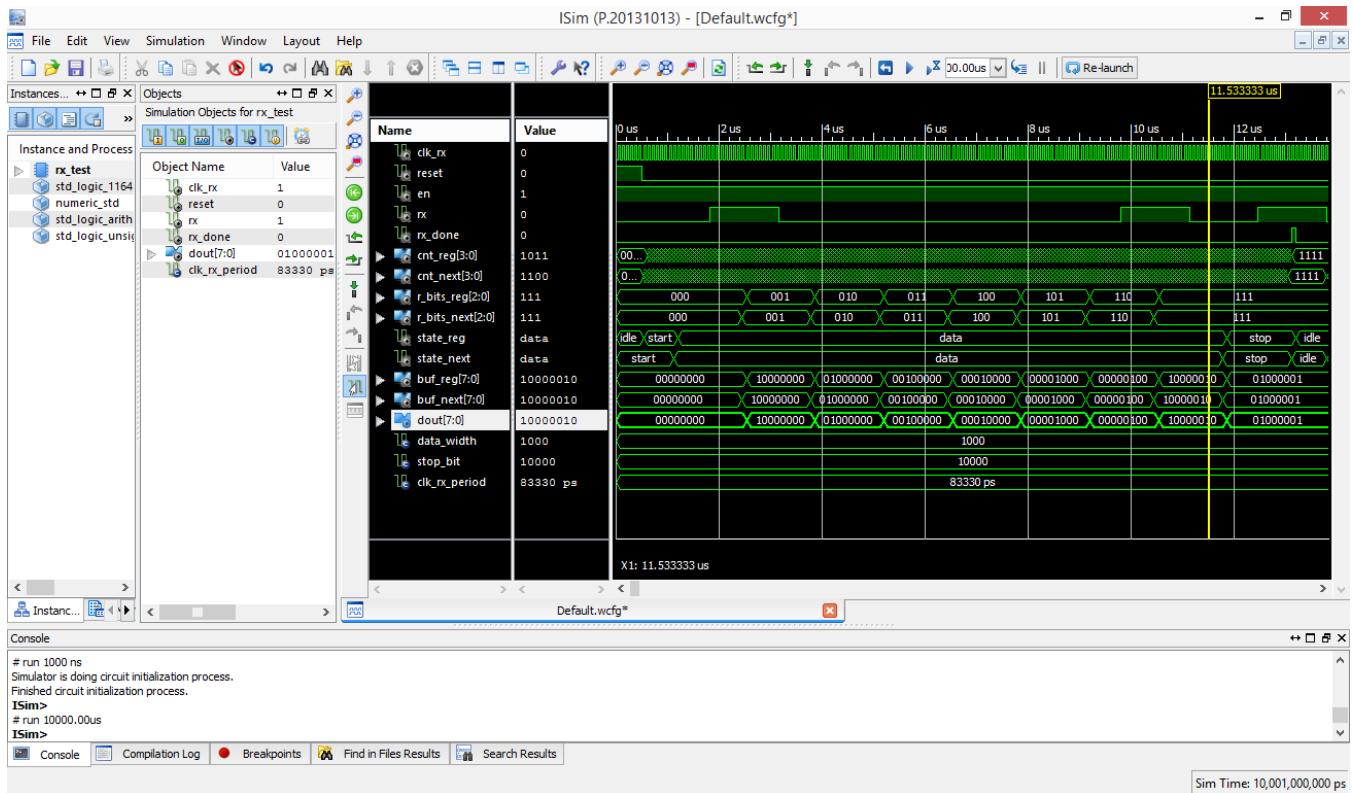


Figure No.:4.9(2) UART Receiver Simulation Result

## 4.2.7 UART Transmitter

### 4.2.7.1 Detail description

- UART Transmitter is module which accepts 8-bit parallel data input and provides serial data output. The UART Transmitter uses no oversampling so the frequency is 16 times slower than UART Receiver using internal counter.
- UART Transmitter is implemented as a Finite State Machine with four states (idle, start, data, stop) as shown in the figure below.
- On reset FSM is on idle state and if tx\_start is enabled, it jumps to start state.
- On start state, counter register (cnt\_reg) is enabled and it jumps to data state when counter register reaches 15 (cnt\_reg = 15) and reset the counter register.
- On data state, received data bits is shifted into buffer register when counter register reaches 15 (cnt\_reg = 15) and counter register is reset (cnt\_reg = 0). When received register (R\_BITS\_REG) equals to data width, it jumps to stop state, else received register is incremented.

- On stop state, when counter register reaches 15 ( $\text{cnt\_reg} = 15$ ),  $\text{tx\_done}$  pulse indicates completion of conversion.

#### 4.2.7.2 Flowchart

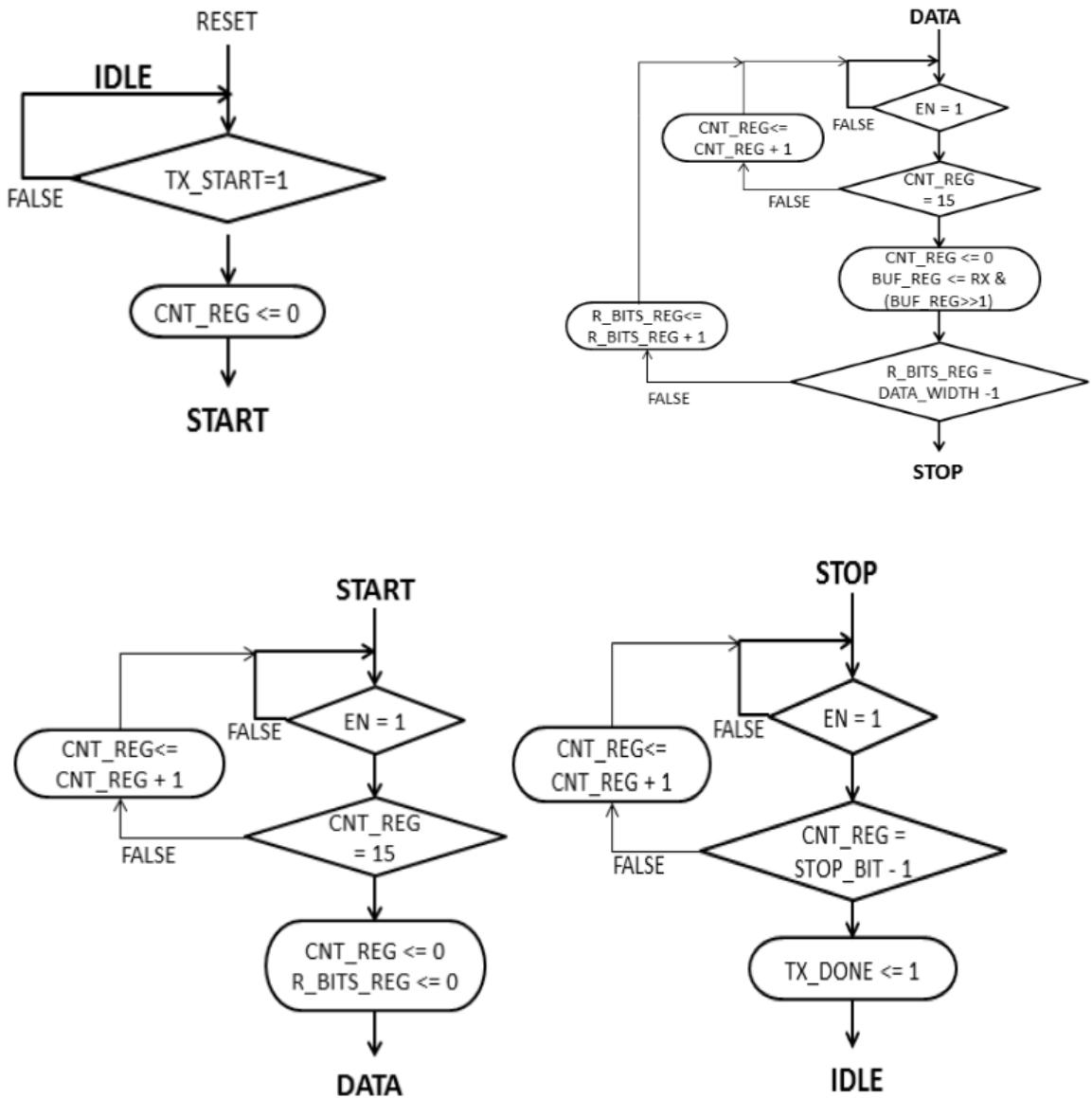


Figure No.:4.10 UART Transmitter Flowchart

#### 4.2.7.3 Finite State Machine

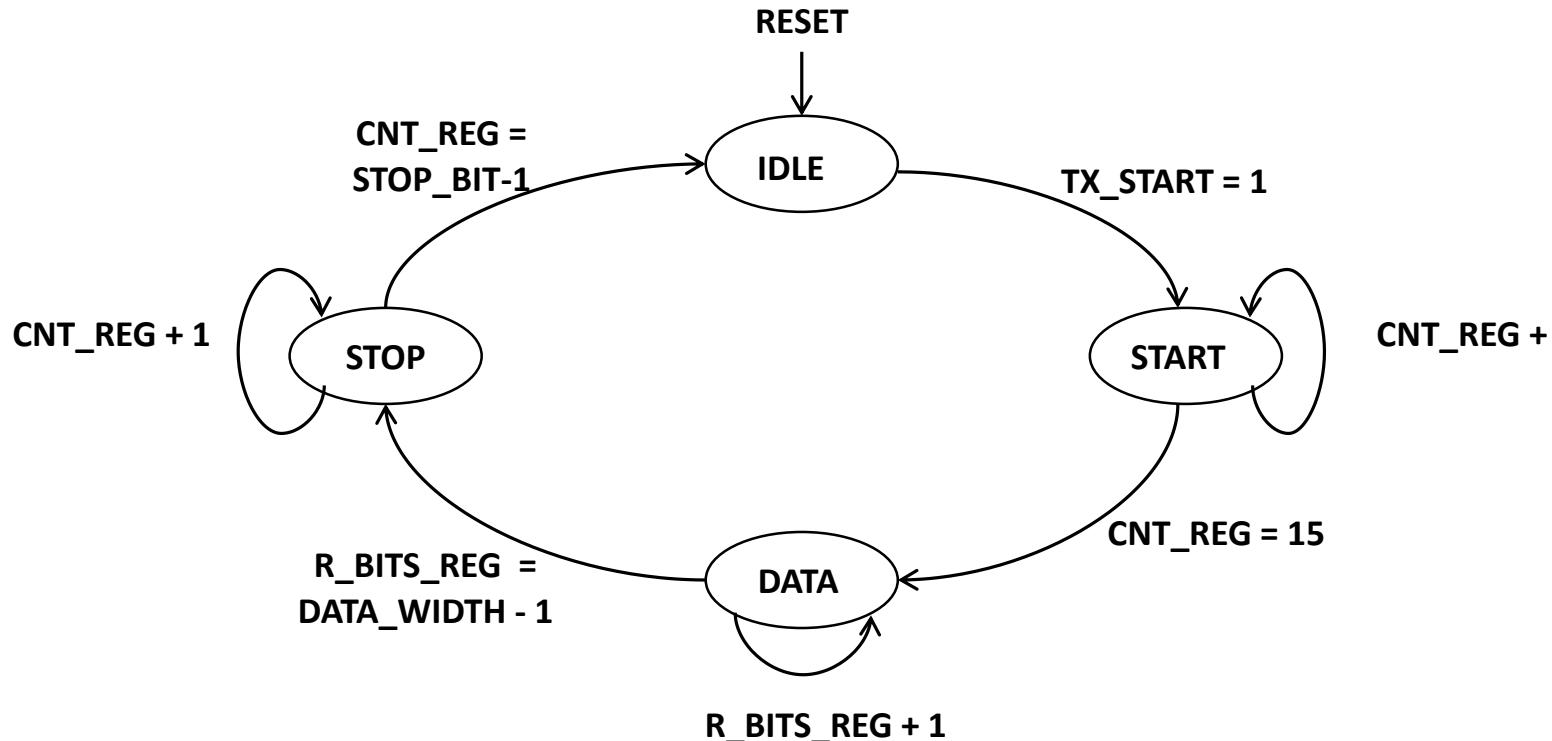


Figure No.:4.11 UART Transmitter FSM

#### 4.2.7.4 Simulation Result

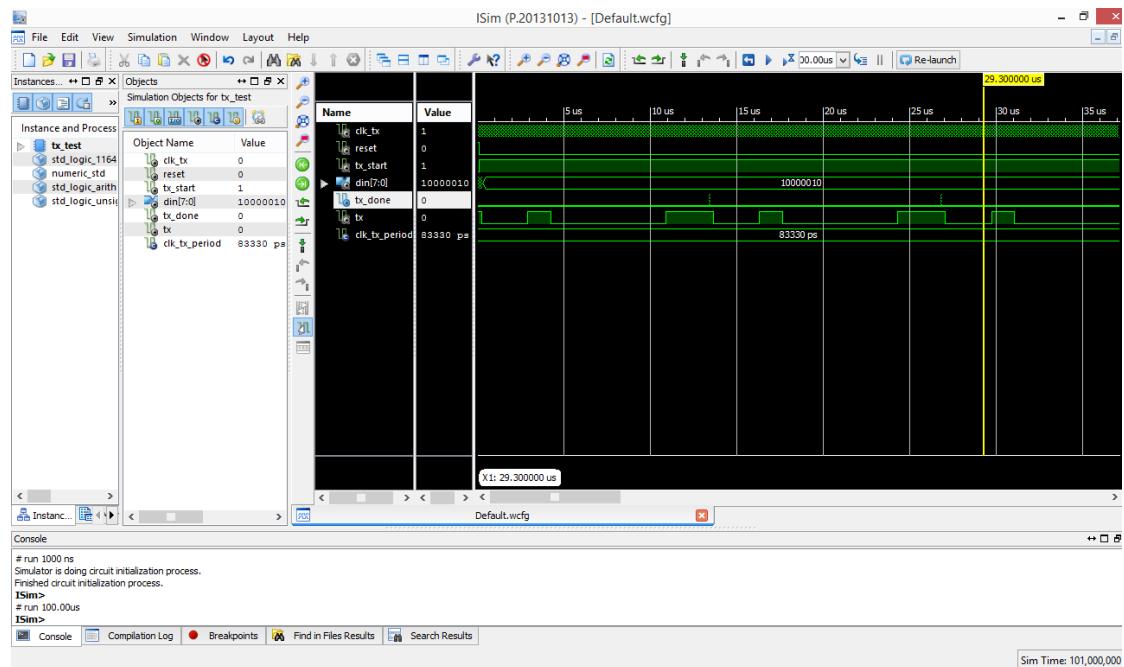


Figure No.:4.12(1) UART Transmitter Simulation Result

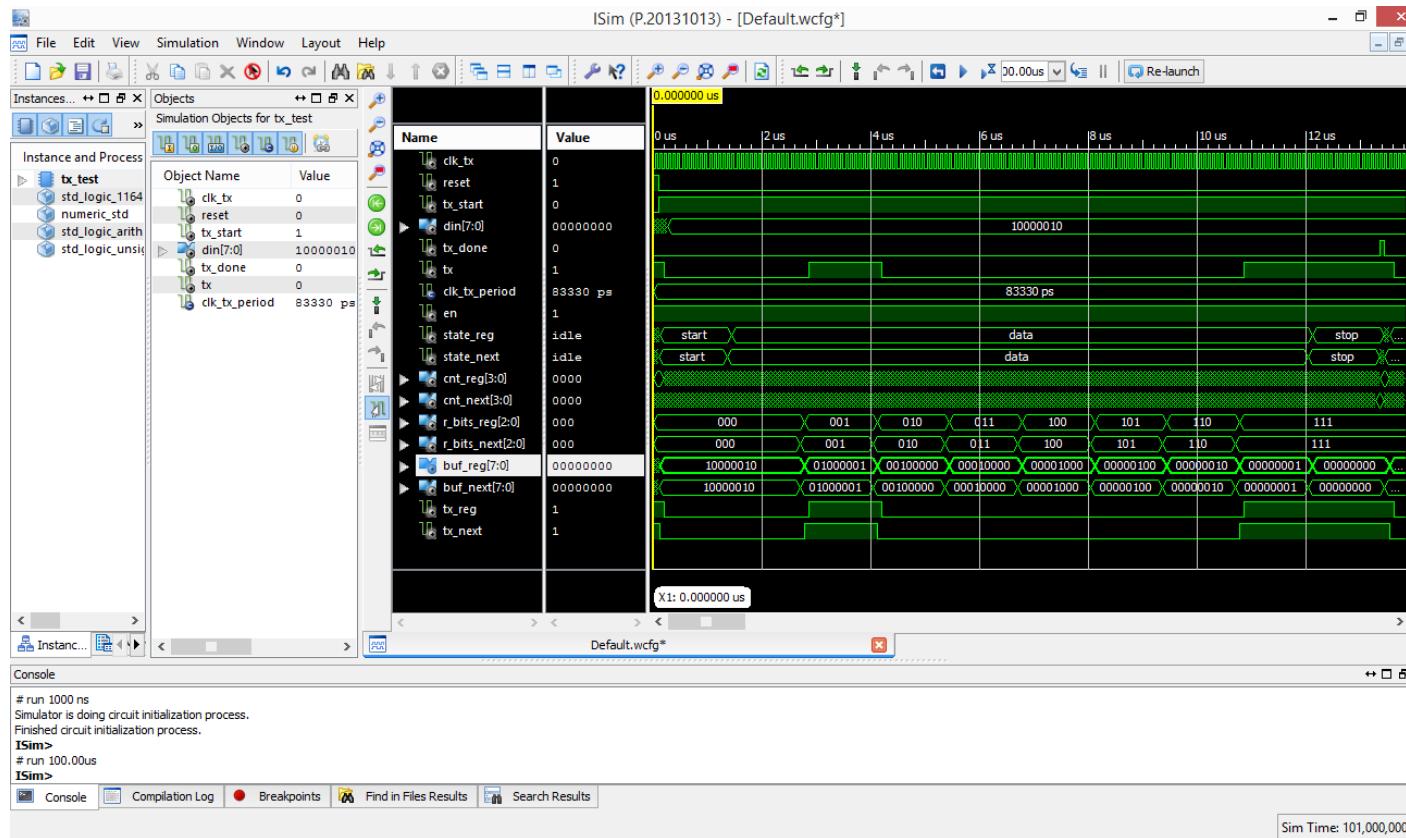


Figure No.:4.12(2) UART Transmitter Simulation Result

#### 4.2.8 UART Simulation Result

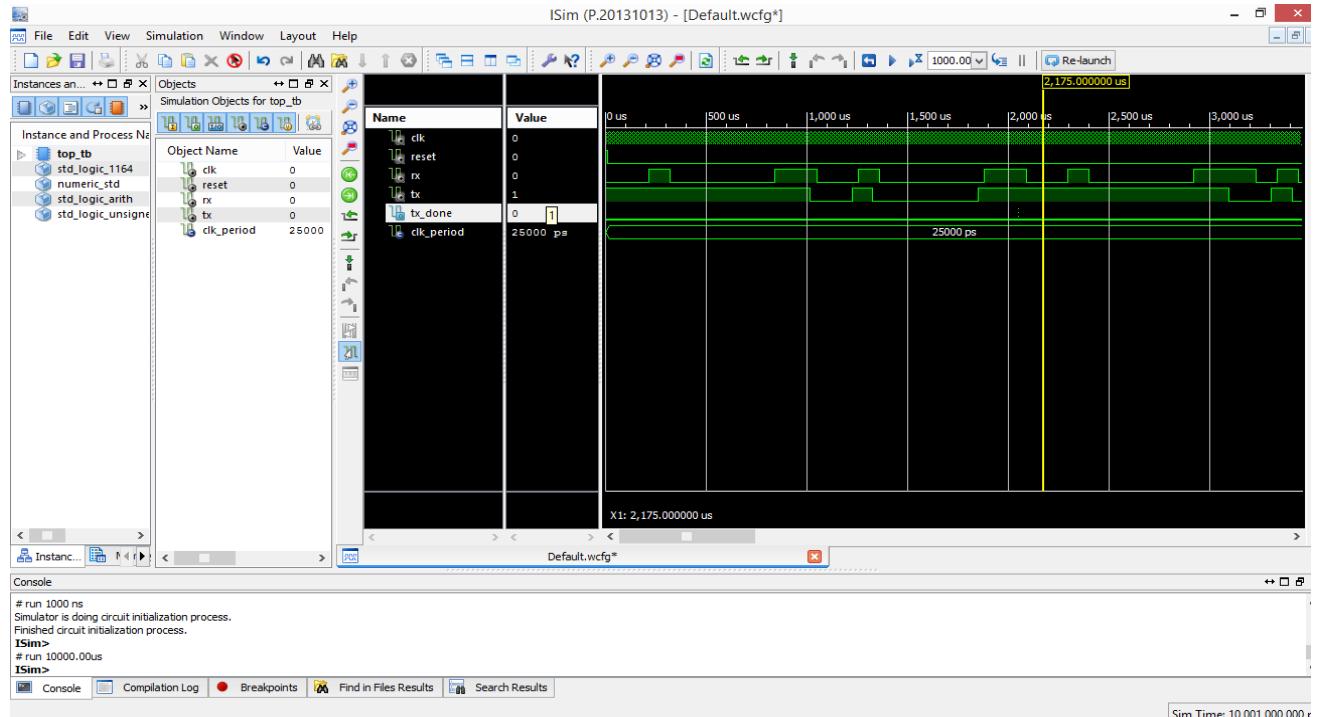


Figure No.:4.13(1) UART Simulation Result

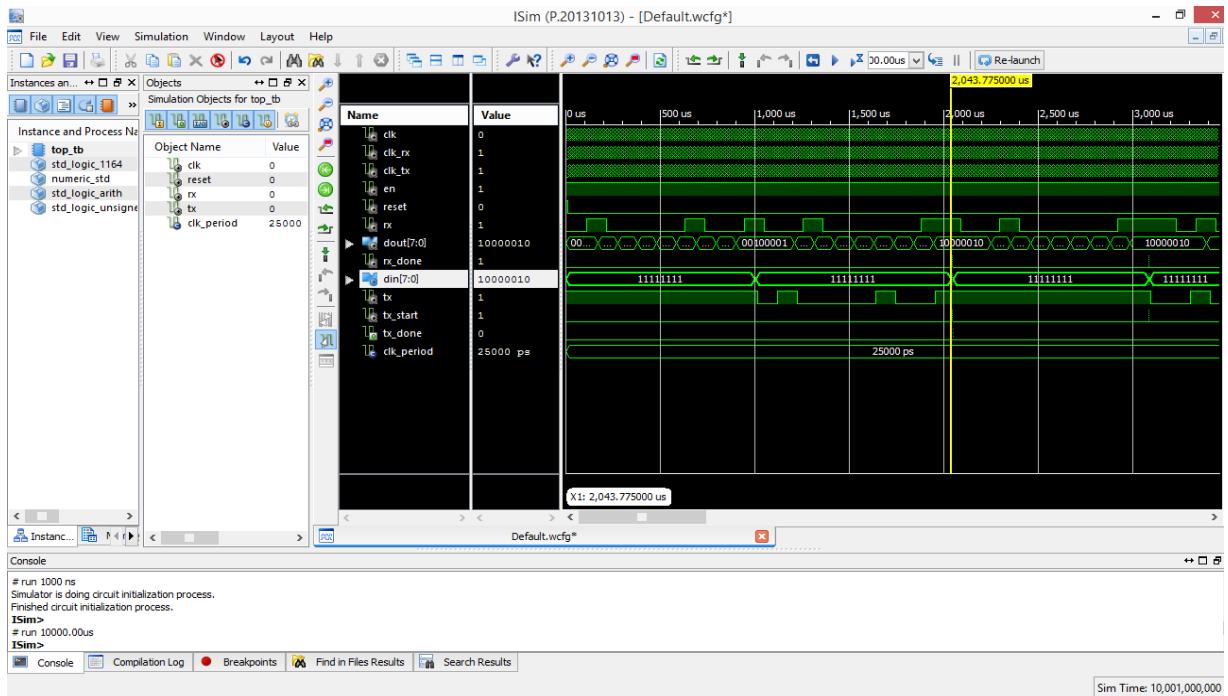


Figure No.:4.13(2) UART Simulation Result

#### 4.2.9 UART Test Setup

- The board is supplied with +12 V supply using Lambda source
- The oscillator is set to measure the input to UART Receiver and terminal output.
- The JTAG programmer is connected to the board and Pc as shown in the figure.
- The RS-232 male connector of board is connected to the Rs-232 female connector of module.
- The baud rate is set to 9600 by setting appropriate transmitter clock.

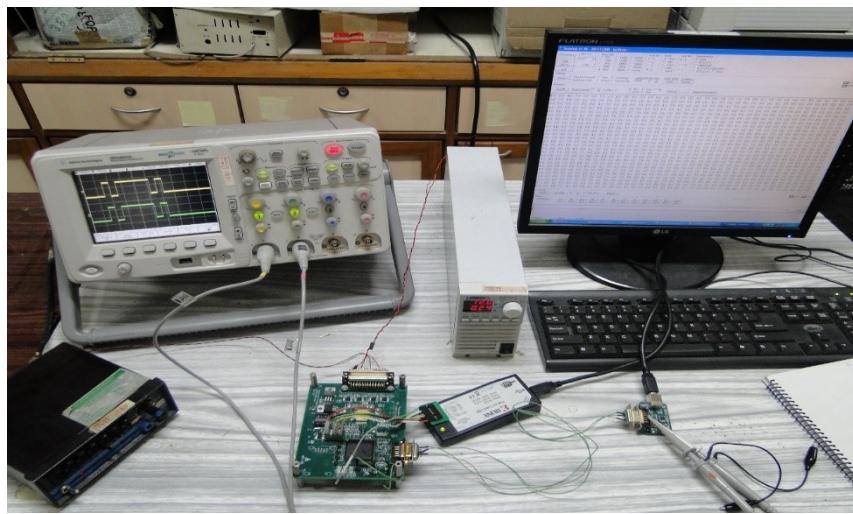


Figure No.:4.14 UART Simulation Result

#### 4.2.10 UART Terminal Result

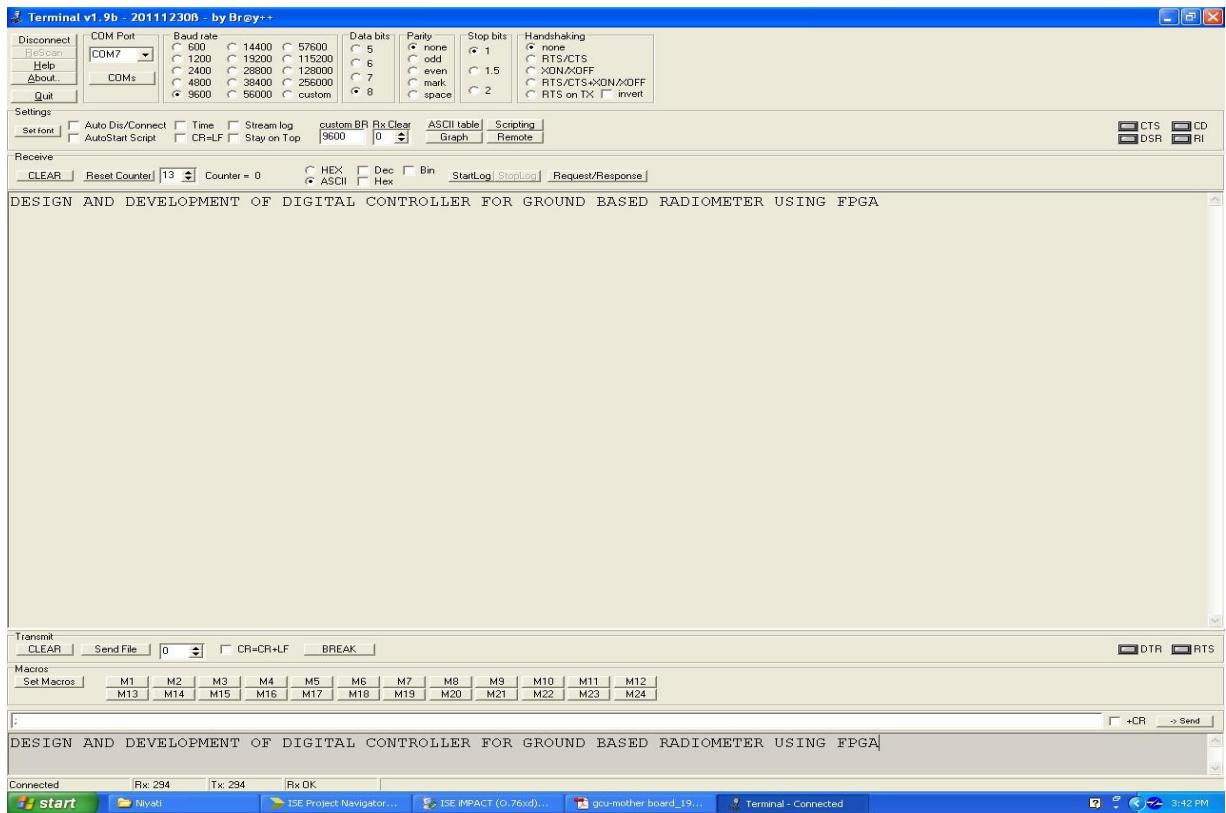


Figure No.:4.15 UART Terminal Result

### 4.3 Frame-Sync Interface

#### 4.3.1 Description

- Frame-Sync format is similar to the interface often used on audio ADCs.
- It operates in slave fashion—the user must supply framing signal FSYNC (similar to the left/right clock on stereo audio ADCs) and the serial clock SCLK (similar to the bit clock on audio ADCs).
- The data are output MSB first or left-justified on the rising edge of FSYNC. When using Frame-Sync format, the FSYNC and SCLK inputs must be continuously running with the relationships shown in the following figure.

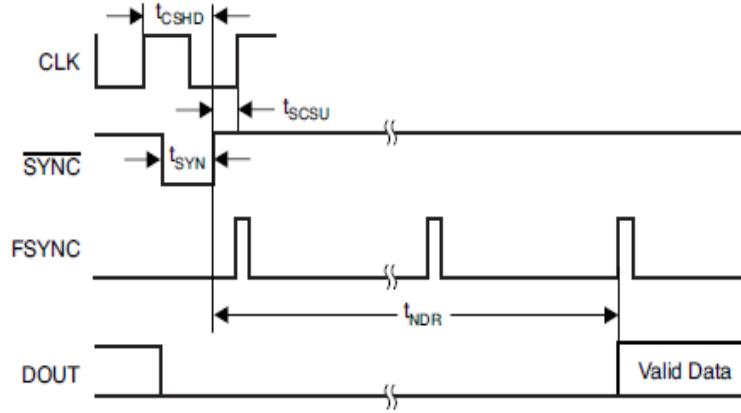


Figure No.:4.16 Frame-Sync Protocol

#### 4.3.2 Timing Specifications

- The frame-sync input (FSYNC) sets the frame period, which must be the same as the data rate. The required number of FCLK cycles to each FSYNC period depends on the mode selection
- The number of SCLKs within a frame period (FSYNC clock) can be any power-of-2 ratio of CLK cycles (1, 1/2, 1/4, etc), as long as the number of cycles is sufficient to shift the data output from all channels within one frame.

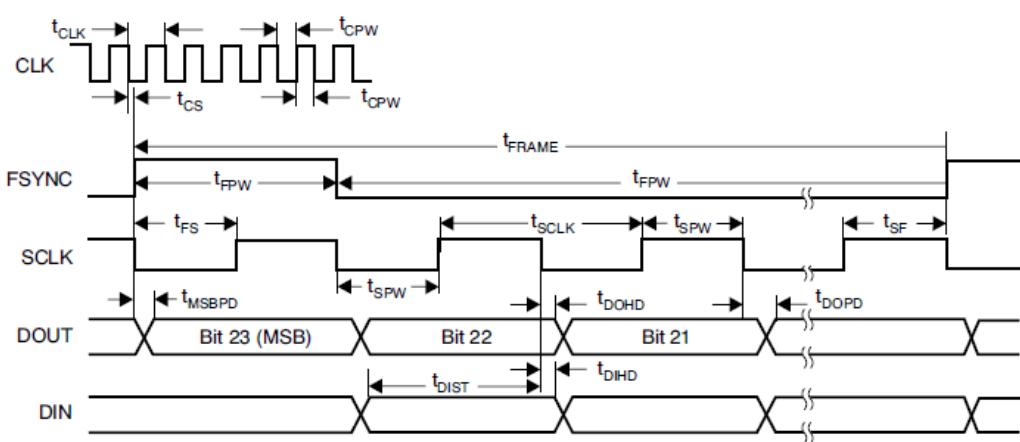


Figure No.:4.17 Frame-Sync Format Timing

### 4.3.3 Pin Assignments

- Here ADS1278 would be working on Low-power mode and we would use frame sync interface for extracting data.
- The ADS1278 requires following input signals to operate successfully.
  - Low-Power mode:
    - ADC\_clk – 13.5 MHz
    - Sclk – 13.5 MHz
    - Mode0 -‘0’
    - Mode1 -‘1’
  - Frame-Sync format (Discrete Data Output):
    - Format0 -‘1’
    - Format1 -‘0’
    - Format2 -‘1’
  - Single device operation:
    - Din -‘0’
  - Synchronization:
    - Sync -‘1’
  - Normal operation:
    - Test0 -‘0’
    - Test1 -‘0’

## 4.3.4 Simulation Result

### 4.3.4.1 Single Channel

- Output with check bytes

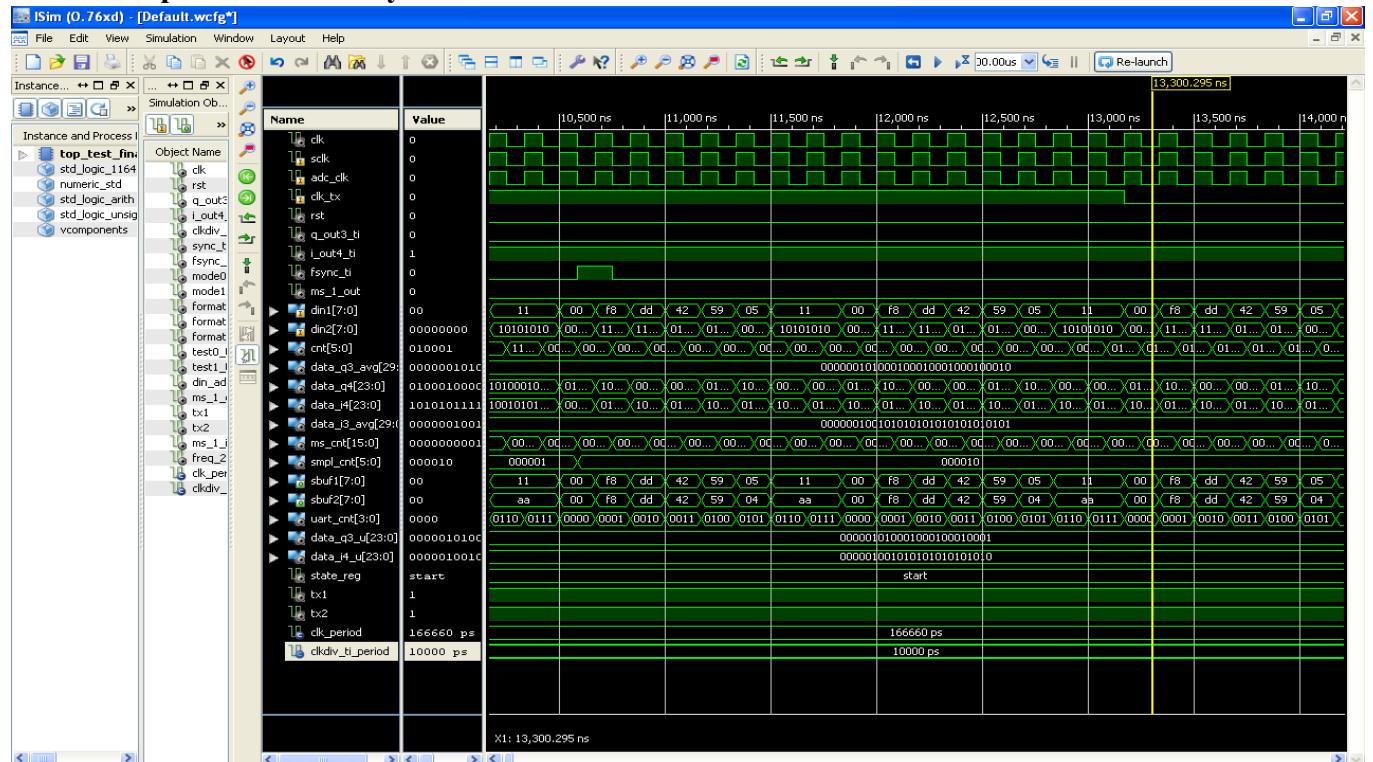


Figure No.4.18(1) Simulation- Single channel with check bytes

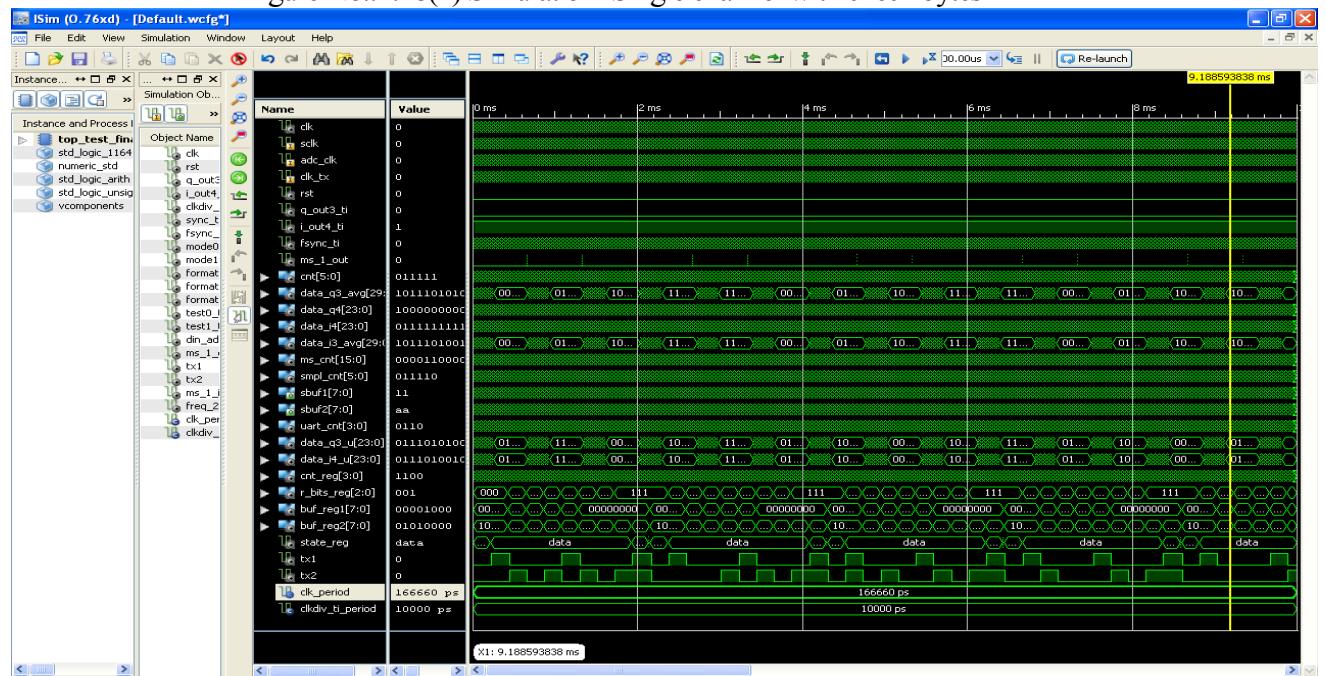


Figure No.:4.18(2) Simulation- Single channel with check bytes

- Output without check bytes

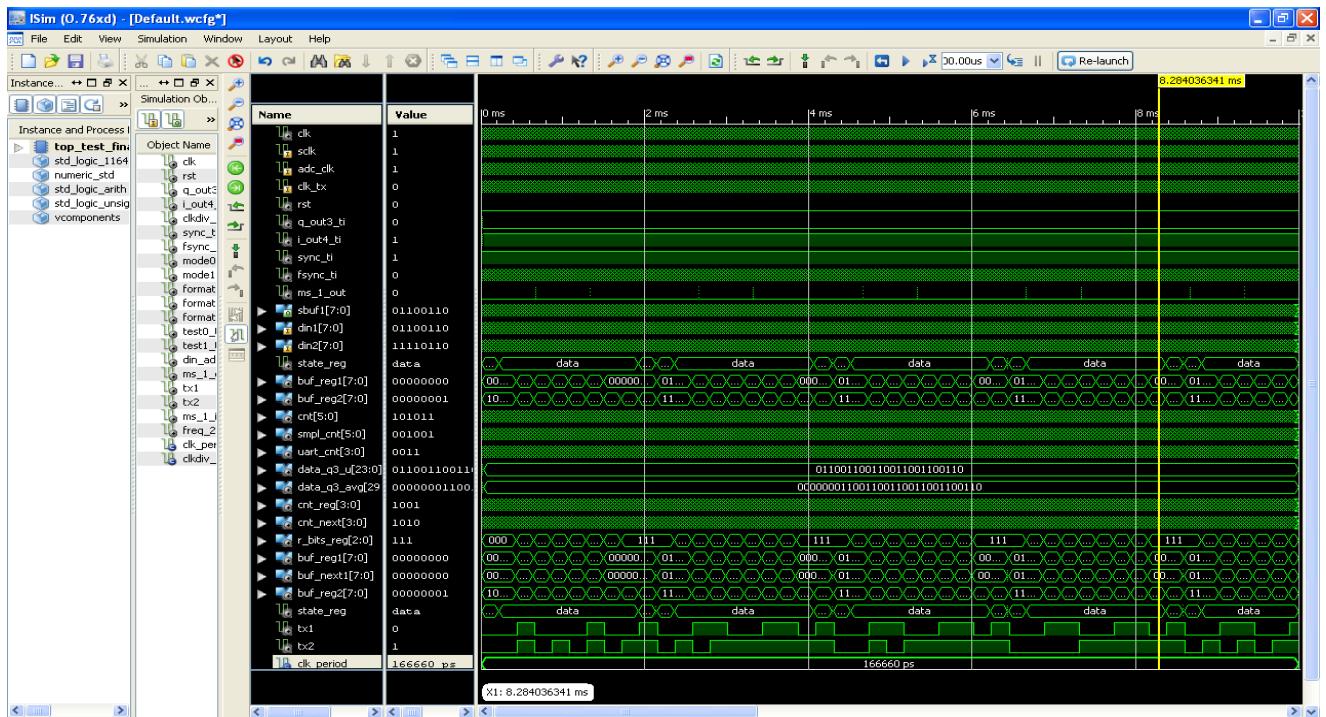


Figure No.:4.19(1) Simulation- Single channel without check bytes

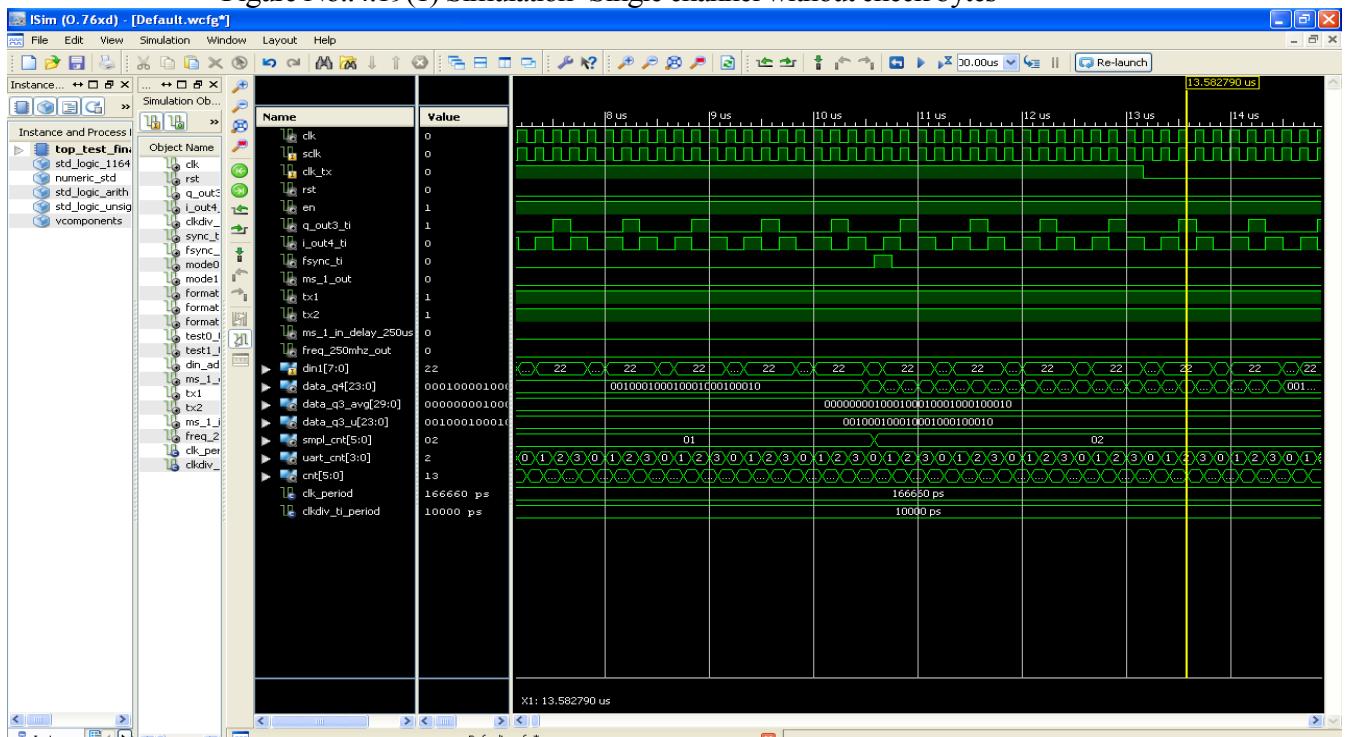


Figure No.:4.19(2) Simulation- Single channel without check bytes

#### 4.3.4.2 Multiple Channels

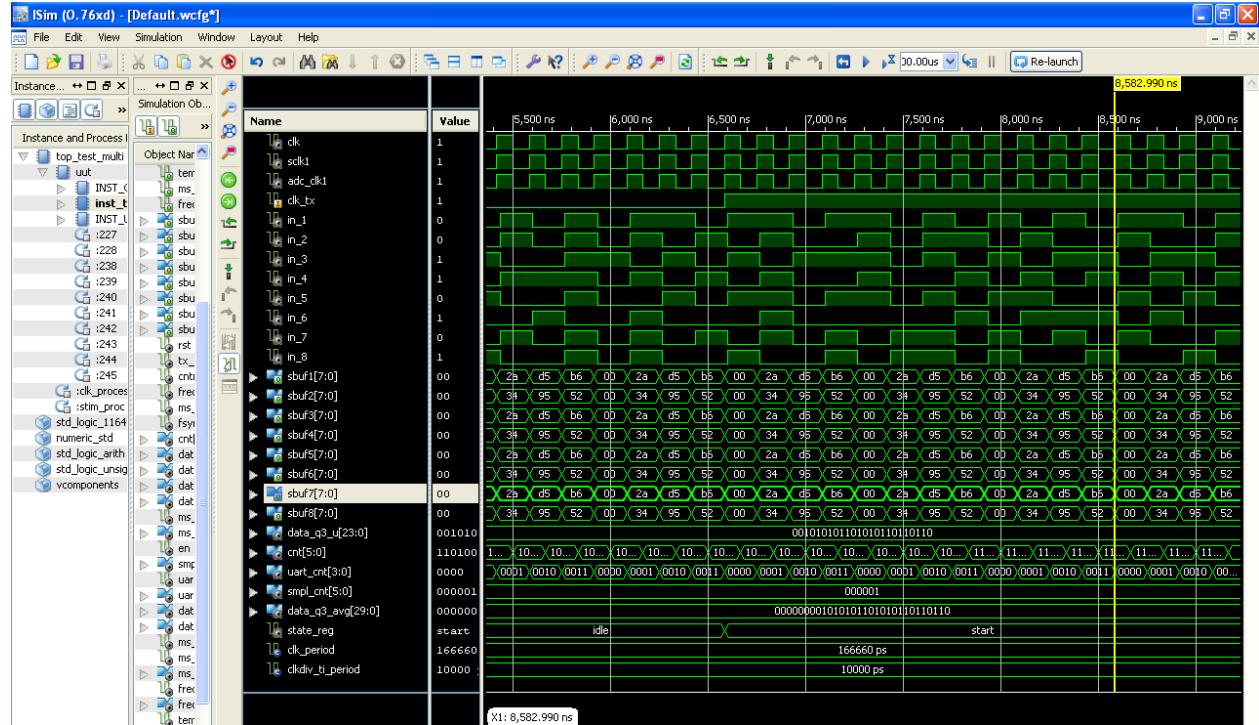


Figure No.:4.20(1) Simulation Result – Multiple Channels

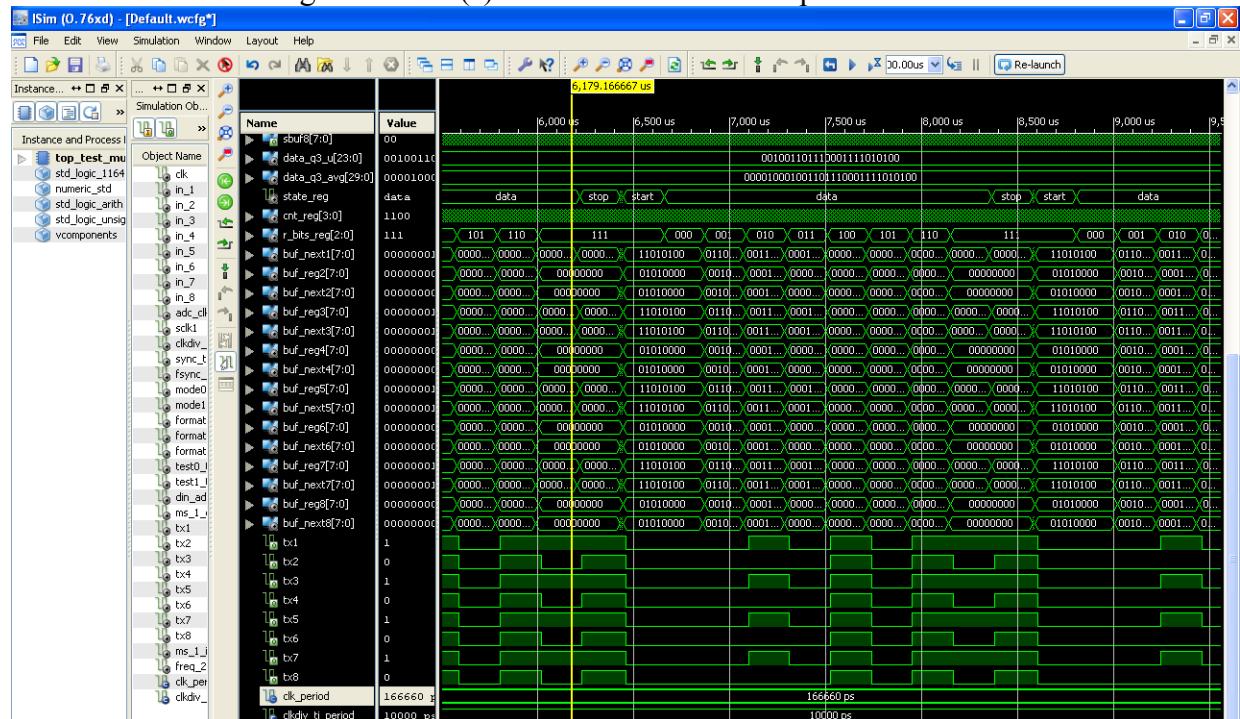
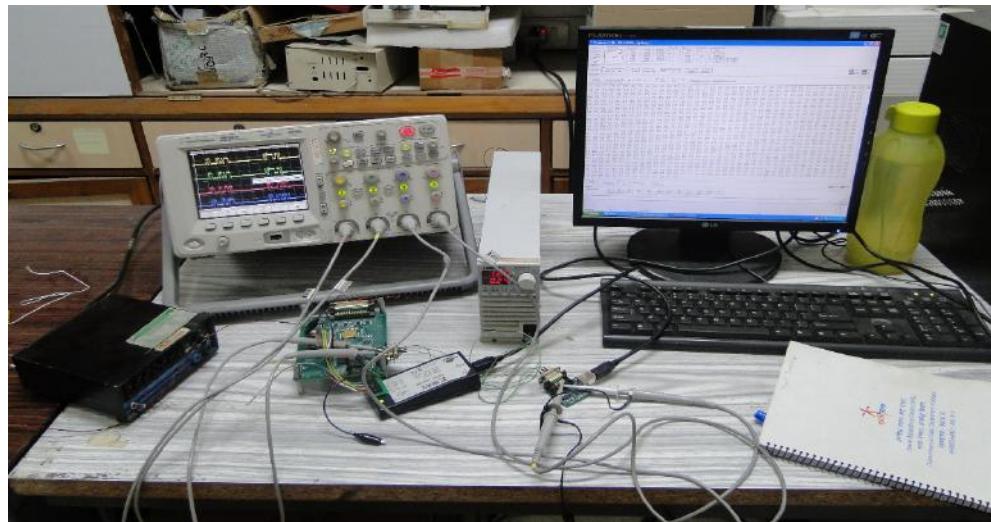


Figure No.:4.20(2) Simulation – Multiple Channels

## 5. Implementation

### 5.1 Test Setup

- The board is supplied with +12 V supply using Lamda source
- The ADC is supplied with variable analog supply using DC source.
- The oscillator is set to measure the terminal output for multiple channels.
- The JTAG programmer is connected to the board and Pc as shown in the figure.
- The RS-232 male connector of board is connected to the Rs-232 female connector of module.
- The baud rate is set to 9600 by setting appropriate transmitter clock.



### 5.2 Output theoretical Calculation

$$\text{Step Width} = \text{Max voltage} / (2^n)$$

$$\text{Step width} = 5 \text{ V} / (2^{24}) = 0.298 \text{ uV}.$$

$$\frac{\text{Resolution of the ADC}}{\text{System Voltage}} = \frac{\text{ADC Reading}}{\text{Analog Voltage Measured}}$$

For Vin = 4 V

$$\text{ADC Reading} = 4 \text{ V} / 0.298 \text{ uV} = \text{Hex-CCD0E2 (13422818.79)}$$

### Practical Result

For Vin (Analog Supply Voltage) = 4 V

Voltage measured at ADC input pin = 3.99092 V

$$\text{ADC Reading} = 3.99092 \text{ V} / 0.298 \text{ uV} = \text{Hex-CC59DD (13392349.69)}$$

## 5.3 Terminal Output

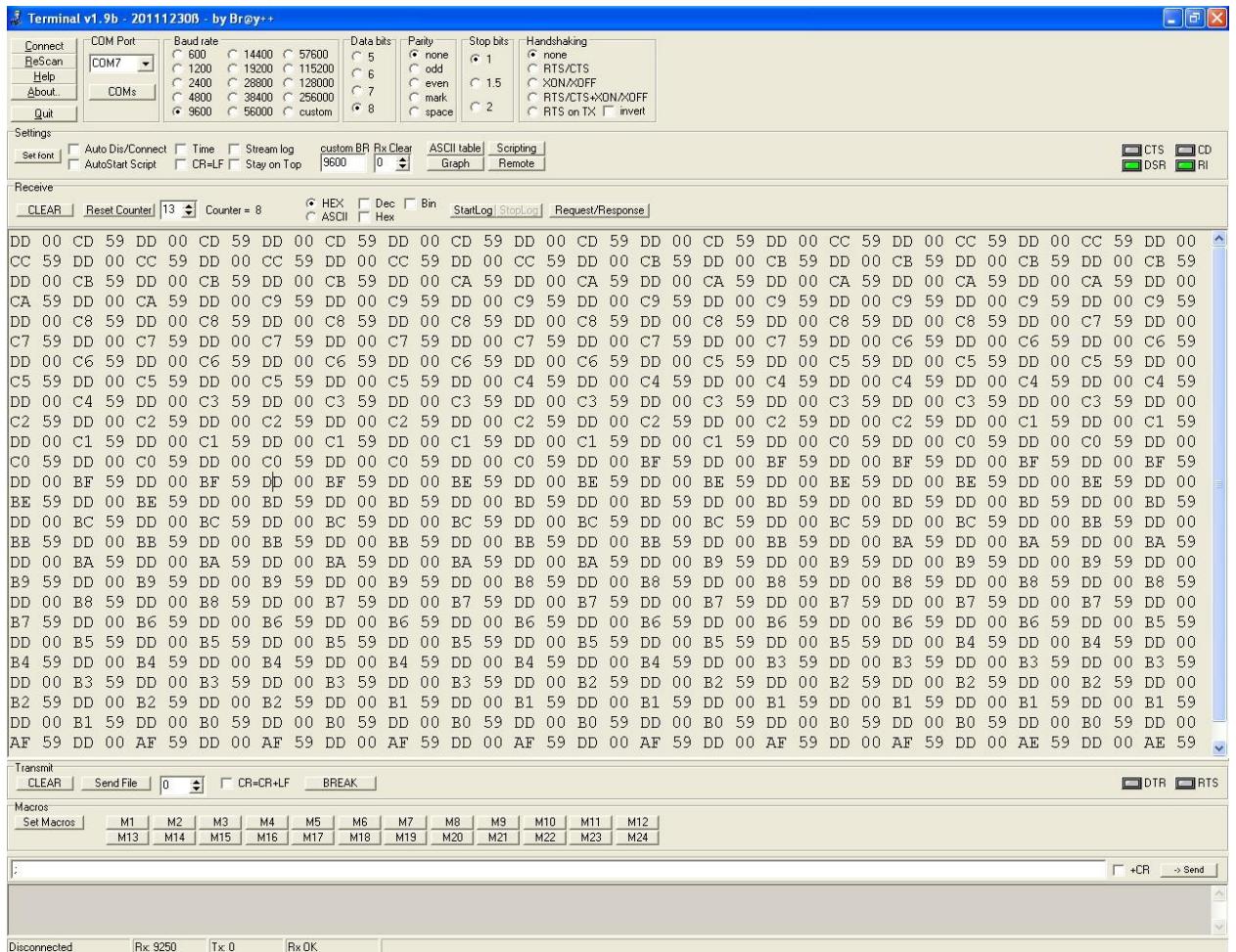


Figure No.: 5.3 Single Channel Terminal Output

## **Chapter 6**

### **Conclusions and Future Work**

#### **6.1 Conclusions**

The UART general module has been prepared and tested for different baud-rates. Analog signal given as input to ADS1278 are converted to digital format. This data is extracted by Field Programmable Gate Array (FPGA) and transmitted to PC through RS-232 interface. The digital output corresponding to analog input is obtained at terminal software.

#### **6.2 Future Work**

Characterization of Delta-sigma Analog to Digital Converter (ADC) is to be performed to obtain AC and DC characteristics of ADC and to verify the results obtained at terminal output.

## **References**

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- [www.xilinx.com](http://www.xilinx.com)
- [www.ti.com](http://www.ti.com)