MMIC Chip Design

Microwave Design and Measurements (EERF 6396)
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Submitted By

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1. Introduction

A. What did you do?

- Design A: Ideal Butterworth high-pass lumped element filter at cut off frequency 10 GHz.
- Design B: MMIC Butterworth high-pass on GaAs at cut off frequency 10 GHz.

2. Design and Simulations

Design A: Ideal Butterworth high-pass lumped element filter

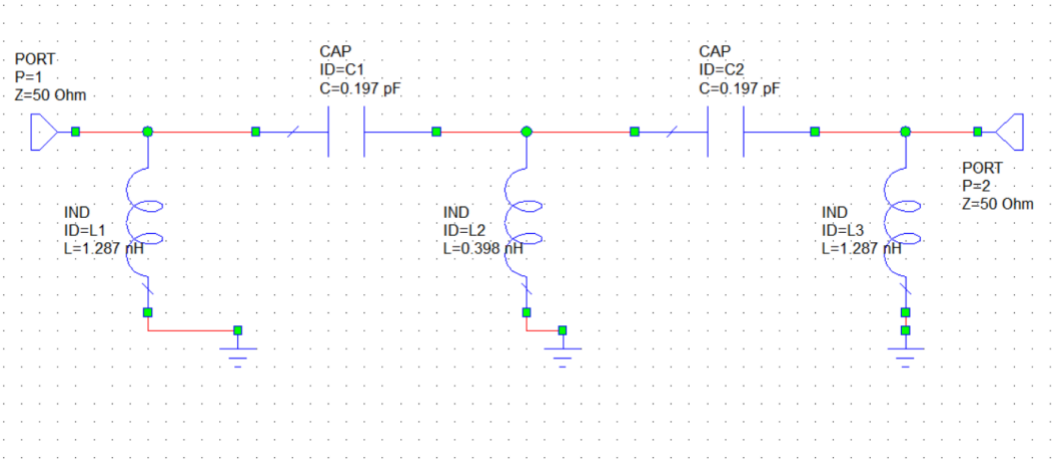
Parameter	Design Goal
f_C (GHz)	10.0
Rejection at 5GHz (dB)	≥30
No. of elements (N, odd)	Minimum
Pi topology	
Z_G and Z_L = 50Ω	

- Number of elements required was found to be 5 from the graph (normalized frequency vs. attenuation) to get minimum 30 dB attenuation at 5 GHz, where cut off frequency is 10 GHz.
- The value of inductances and capacitances were calculated from the below equations:

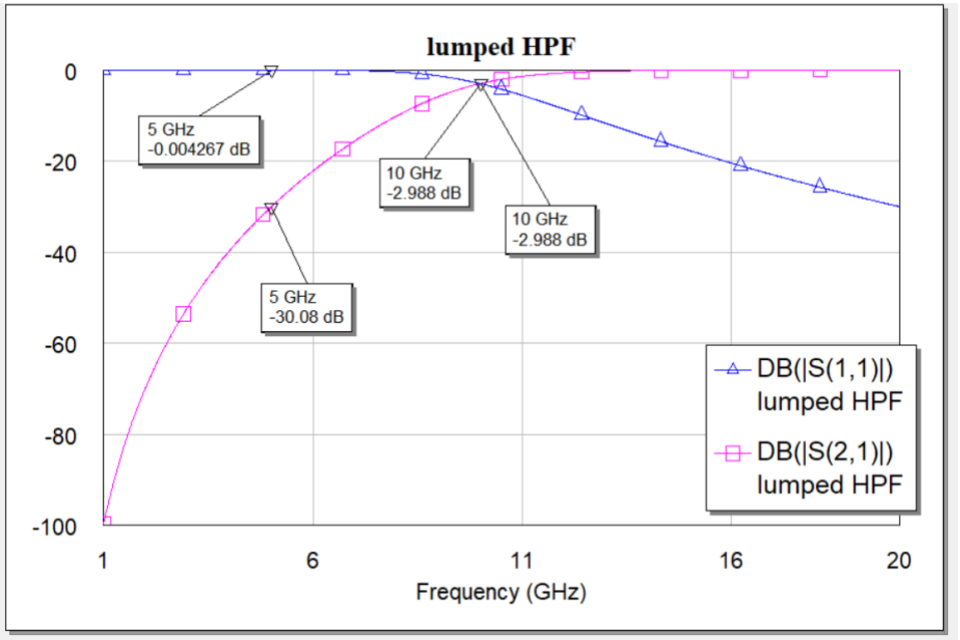
$$L = \frac{R}{2 * pi * Gn * Fc}$$

$$C = \frac{1}{2 * pi * Fc * Gn * R}$$

1. Circuit schematic with component values:



2. MWO simulation for S11 and S21 (in dB) over a frequency range 1-20GHz



3. Compliance Matrix

Parameter	Design Goal	MWO Simulation Performance	Compliant (Yes/No)
Cut-off frequency (f_c)(GHz)	10 GHz	10 GHz	Yes
Rejection @ 5 GHz GHz (dB) Ideal	>= 30 dB	30.08	Yes
No. of elements (N, odd)	Minimum	5	Yes

Design B: MMIC Butterworth high-pass filter on GaAs

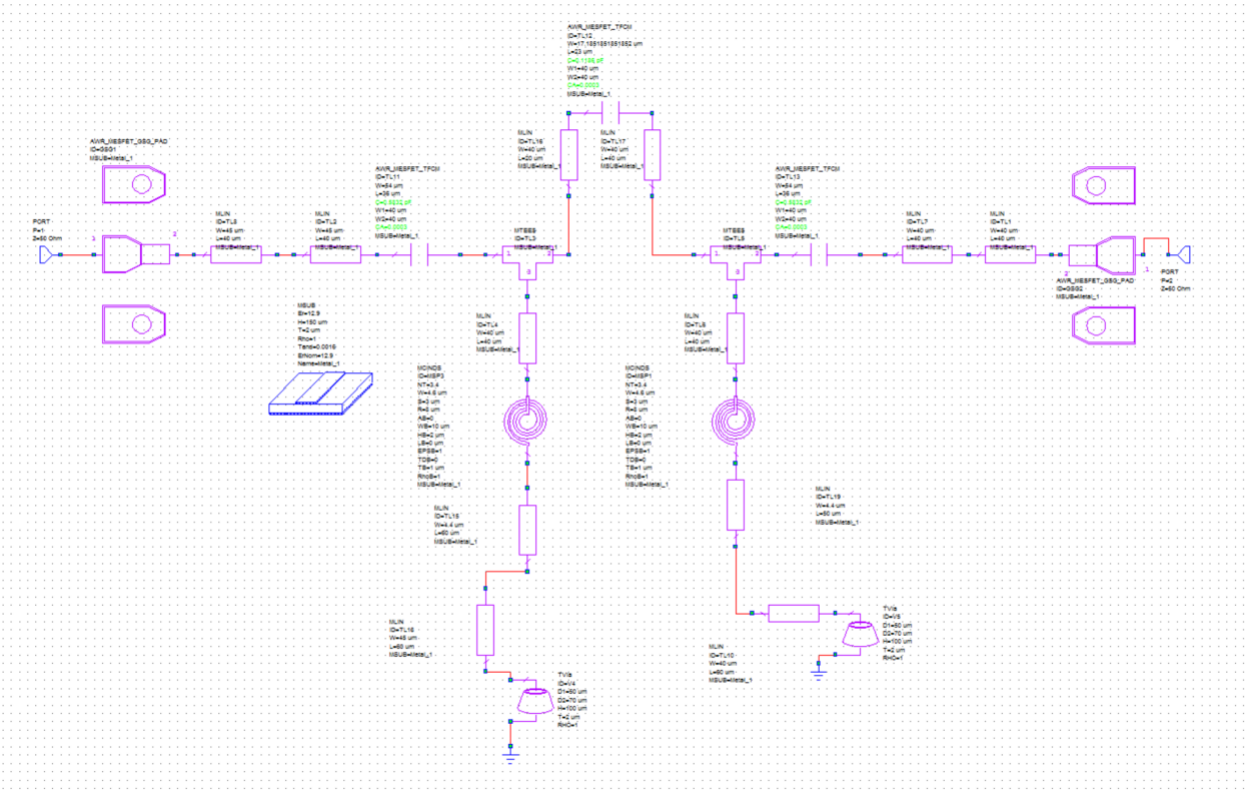
Parameter	Design Goal
f_C (GHz)	10.0
Rejection at 5GHz (dB) (actual |S21|)	≥25
No. of elements (N, odd)	Minimum
Tee topology	
Z_G and Z_L = 50Ω	
MMIC Chip Size (sq mm)	Minimum

- Number of elements required was found to be 5 from the graph (normalized frequency vs. attenuation) to get minimum 25 dB rejection at 5 GHz, where cut off frequency is 10 GHz.
- The value of inductances and capacitances were calculated from the below equations:

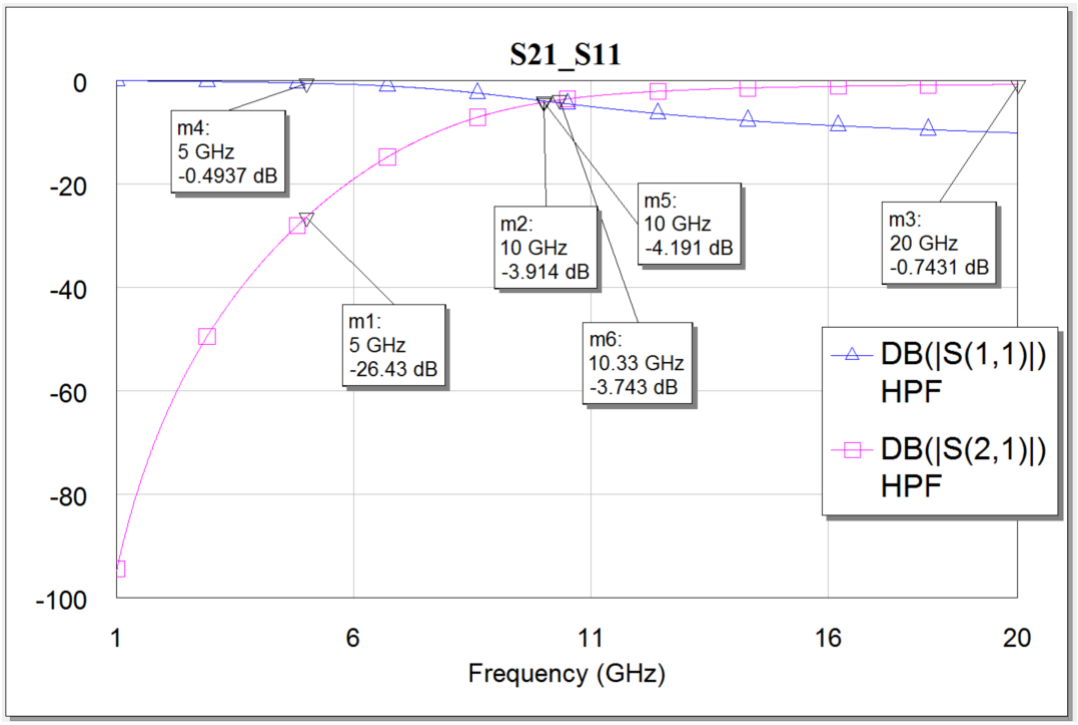
$$L = \frac{R}{2 * pi * Gn * Fc} \qquad C = \frac{1}{2 * pi * Fc * Gn * R}$$

- Ground pads were placed on both sides of the RF signal pad to enable G-S-G autoprobing capability.

1. **Circuit schematic with component values**

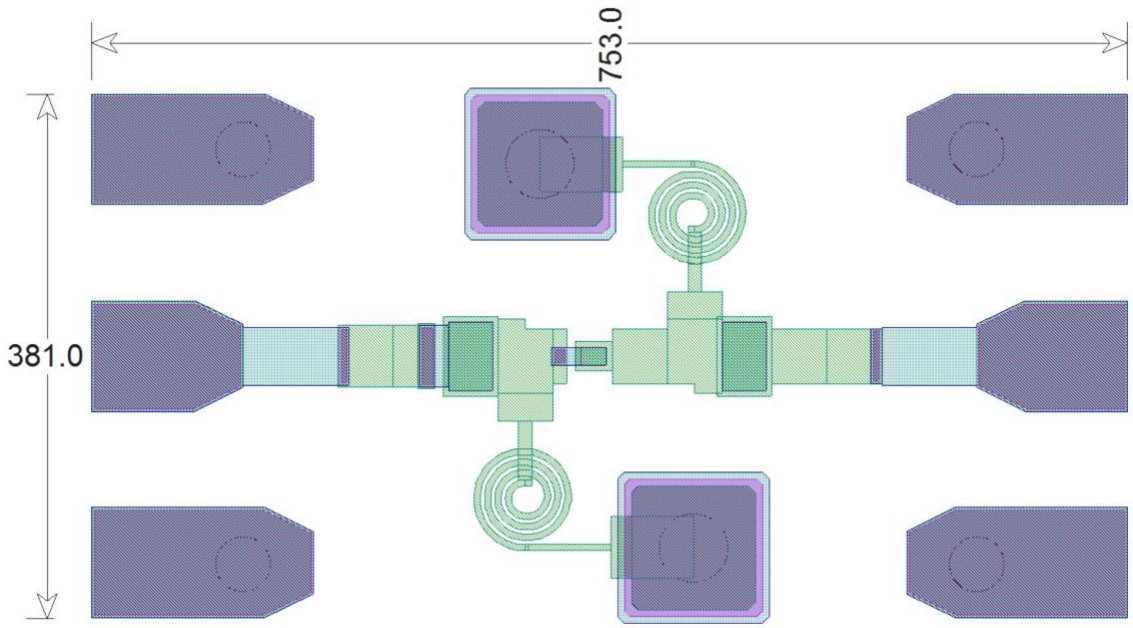


2. MWO simulation for S11 and S21 (in dB) over a frequency range 1-20GHz



The cutoff frequency is at 10.33 GHz where S21 is -3 dB down from its maximum.

3. MMIC chip layout



4. Compliance matrix

Parameter	Design Goal	MWO Simulation Performance	Compliant (Yes/No) (+/- 5%)
Cut-off frequency (f_c)(GHz)	10 GHz	10.33 GHz	Yes
Rejection @ 5 GHz GHz (dB)	>= 25 dB	26.43	Yes
No. of elements (N, odd)	Minimum	5	Yes

5. Summary

Q1. Calculation of how many filters you would expect to yield on a 150mm diameter wafer.

Chip Area = 381 * 753 μm² = 0.286893 mm²

a. Assume the outside 10mm of the wafer cannot be used

If outside 10mm of the wafer cannot be used, then the radius will be 65 mm.
Area with 65mm = 13273.22 mm².

b. Assume you lose another 5% of the (total) wafer area for process control monitor chips

Area = 0.95 * 13273.22 = 12609.559 mm².

c. Assume you have a 90% total process & RF yield to calculate your final number of available chips from one completed wafer.

Wafer Area = 0.90 * 12609.559 mm² = 11348.6 mm².

Number of filters = 11348.6 mm² / 0.286893 mm². = 39556.91

- MMIC HPF was designed which has cut-off frequency around 10 GHz with rejection of 26.43 dB at 5 GHz.
- 39556 filters are expected to be yield on a 150mm diameter wafer.