28V 1A Boost Converter

3.3V Input
28V 1A Output
200kHz switching frequency
LT3757 IC

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28V 1A Boost Converter

Design Steps

1. System parameters and design constraints
2. Examination of working mods of System and Power IC
3. Duty cycle calculation (Duty)
4. Inductor selection (L)
5. Output capacitor selection (C)
6. Diode selection(D)
7. Switching component selection(Q)
8. Configuration of power IC’s peripherals (UVLO, RT etc.)

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Tasarım Adımları

9. Input capacitor selection
10. Defining control Loop parameters
11. Spice Simulation ve design validation
12. Schematic design
13. PCB Layout design

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1. System parameters and design constraints

1. Input Voltage (Vin) = 3.3V
2. Output Voltage (Vout) = 28V
3. Output Current (Iout) = 1.0A
4. Output Power (Pout) = 28W
5. Switching frequency (fsw) = 200kHz
6. %dVo/dt: 0.1%
7. %diL/dt: 25%

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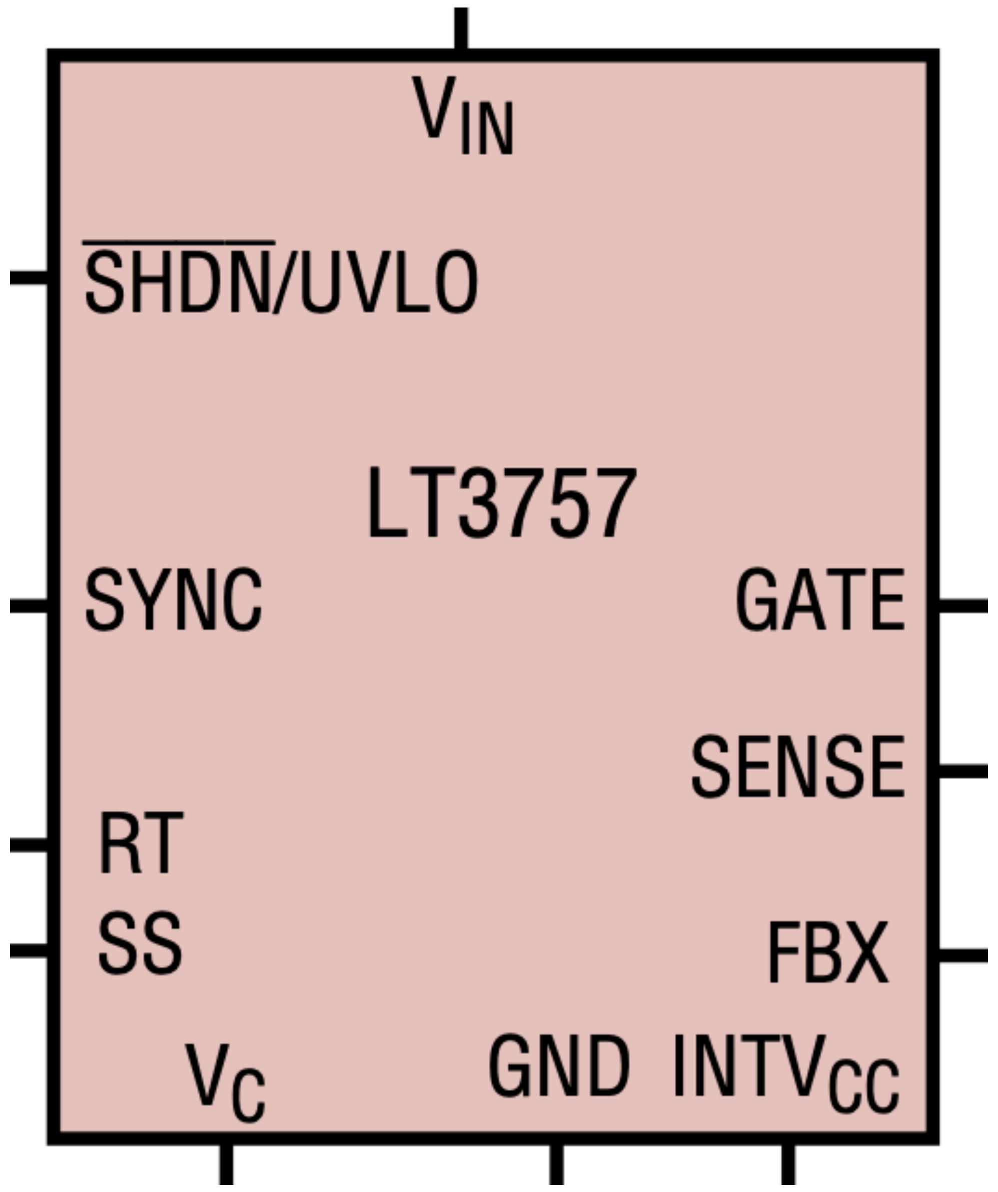
2. Examination of working mods of System and Power IC

1. nput Voltage (Vin) = 3.3V
2. Output Voltage (Vout) = 28V
3. Output Current (Iout) = 1.0A
4. Output Power (Pout) = 28W
5. Switching frequency (fsw) = 200kHz
6. %dVo/dt: 0.1%
7. %diL/dt: 25%

LT3757

Boost Controller IC

- Vin range: 2.9V to 40V
- Operating frequency: 100kHz-1MHz
- Current mode control
- Synchronizable to External Clock
- UVLO feature at 1.22V with Hysteresis
- Soft start, Frequency foldback



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3. Duty cycle value calculation (ideal Duty)

$$\frac{Vout}{Vin} = \frac{1}{1-D}$$ (ideal boost converter)

$$D = \frac{Vout - Vin}{Vin} = \frac{28 - 3.3}{28} = 0.882$$ %88.2 Duty cycle (İdeal duty cycle)

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4. Inductor selection (L)

Average Inductor Current

$$I_L = \frac{Vin}{R*(1-D)^2} = \frac{3.3}{28*(1-0.8821)^2} = 8.484A$$

$$\Delta I_L = \%\,\Delta I_L * I_L = 0.25 * 8.484A = 2.121A$$

$$I_{L_{peak}} = I_L + \Delta I_L = 8.484 + 2.121 = 10.606A$$

$$I_{L_{sat}} = I_{L_{peak}} * S = 10.606 * 1.5 = 15.909A$$

$$\Delta I_L = \frac{VinDT_{sw}}{2L}$$

$$L \geq \frac{VinD}{2\Delta I_L f_{sw}}$$

$$L \geq \frac{3.3}{2*2.121*200000}$$

$L \geq 3.431\mu H$ closest commercial inductor value 3.9uH

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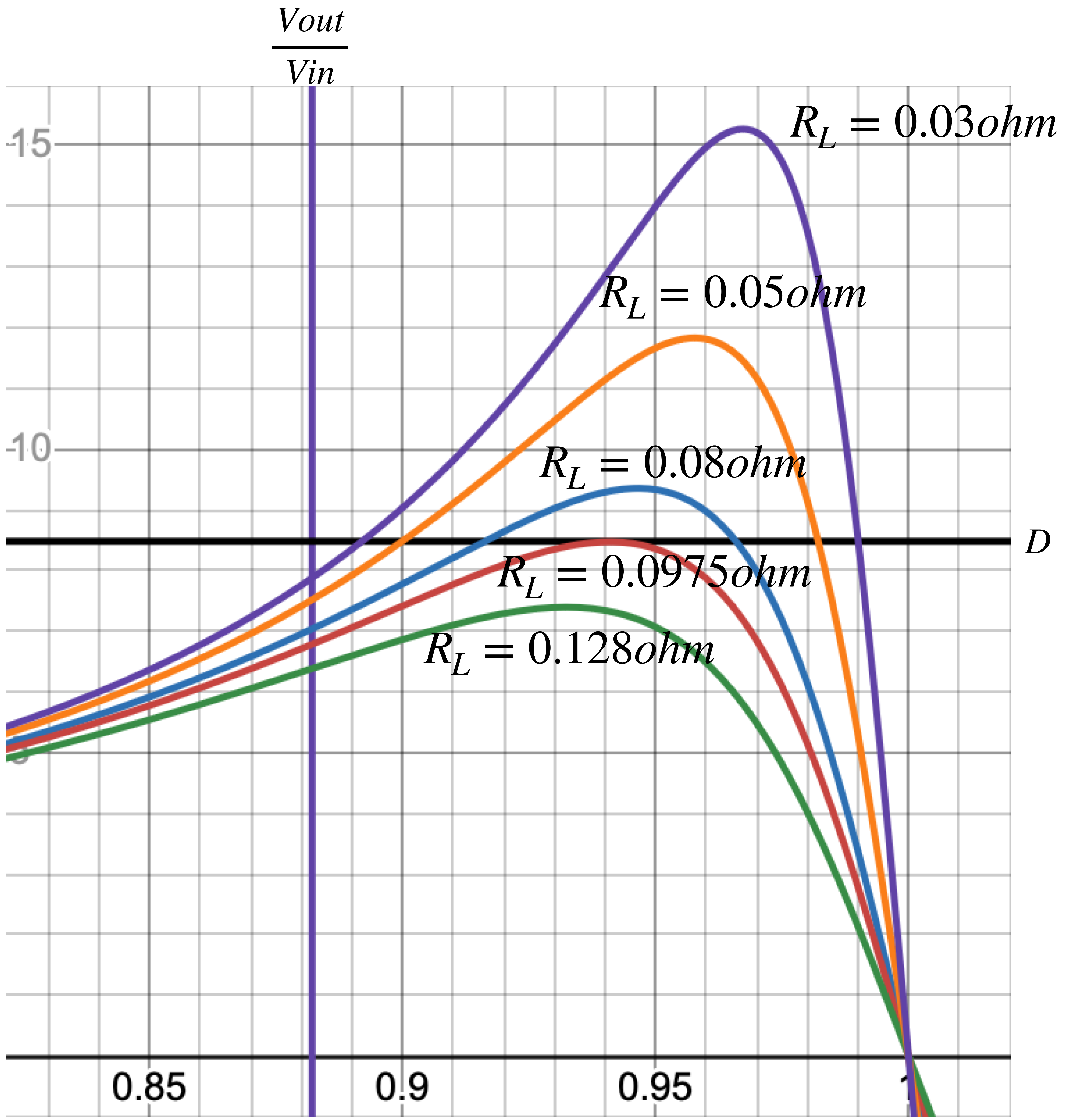
4. Inductor selection (L)

$R_L \leq 0.0975ohm$ boundary condition

The graph in the right side of the page, numerically obtained value of the inductor internal resistance must be equal or less than 0.0975ohm, if not the desired Vout/Vin ration will not be achieved.

A small RL will reduce the duty cycle value and have a positive contribution to efficiency.

By this reason RL value will be selected equal or less than $R_L \leq 0.01ohm$.



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4. Inductor selection (L)

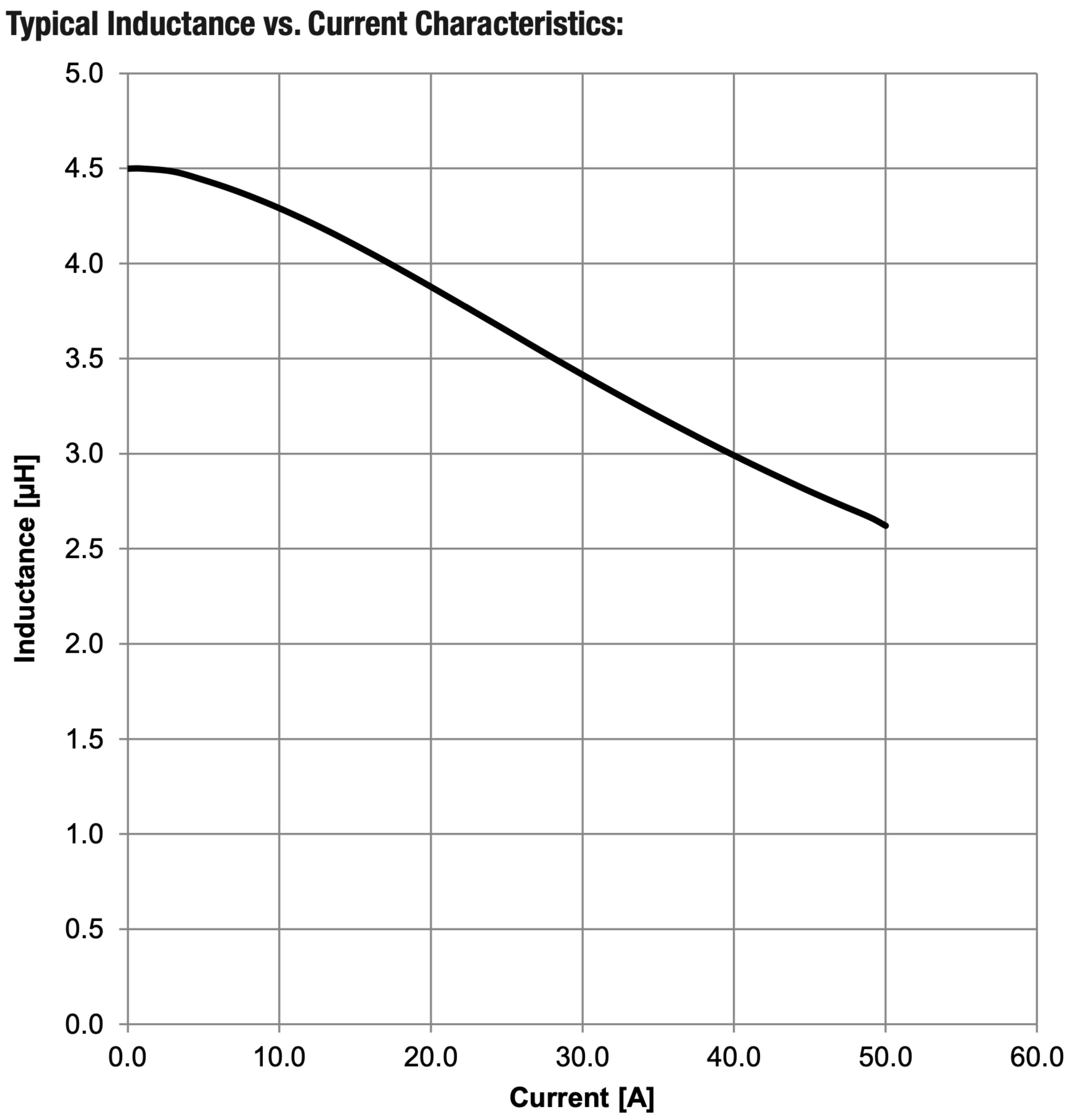
The coil that best meets these criteria was selected as the coil with the product number 7443556450 from Würth Elektronik.

L = 4.5uH

IL rated = 20.5A

Isat = 37A

DCRmax= 3.4mohm



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5. Output Capacitor Selection (Cout)

$$\Delta_{V_{out}} = \frac{Vout * D}{2 * R * C_{out} * f_{sw}}$$

$$\Delta_{V_{out}} = \% \, \Delta_{V_{out}} * V_{out} = 0.001 * 28 = 0.028 = 28mV$$

$$C_{out} = \frac{Vout * D}{2 * R * \Delta V_{out} * f_{sw}} = \frac{28 * 0.848}{2 * 28 * 0.028 * 200000} \geq 78.76\mu F$$

$C_{out} = 100\mu F$ seçildi

$$ESR \leq \frac{\Delta V_{out}}{\frac{I_{out_{max}}}{1 - D} + \Delta I_L} = \frac{0.028}{\frac{1.001}{1 - 0.882} + 2.121} \leq 2.63mohm$$

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5. Output Capacitor Selection (Cout)

In order to reduce the ESR in the output capacitor, two 39uF 50SVPF39M electrolytic capacitors and two C1210C106K5RAC7800 MLCC capacitors will be used.

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6. Diode selection (D)

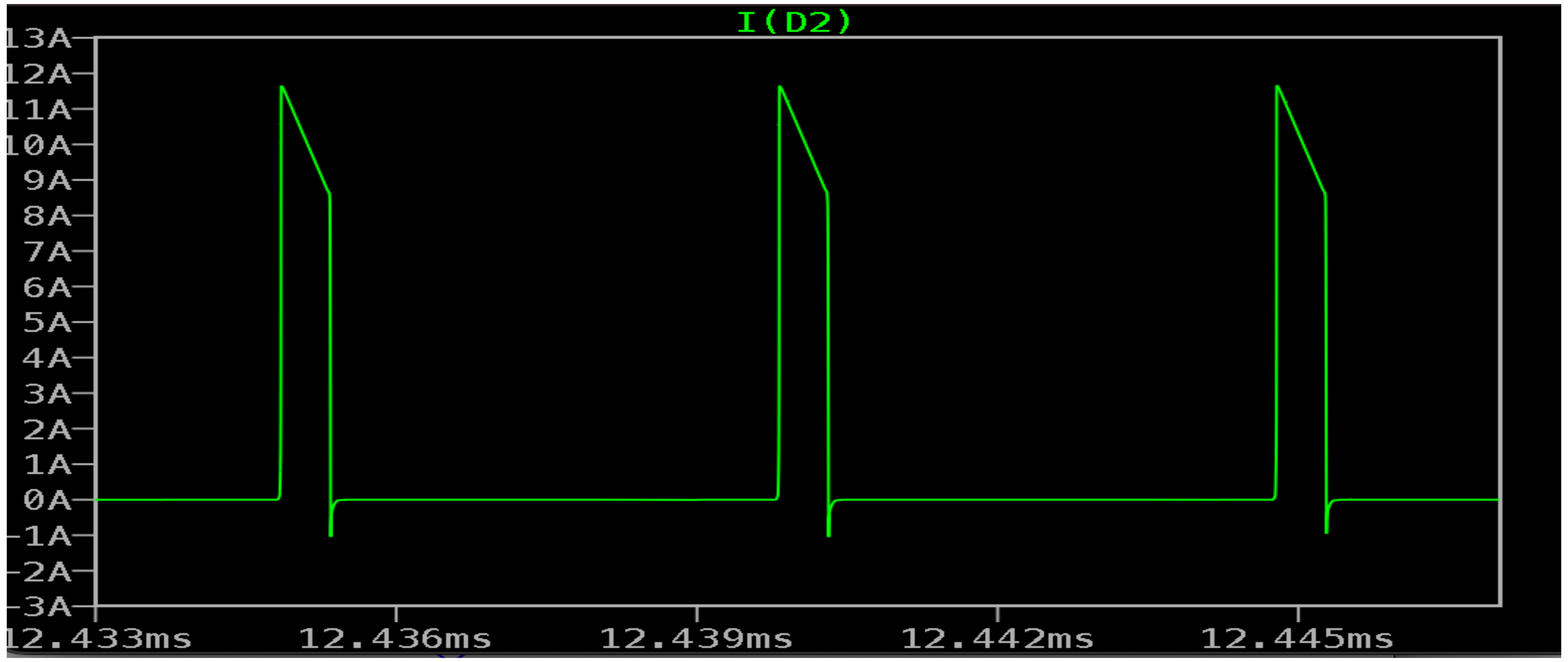
$$I_{D_{peak}} = I_{L_{peak}} = 10.606A$$

$$I_{D_{max}} = I_D * 1.5 = 15.909A$$

$$V_{D_{VRRM}} \sim \ V_{out} = 28V$$

$$V_{D_{VRRM}max} = 28 * 1.5 = 42$$

$$V_{D_{VRRM}max} \geq 42V$$



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6. Ploss of Diode

1. Forward power loss (Pf)

   As a result of the calculations made

   The diode RBQ30NS45B from Rohm company was selected.

   $$P_f = V_f * I_d = 0.590W$$

RBQ30NS45B

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7. Switching component selection(Q)

$$V_{ds} = Vout + V_f = 28 + 0.5V = 28.5V$$

The maximum Vds is multiplied by the 1.5 safety factor, and the minimum Vds value that the switching element must have is 42.75V. For this reason, a switching element with a minimum Vds value of 50V has been selected.

$I_{mosfet_{peak}} = I_{L_{peak}}$=10.606A

$V_{gs_{th}} \leq 3V$ The maximum voltage that the gate driver of the LT3757 integrated circuit can provide is 3.3V.

$P_{fet} = I_L^2 * r_{dson} * D + 2 * V_{out}^2 * I_{Lpeak} * C_{RSS} * f_{sw}/1$=1.8W

Infineon IPD079N06L3 mosfet was selected as a mosfet suitable for these conditions.

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8. Configuration of power IC's peripherals (UVLO, RT etc.)

1. Rsense resistor selection

Rsense=$\dfrac{80mV}{I_L peak} = 6.8mohm$

PRsense = $\dfrac{80mV^2}{R_{sense}} = 933mW$

$$\Delta V_{sense} = \Delta I_L peak * R_{sense} = 30mV$$

X=$\dfrac{\Delta V_{sense}}{80mV - 0.5 * \Delta V_{sense}} = 0.44$

The Vishay Dale WSL25126L800FEA18 6.8mR 2W resistor was selected to meet these conditions.

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8. Configuration of power IC’s peripherals (UVLO, RT etc.)

2. Voltage feedback resistor selection

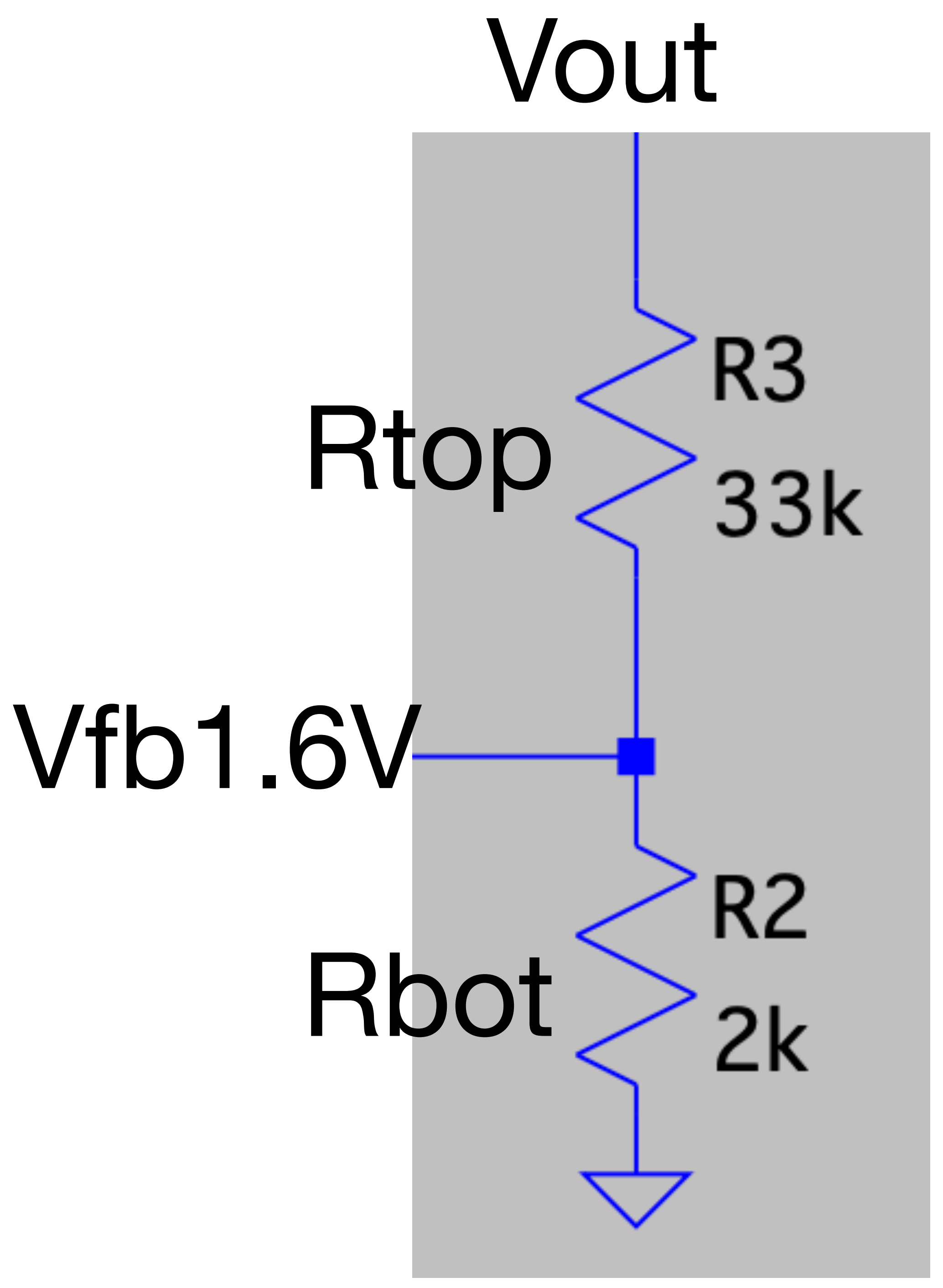
For Rtop = 33k;

$$R_{bot} = R_{top} * \frac{V_{fb}}{V_{out} - V_{fb}} = 2kohm$$

0.1% precision resistors were used as tolerance.

Rtop 33k: ERA-3AEB333V

Rbot 2k: ERA-3AEB202V



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8. Configuration of power IC's peripherals (UVLO, RT etc.)

3.Under Voltage Lock Out resistor selection

Vuvlo voltage is chosen 2.4V

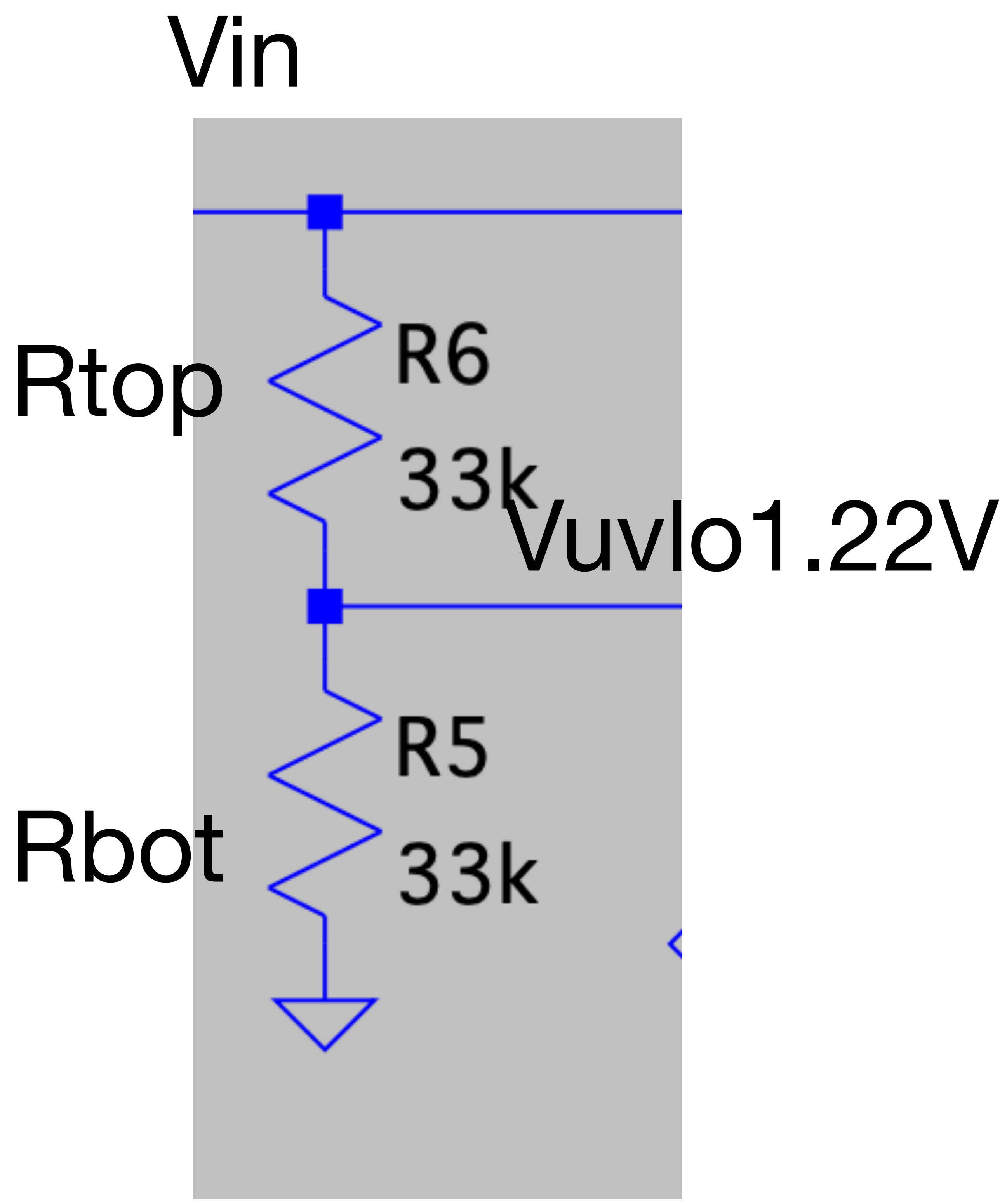
For Rtop = 33k

$$R_{bot} = R_{top} * \frac{V_{uvlo}}{V_{in} - V_{uvlo}} = 33kohm$$

0.1% tolerance precision resistors were used.

Rtop 33k: ERA-3AEB333V

Rbot 33k: ERA-3AEB333V



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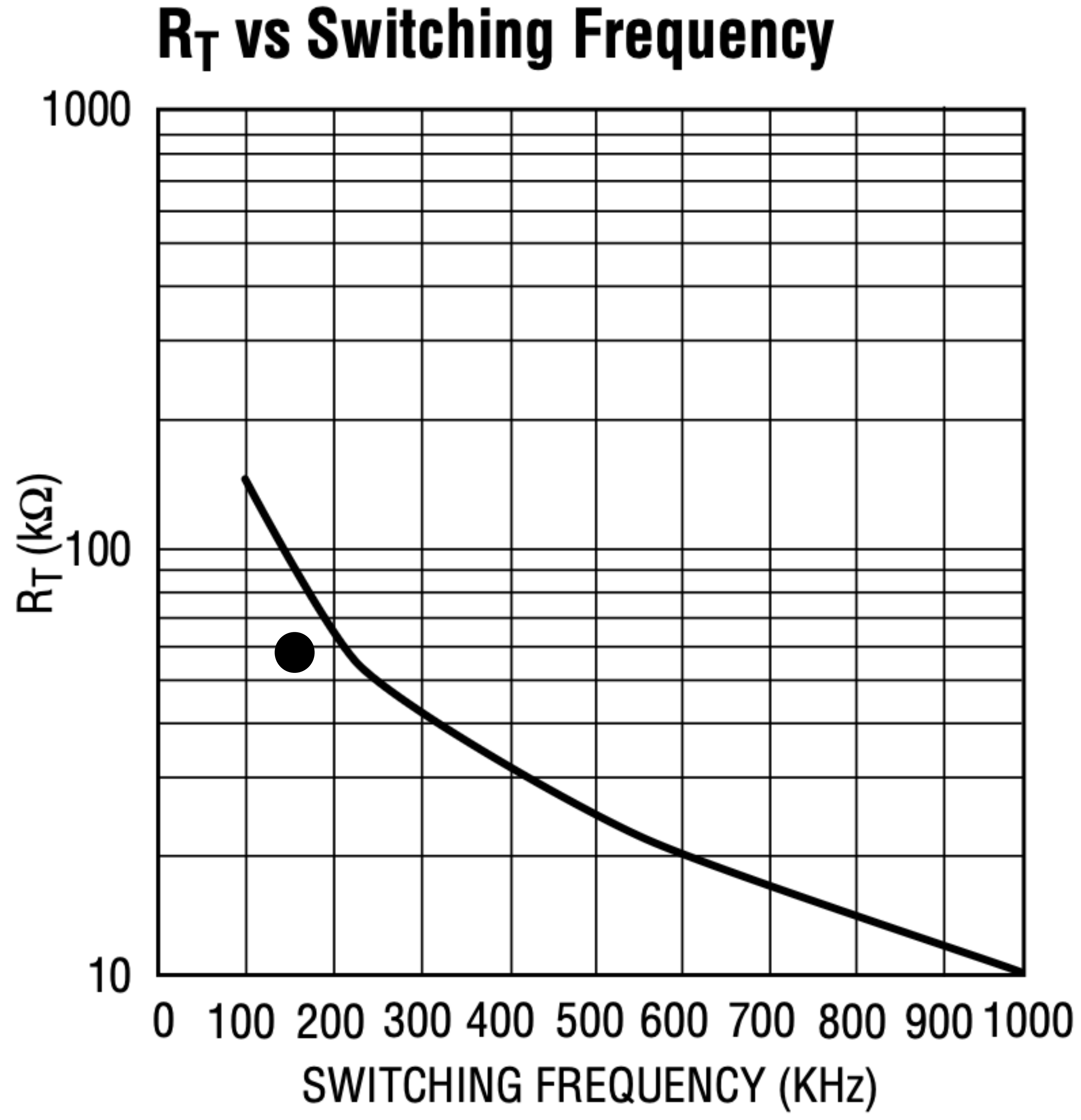
8. Configuration of power IC's peripherals (UVLO, RT etc.)

4.Rt resistor selection

The Rt resistance value is obtained from the graph on the side taken from the datasheet. According to this graph, a resistor of 68k will allow the IC to operate at a frequency of 200kHz.

Rt = 68k : ERA-6AEB683V



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8. Configuration of power IC’s peripherals (UVLO, RT etc.)

5.Soft Start (SS) capacitor

To ensure that the system performs an 8ms soft start

$Css = Tss * \dfrac{10\mu A}{1.25V} = 64nF$ aproximately 68nF

Css = 68nF : C0603C683J1RACTU %5 tolerance was chosen

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8. Configuration of power IC's peripherals (UVLO, RT etc.)

6. INTVcc capacitor selection

A capacitor of 4.7uF value specified in the datasheet was preferred. The voltage was selected as 35V.

CintVcc = 4.7uF : GRM188R6YA475KE15D was chosen.

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9. Input Capacitor Selection

The input capacitor must have a very low ESR value.
For this design <6mohm.
For this reason, three parallel 56uF EEH-ZV1J560P capacitors were selected.

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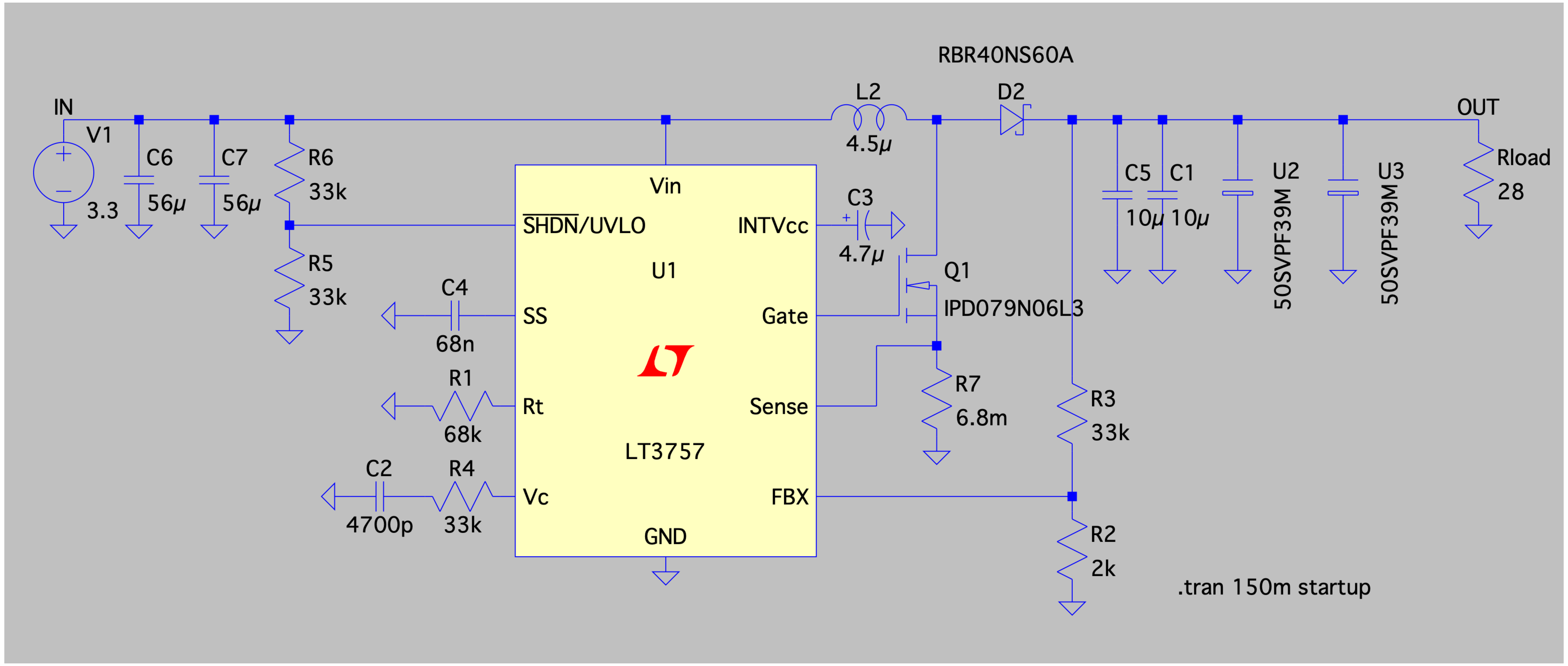
11. Spice Simulation and Design Validation

1. Spice simulation schematic



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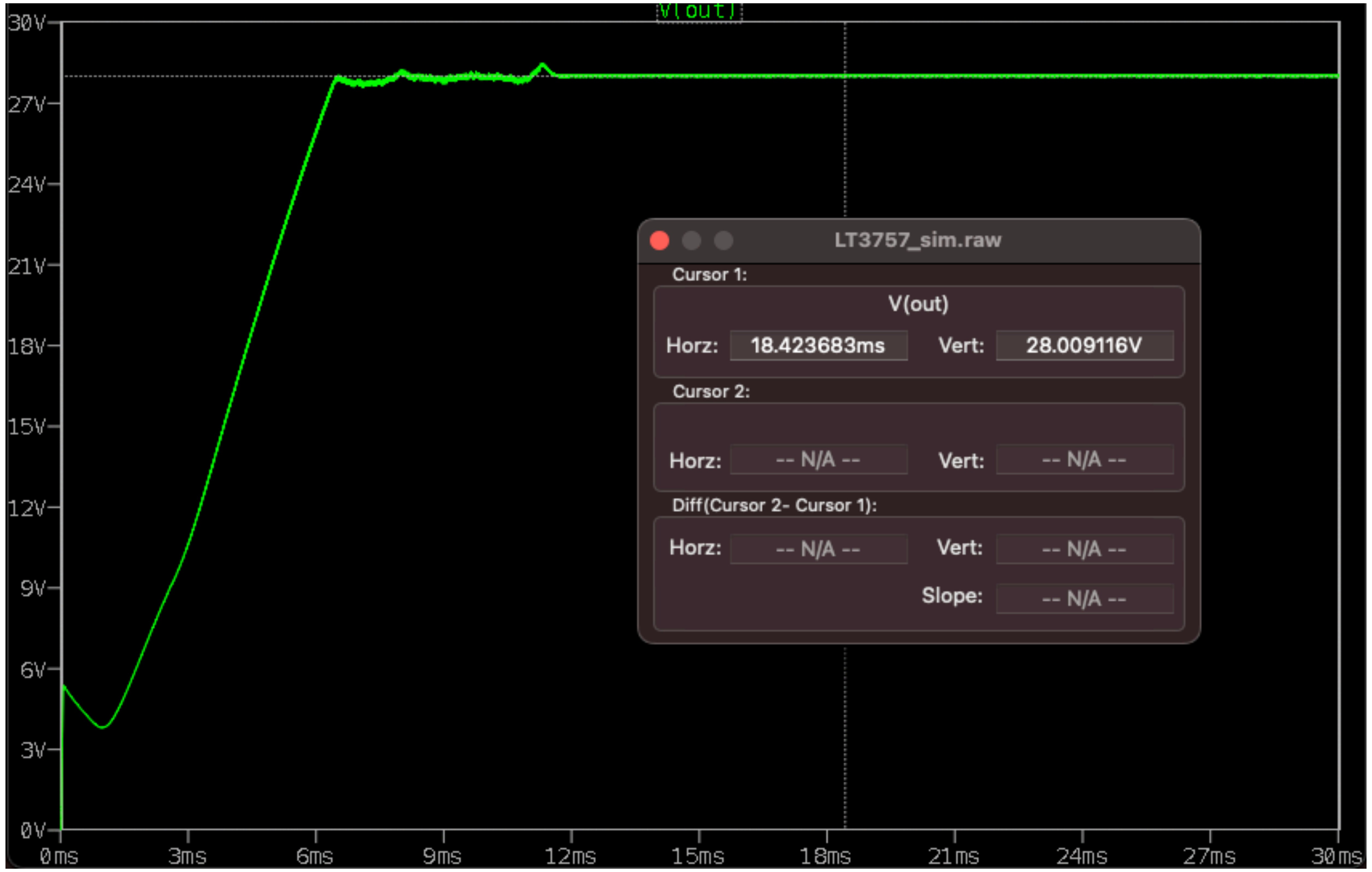
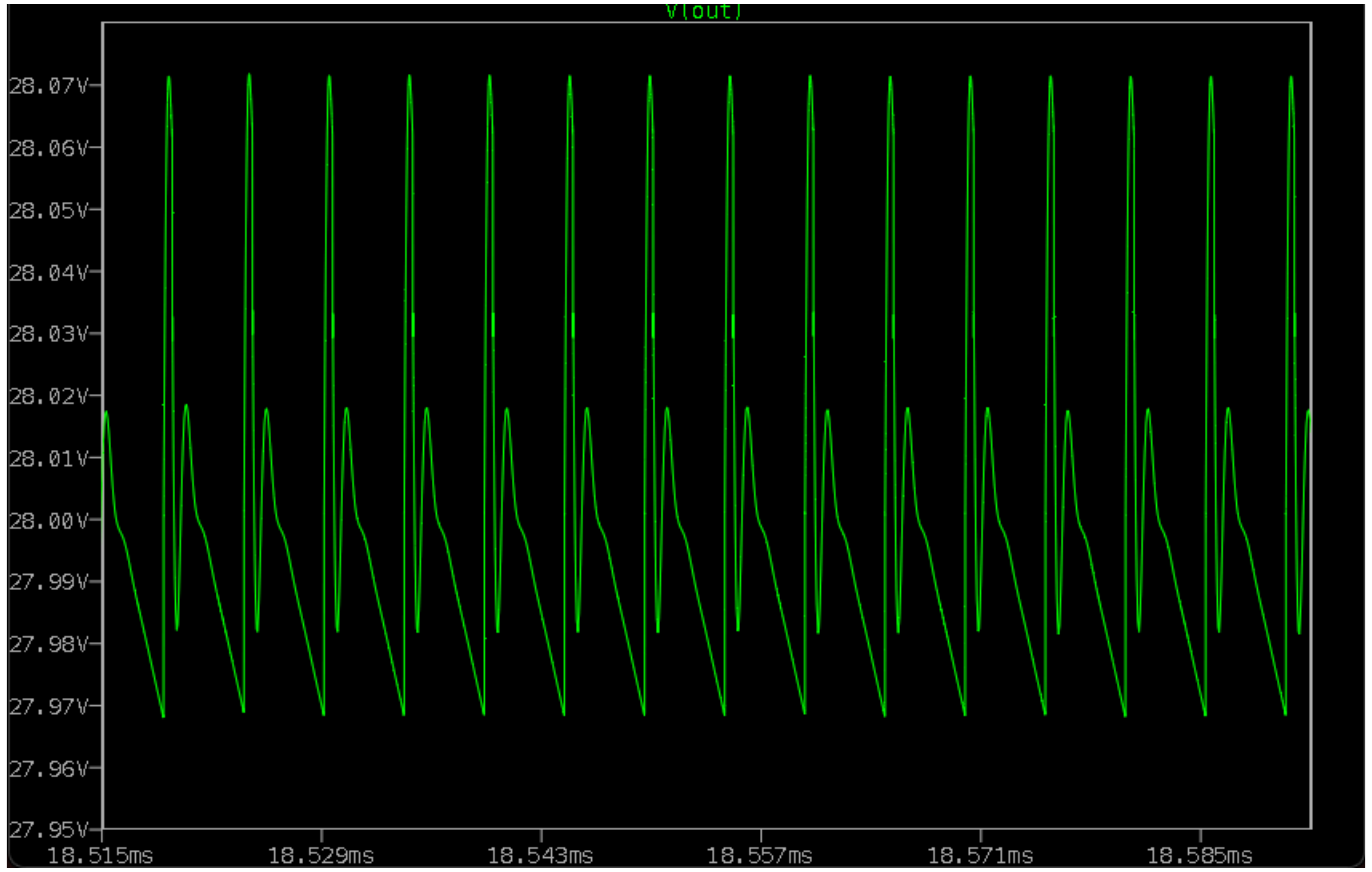
11. Spice Simulation and Design Validation

1. Output Voltage simulation





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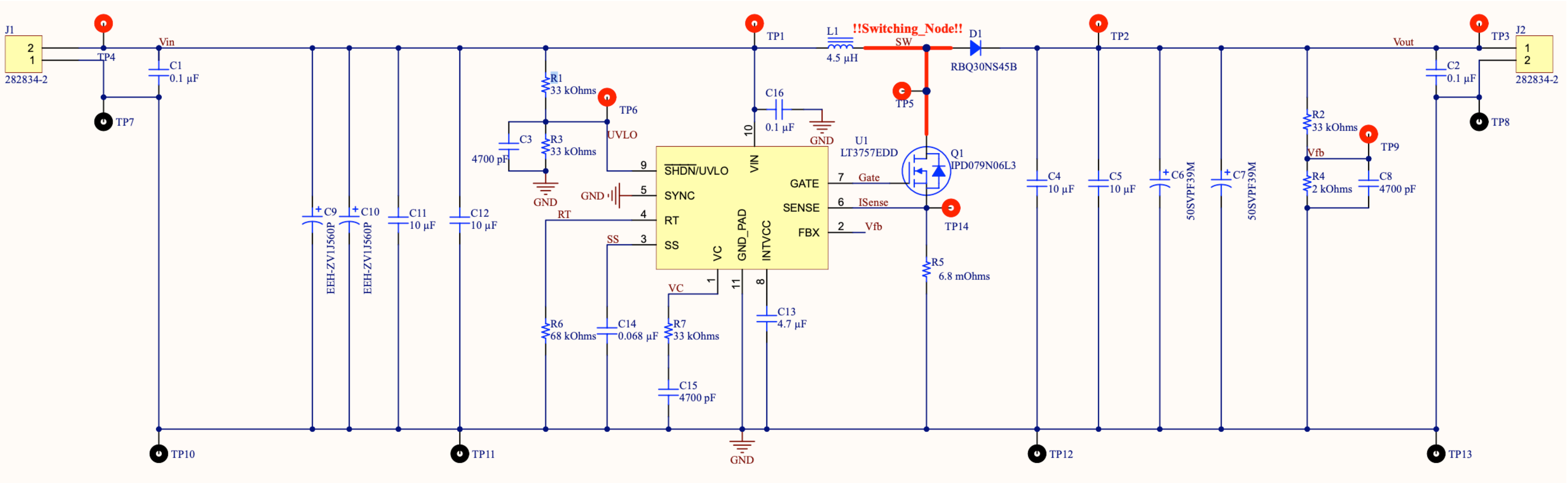
12. Schematic Design



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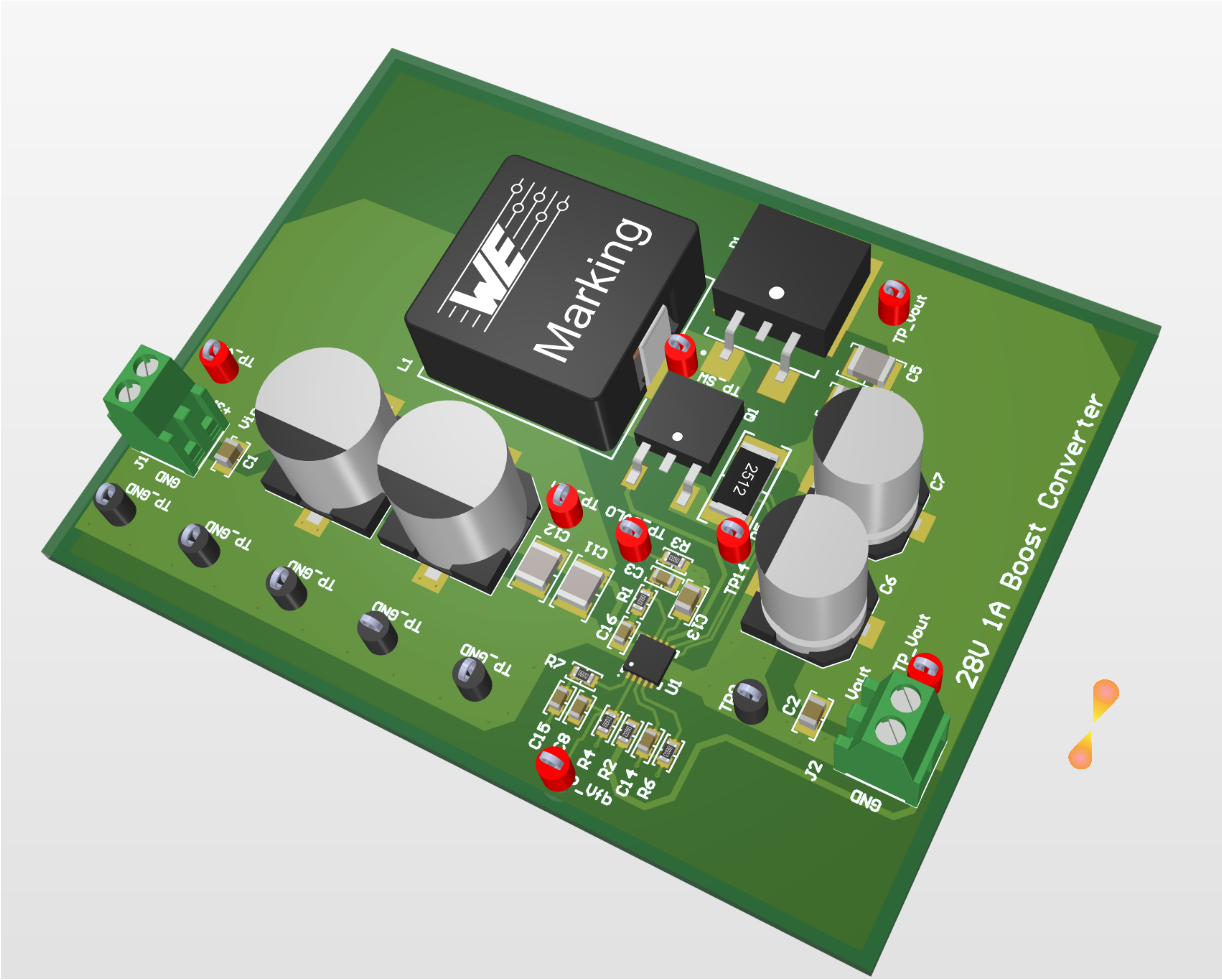
13. PCB Layout Design



3D Görünüm

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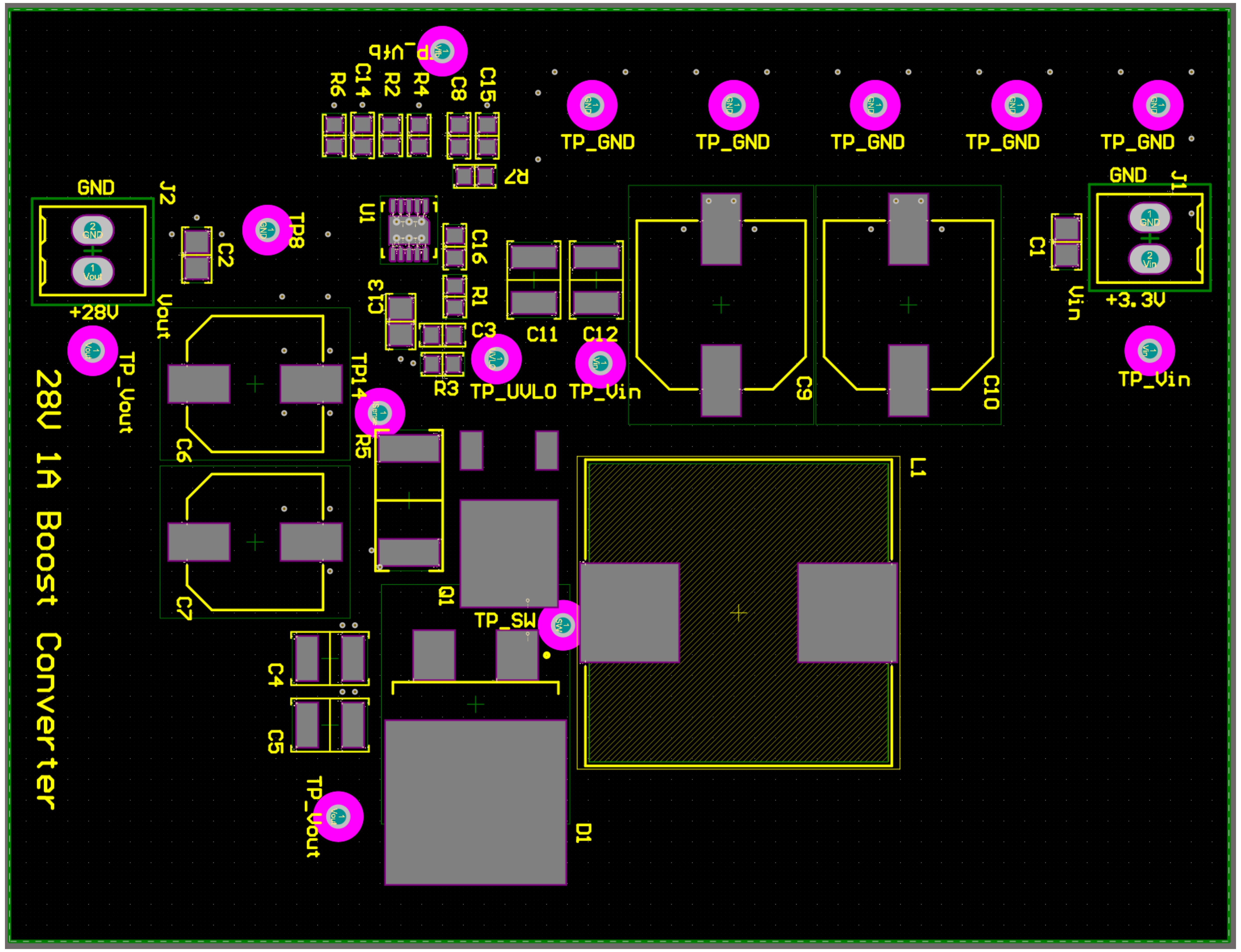

Komponent Yerleşimi

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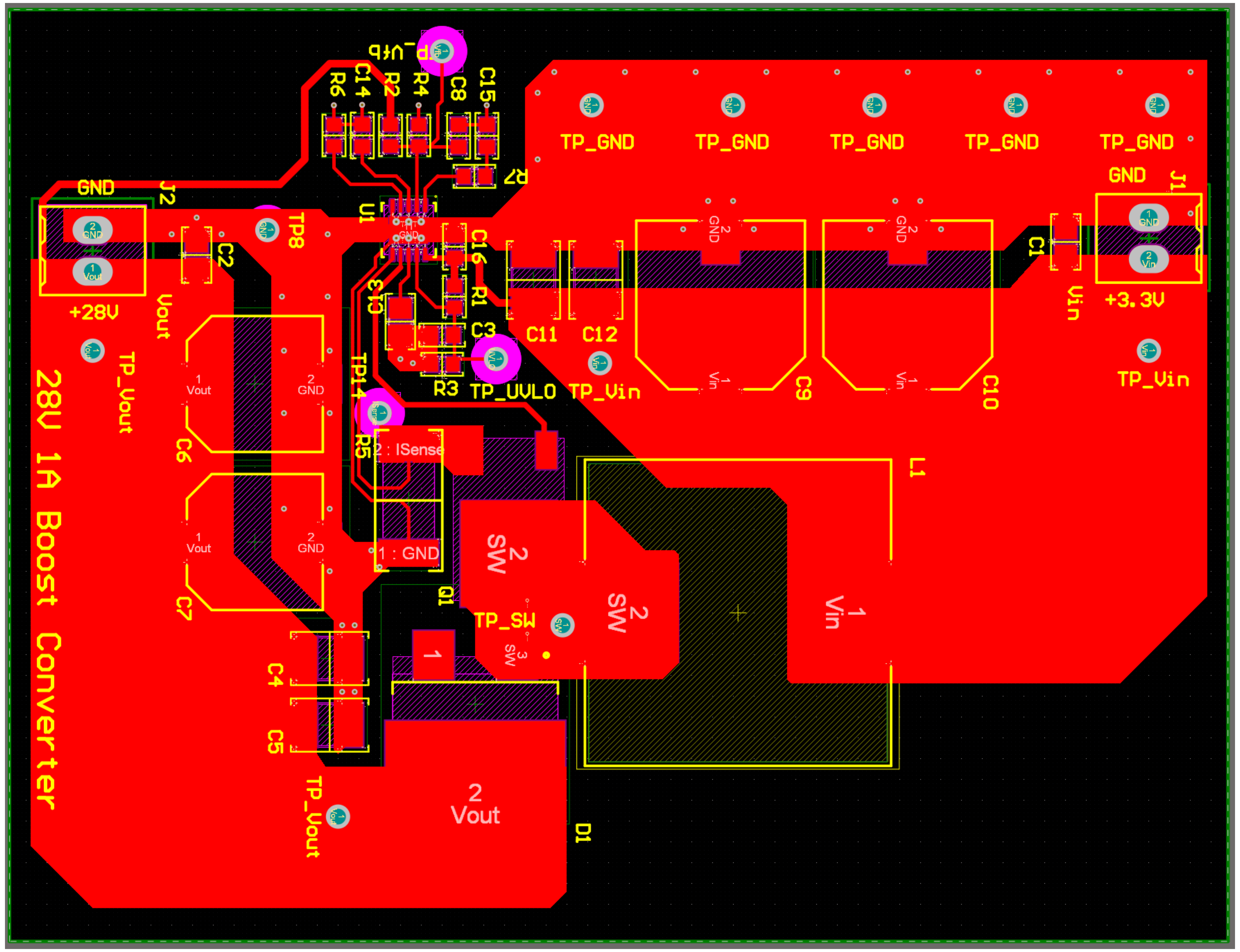
13. PCB Layout Design



Top Layer

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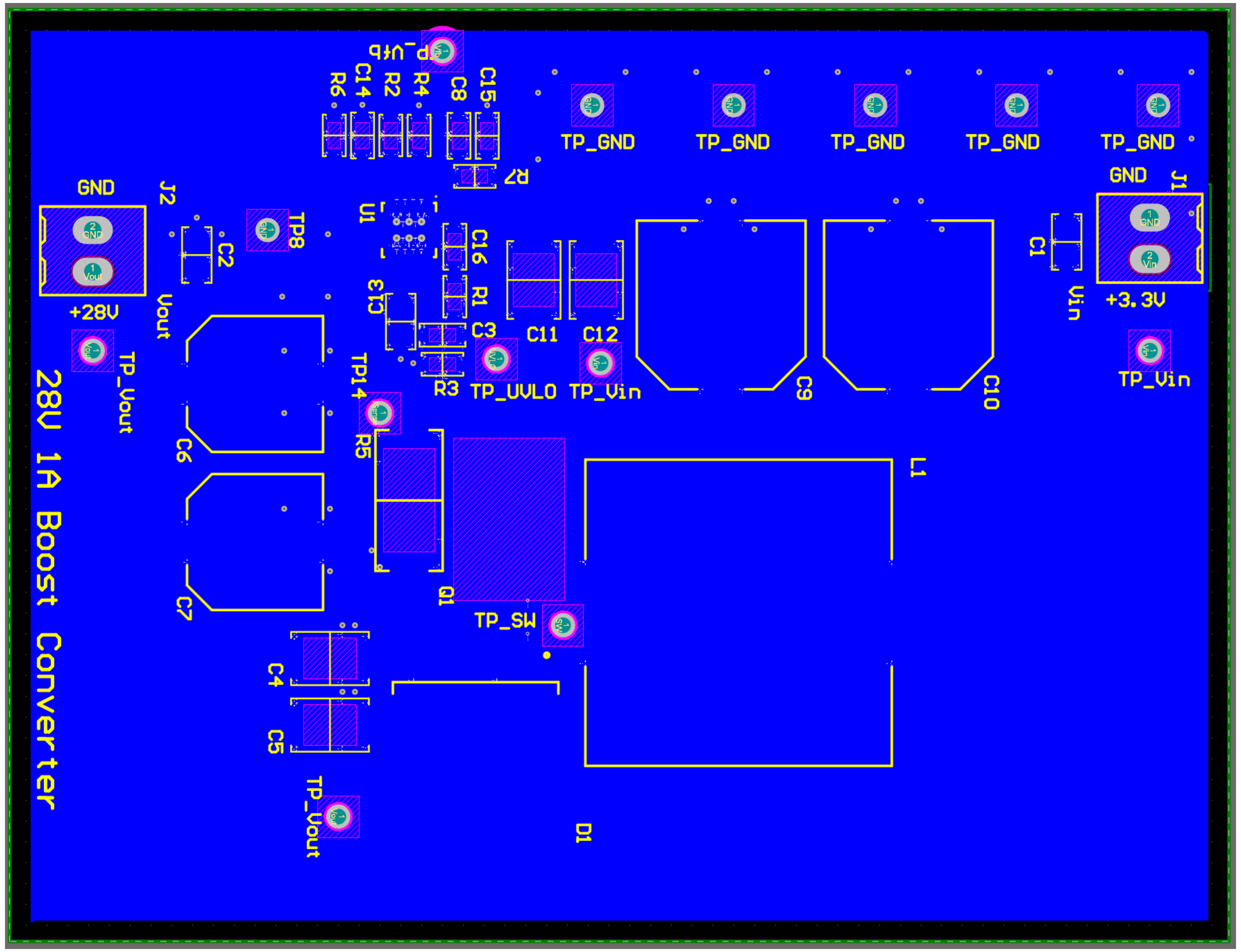
13. PCB Layout Design



Bottom Layer