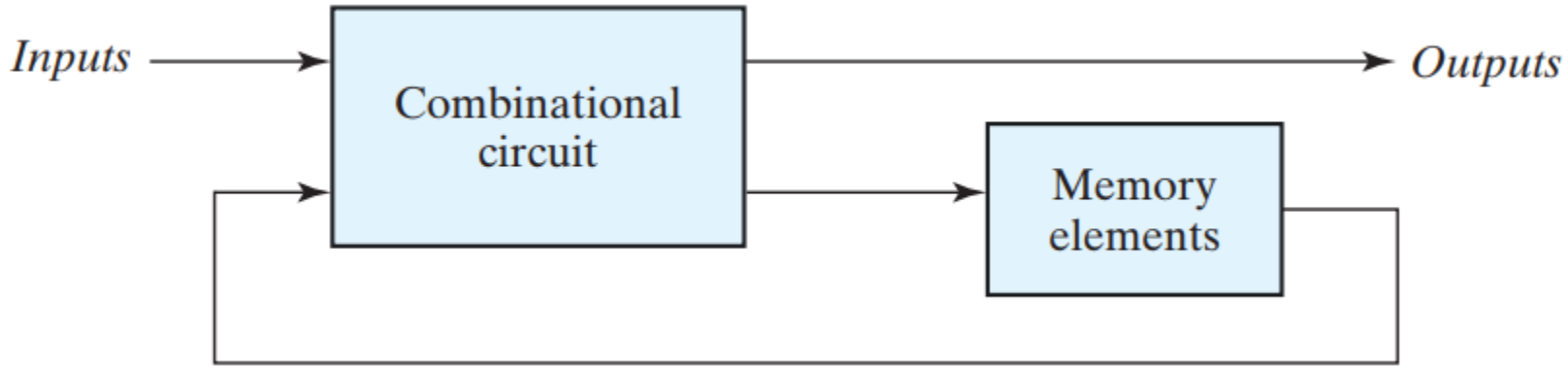
Sequential logic circuits

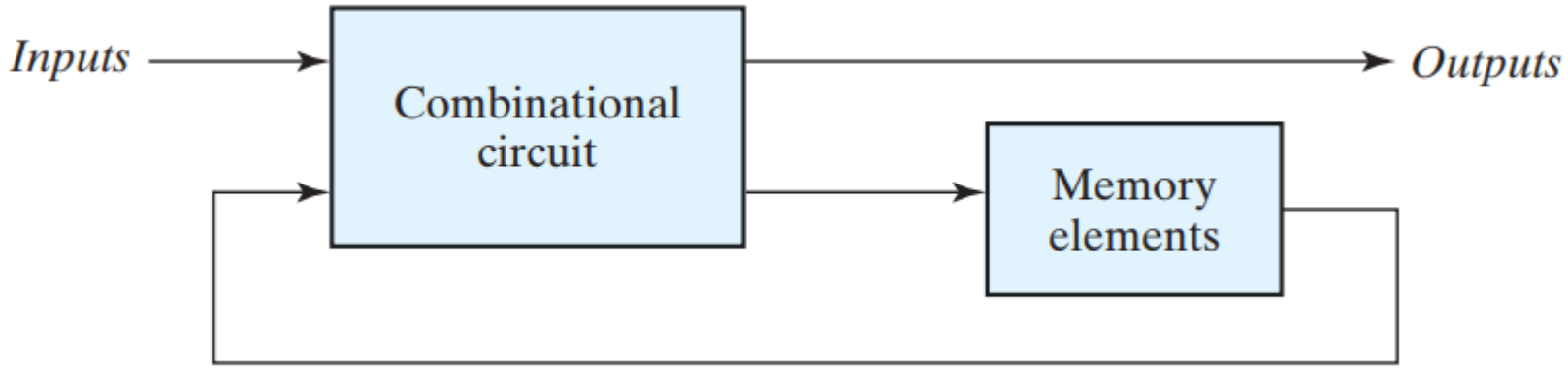
Sequential Circuit

- Output depends not only on current input but also on past input values
- Need some type of memory to remember the past input values



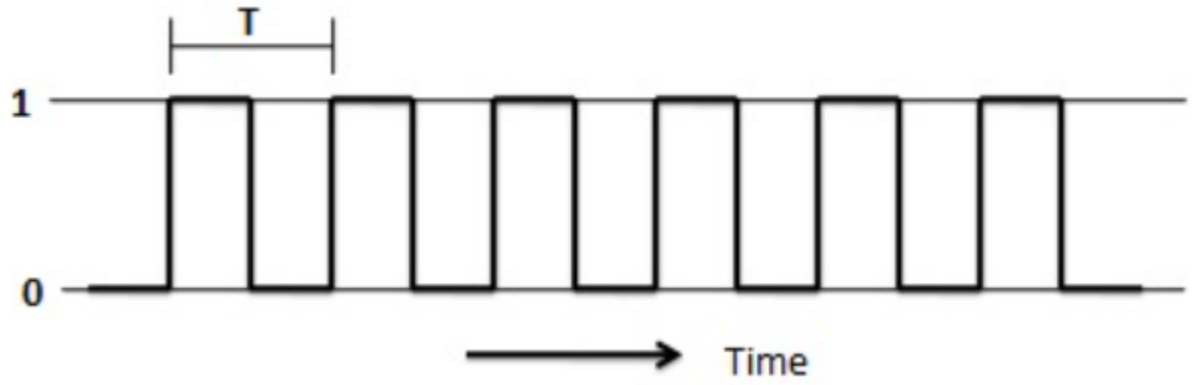
Sequential Circuit

- It consists of a combinational circuit to which storage elements are connected to form a feedback path.
- The storage elements are devices capable of storing binary information.
- The binary information stored in these elements at any given time defines the *state* of the sequential circuit at that time.



Clock Signal in Sequential Circuits

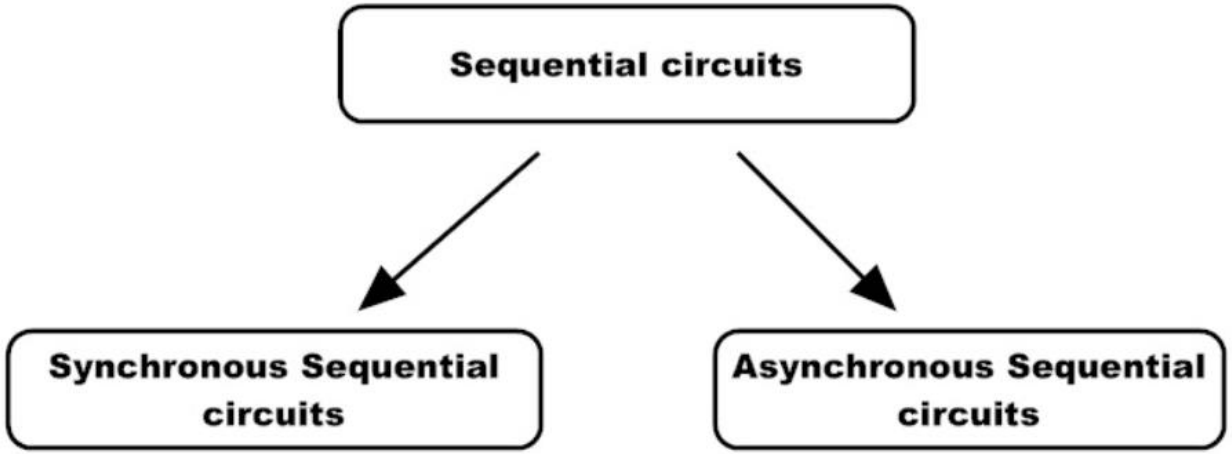
- The clock signal plays a crucial role in sequential circuits.
- A clock is a signal, which oscillates between logic level 0 and logic level 1, repeatedly.
- Square wave with constant frequency is the most common form of clock signal.



Classification of Sequential Circuits

Based on the clock signal input, the sequential circuits are classified into two types

- Synchronous sequential circuit
- Asynchronous sequential circuit



Synchronous Sequential Circuits

- In Synchronous sequential circuit, the output depends on present and previous states of the inputs at the clocked instances.
- The memory elements in these circuits will have clocks.
- These circuits are bit slower compared to asynchronous because they wait for the next clock pulse to arrive to perform the next operation

Asynchronous Sequential Circuits

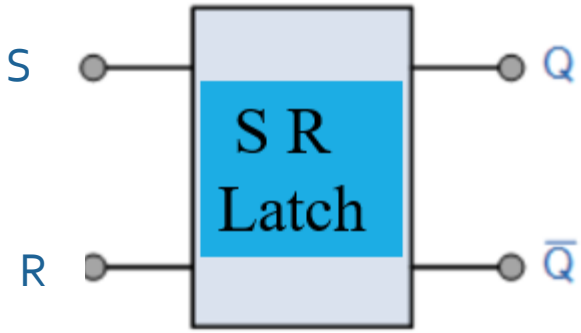
- The Sequential circuits which do not operate by clock signals are called “Asynchronous sequential circuits”.
- These circuits will change their state immediately when there is a change in the input signal .
- The Circuit behavior is determined by signals at any instant in time and the order in which input signals change

L atches and Flip-flops

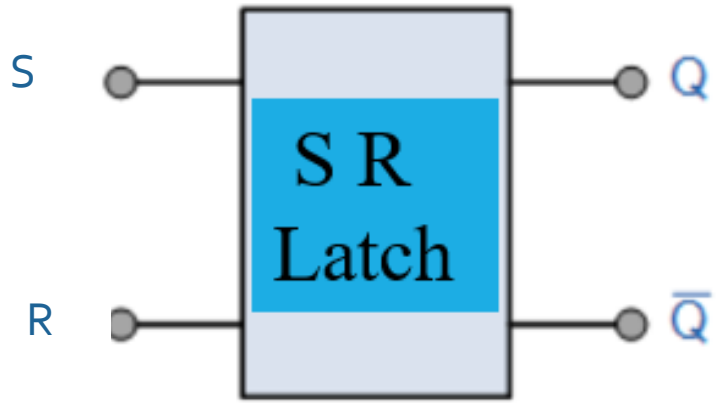
- Storage elements without a clock are called as latches.
- Storage elements which are controlled by a clock transition are called as flip-flops.

S R Latch

- The *SR* latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates
- Two inputs labeled *S* for set and *R* for reset.
- The latch has two useful states.
- When output $Q = 1$ and $\overline{Q} = 0$, the latch is said to be in the *set state*.
- When $Q = 0$ and $\overline{Q} = 1$, it is in the *reset state*.
- Outputs Q and $\overline{Q}$ are normally the complement of each other

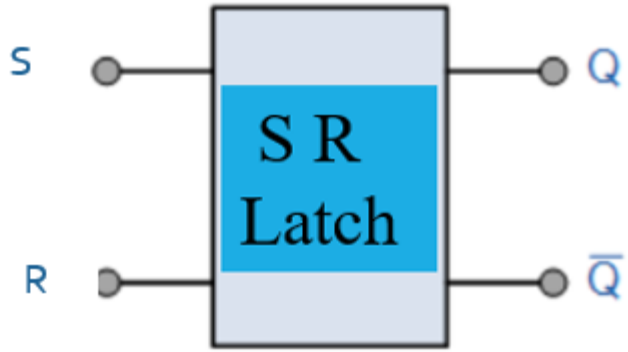


S R Latch



S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

S R Latch



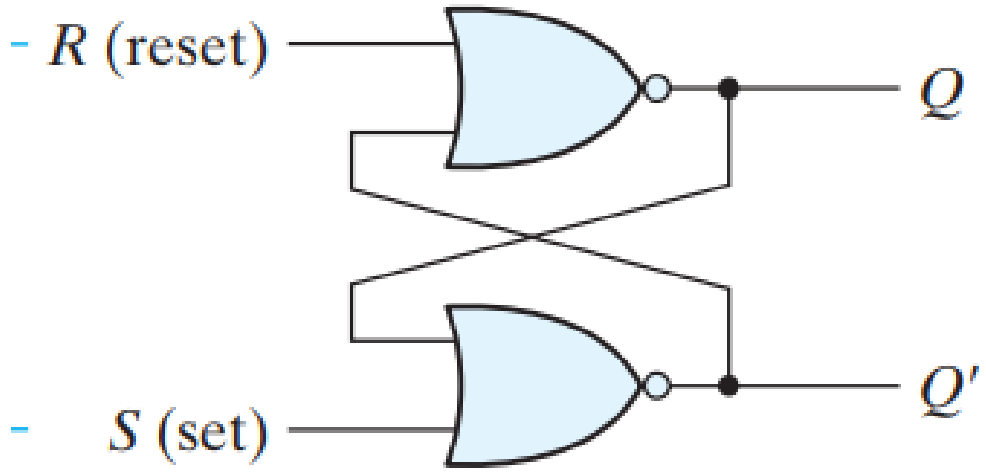
S	R	Q
0	0	**Q**
0	1	0
1	0	1
1	1	Not allowed

NAND & NOR gate

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

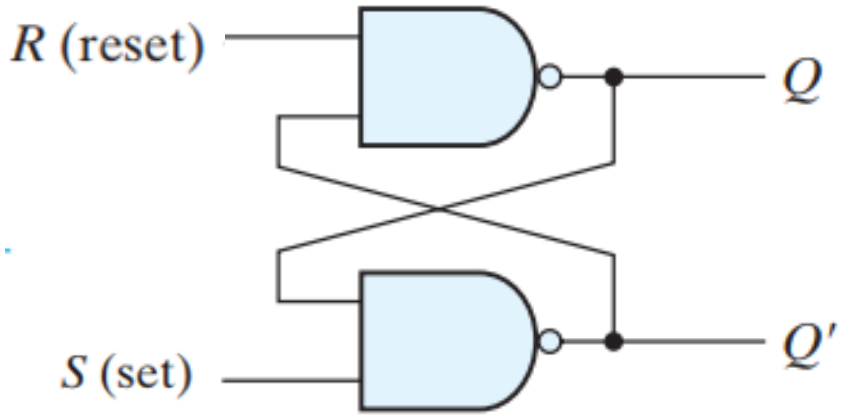
S R Latch using NOR gate



S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden)

- Under normal conditions, both inputs of the latch remain at 0 unless the state has to be changed.
- The application of a momentary 1 to the *S* input causes the latch to go to the set state.

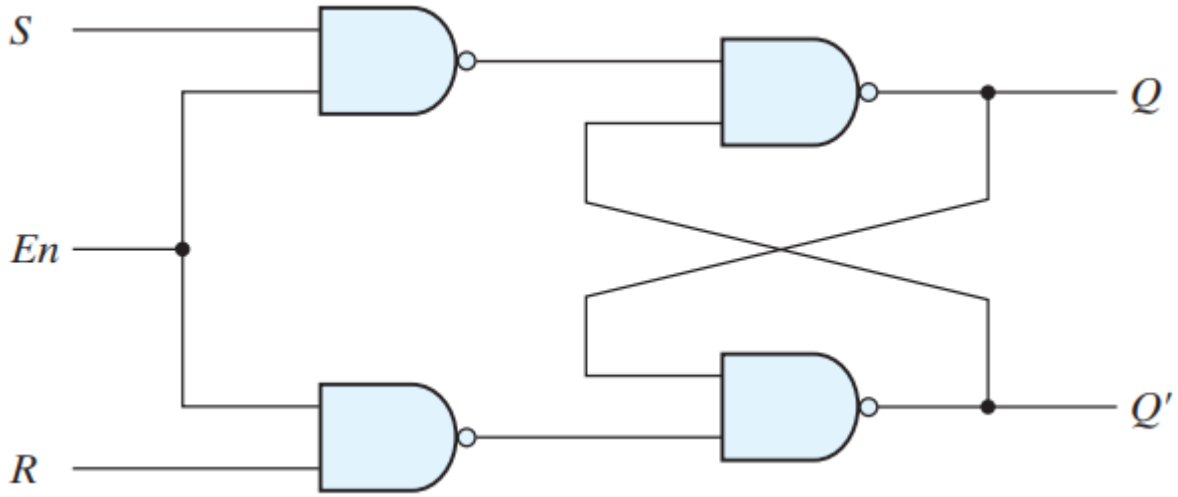
S R Latch using NAND gate



S	R	Q	Q′	
1	0	1	0	
1	1	1	0	(after $S = 1, R = 0$)
0	1	0	1	
1	1	0	1	(after $S = 0, R = 1$)
0	0	1	1	(forbidden)

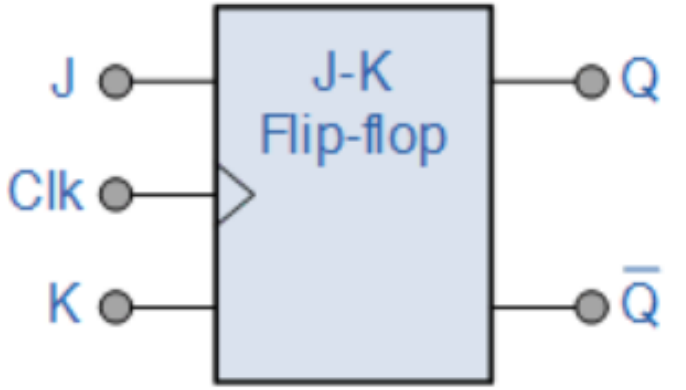
- It operates with both inputs normally at 1.
- The application of 0 to the *S* input causes output *Q* to go to 1, putting the latch in the set state.

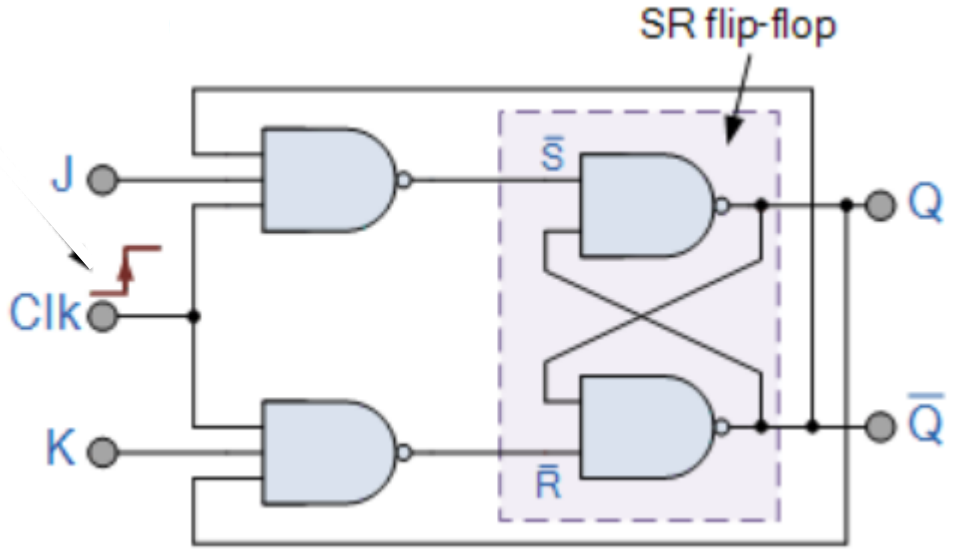
S R Latch using NAND gate and control input



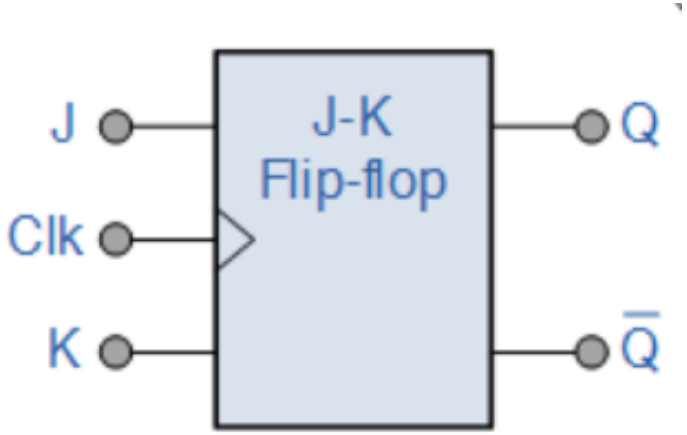
En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

J K Flip-flop


J
Clk
K
J-K
Flip-flop
Q
$\overline{Q}$


SR flip-flop
J
Clk
K
$\overline{S}$
$\overline{R}$
Q
$\overline{Q}$

J K Flip-flop



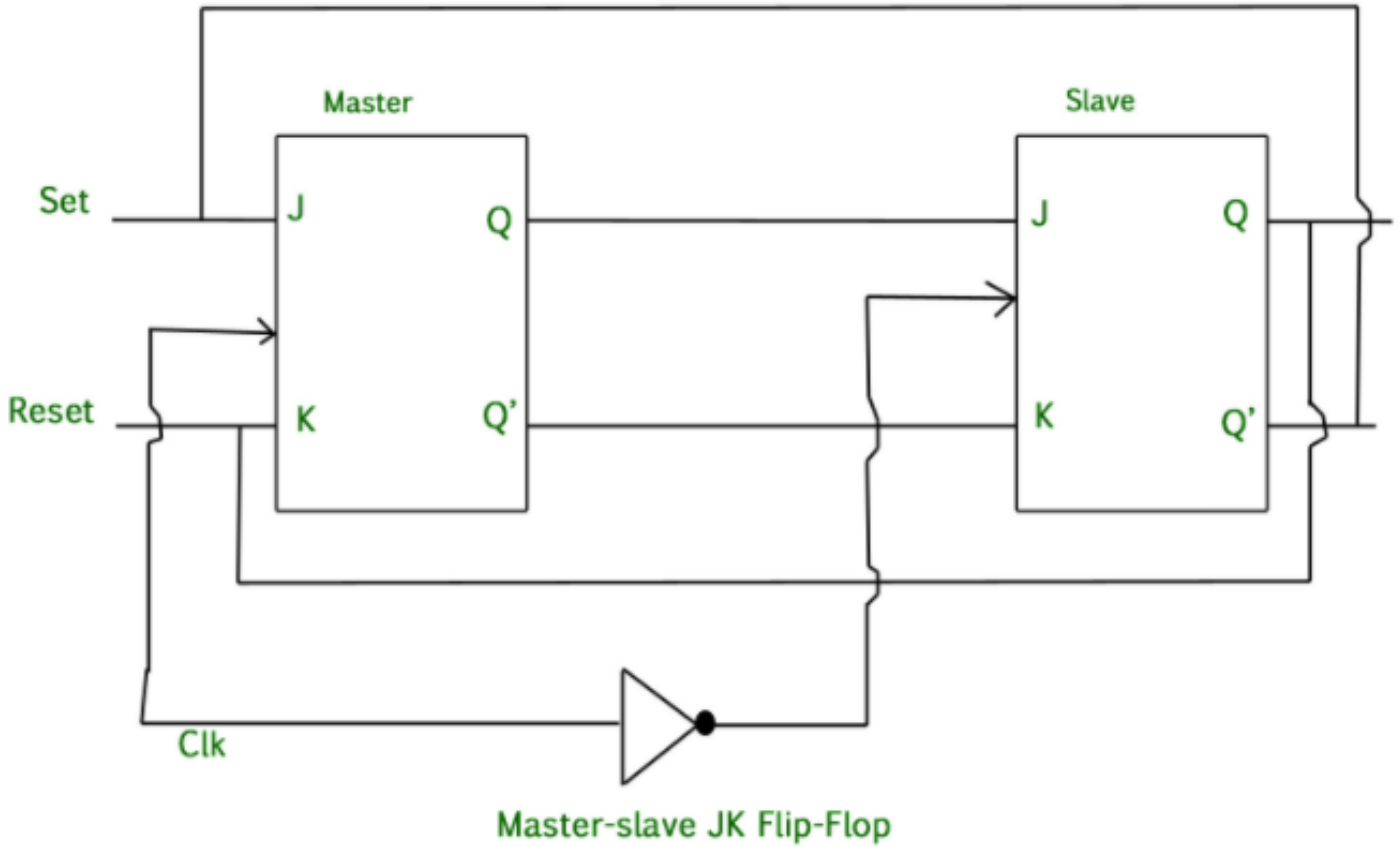
J	K	Q
0	0	**Q**
0	1	0
1	0	1
1	1	$\overline{Q}$

Race Around Condition In JK Flip-flop

For J-K flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop

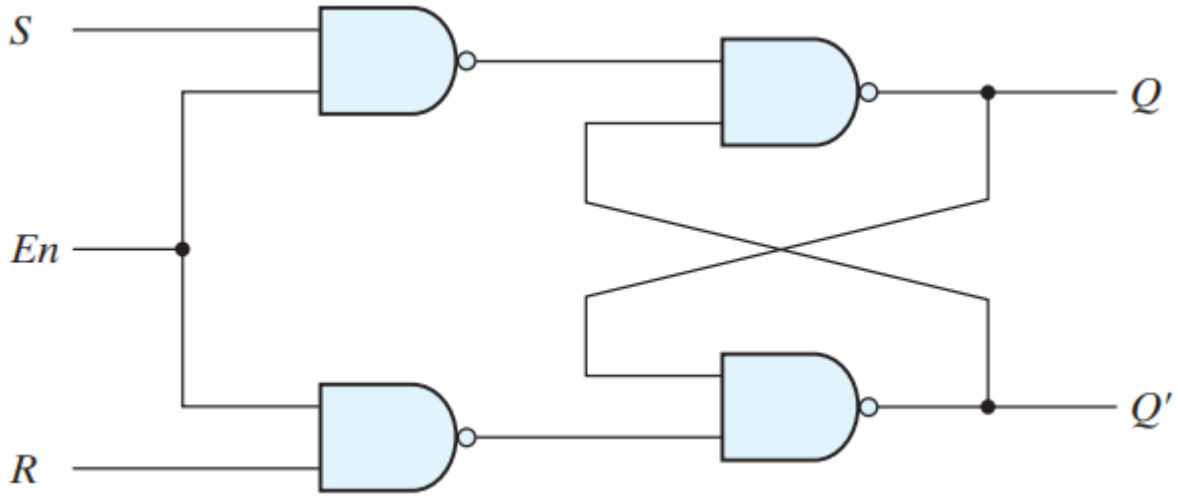
- This can be avoided by ensuring that the clock input is at logic “1” only for a very short time.
- This led to the development of Master Slave JK flip flop.

Master Slave JK flip flop



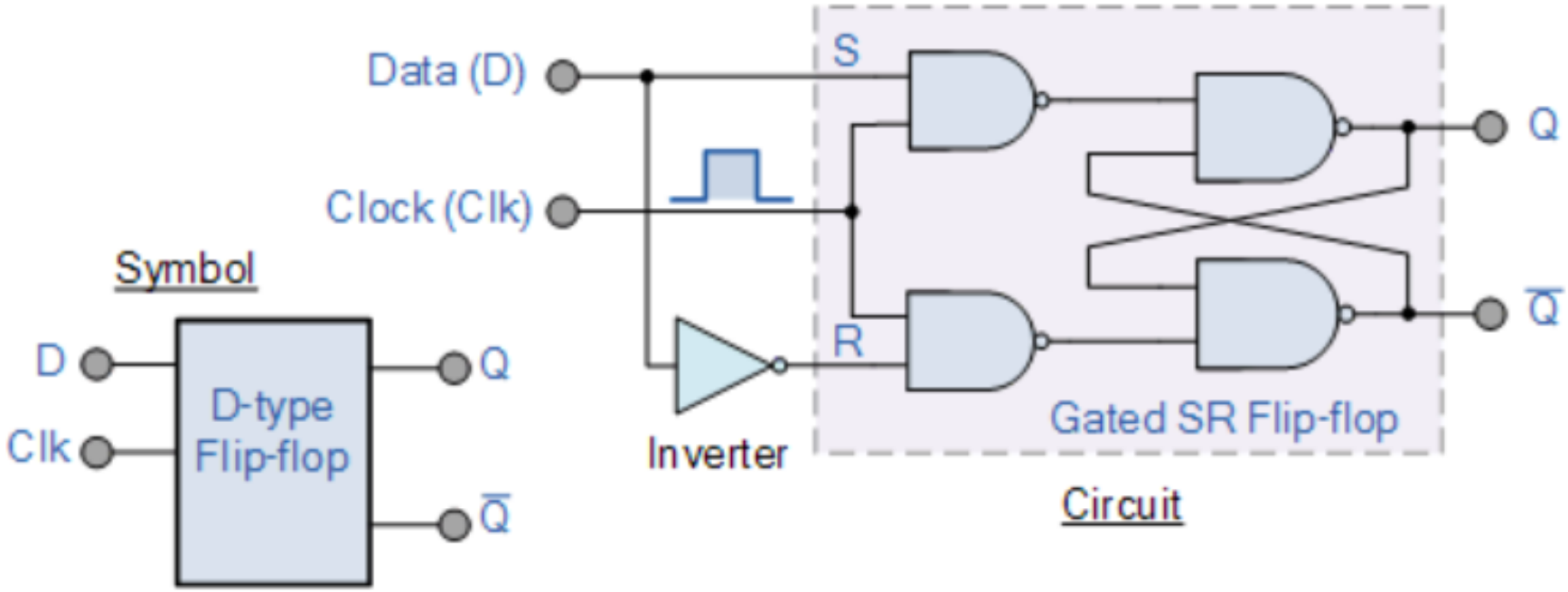
Master-slave JK Flip-Flop

S R Latch using NAND gate and control input

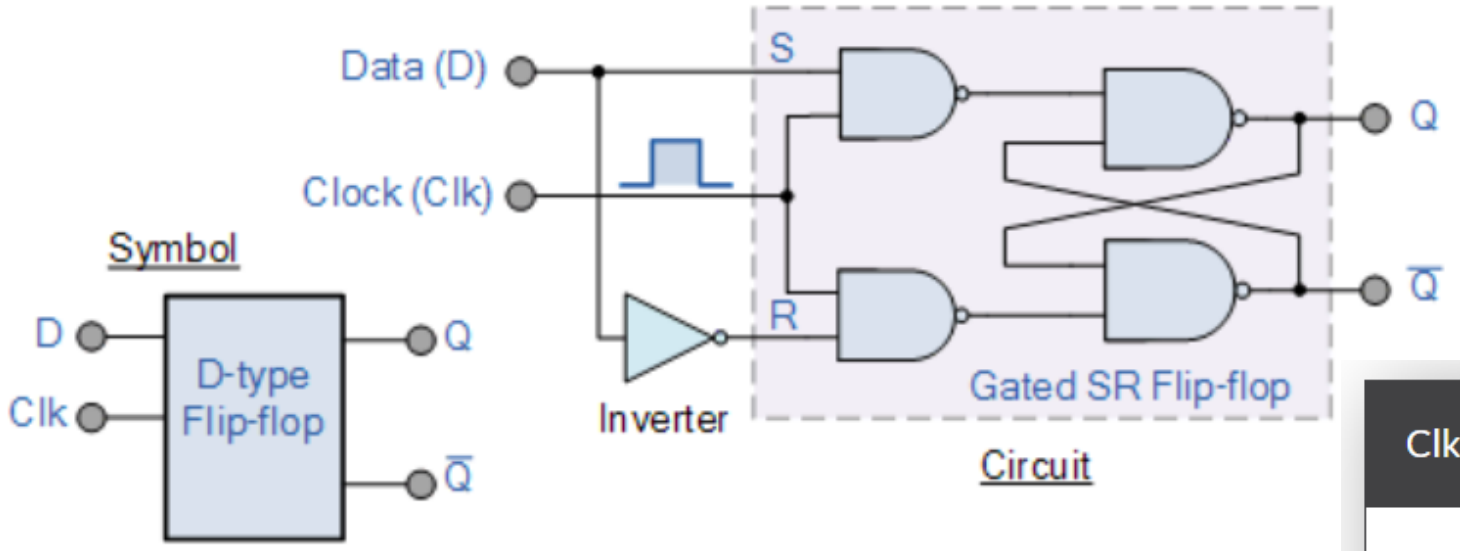


En	*S*	*R*	Next state of *Q*
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

D-flip flop


Data (D)
Clock (Clk)
S
R
Q
$\overline{Q}$
Inverter
Gated SR Flip-flop
Circuit
Symbol
D
Clk
D-type
Flip-flop
Q
$\overline{Q}$

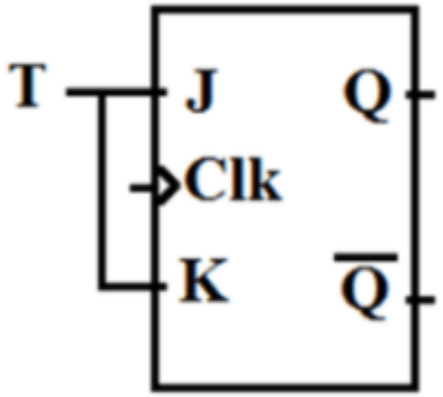
D-flip flop



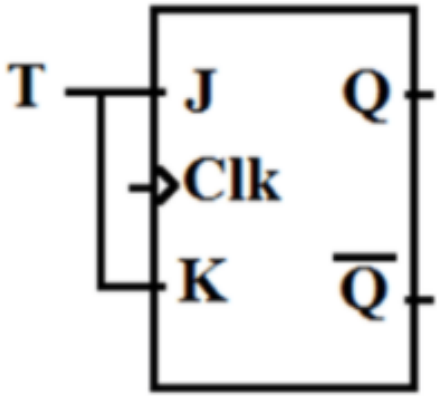
Clk	D	Q		Description
↓ » 0	X	Q	$\overline{Q}$	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

T-flip flop

T stands for the toggle. T flip-flop is modified version of JK flip-flop. JK inputs of JK flip-flop combine together to form a single input T. This flip-flop is called T flip-flop.



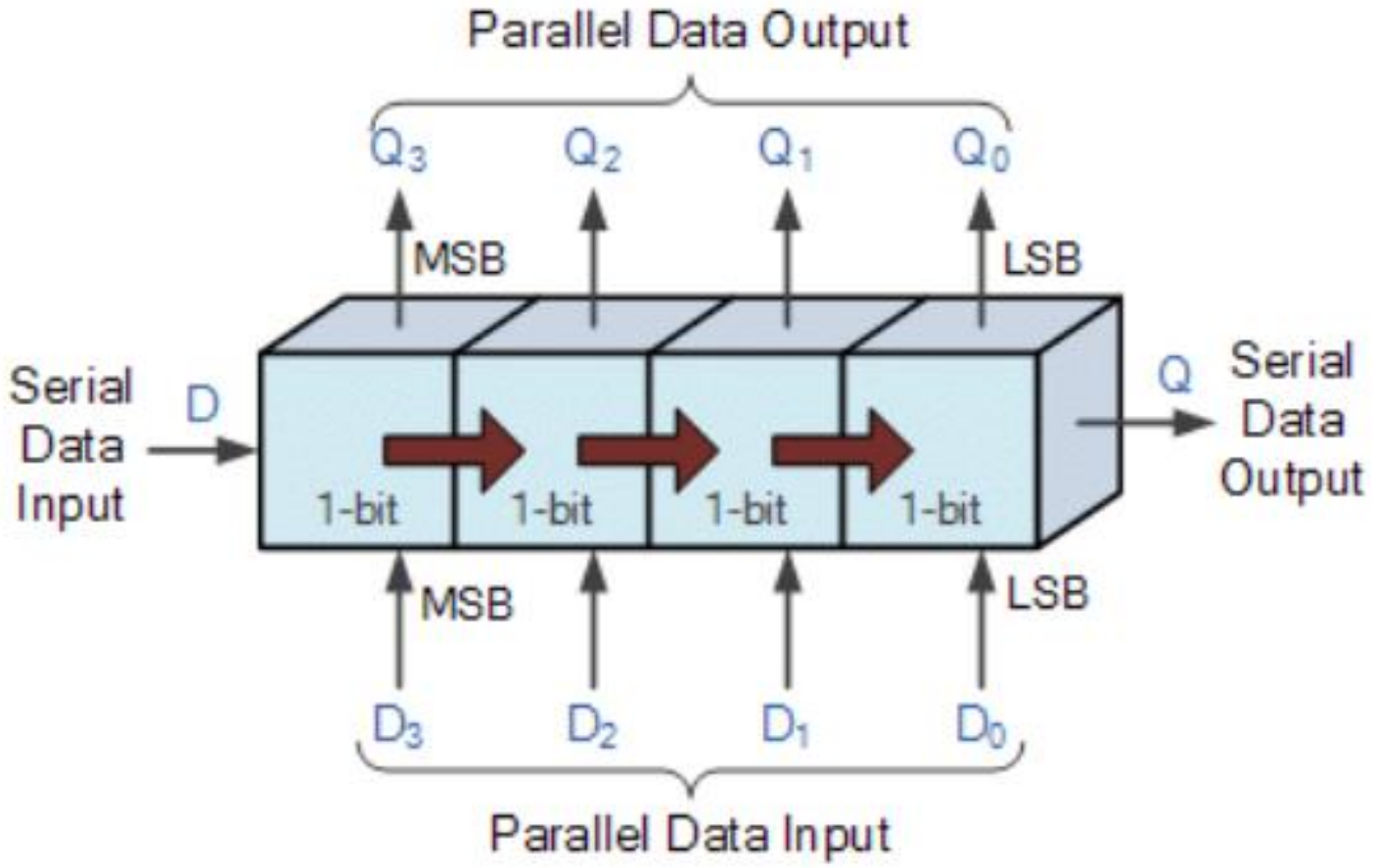
T-flip flop



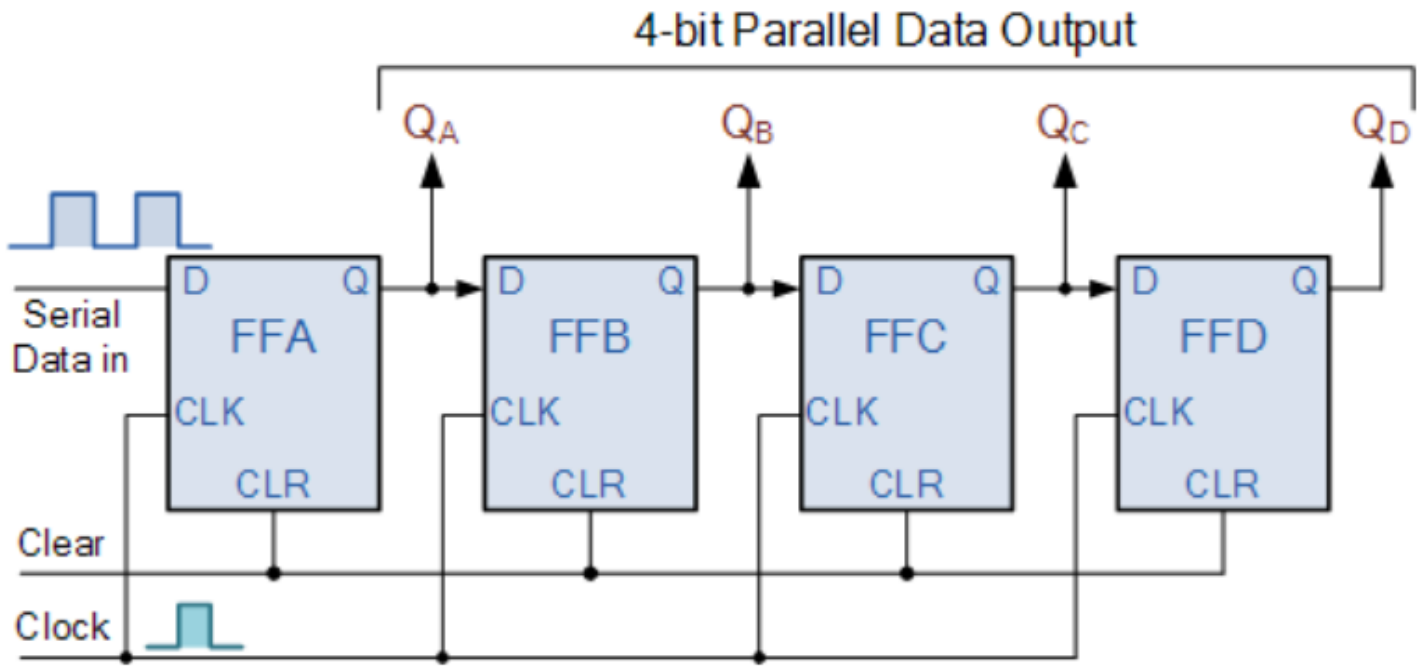
T	Q_{next}
0	Q
1	$\overline{Q}$

When T = 1, the output keeps changing Q = $\overline{Q}$ upon each clock cycle.

When T = 0, the flip-flop hold its state Q = Q.

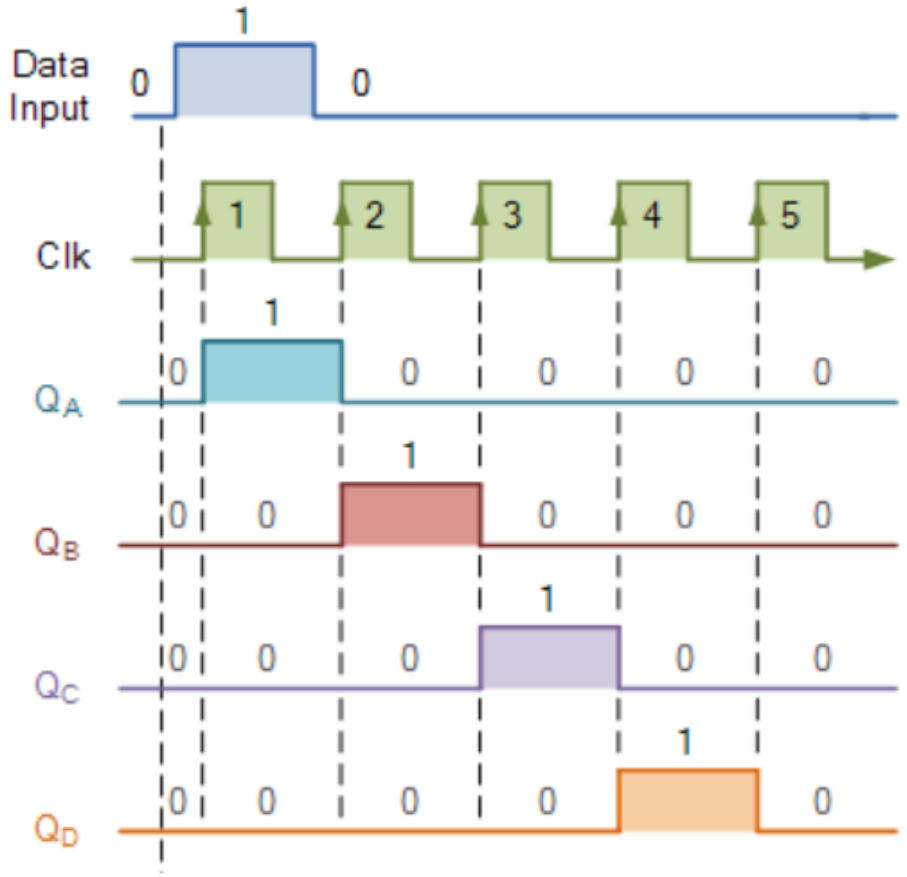

Parallel Data Output
Q_3
Q_2
Q_1
Q_0
MSB
LSB
Serial Data Input
D
1-bit
1-bit
1-bit
1-bit
Q
Serial Data Output
MSB
LSB
D_3
D_2
D_1
D_0
Parallel Data Input

4 bit-serial-in Parallel-Out (SIPO) Shift Register

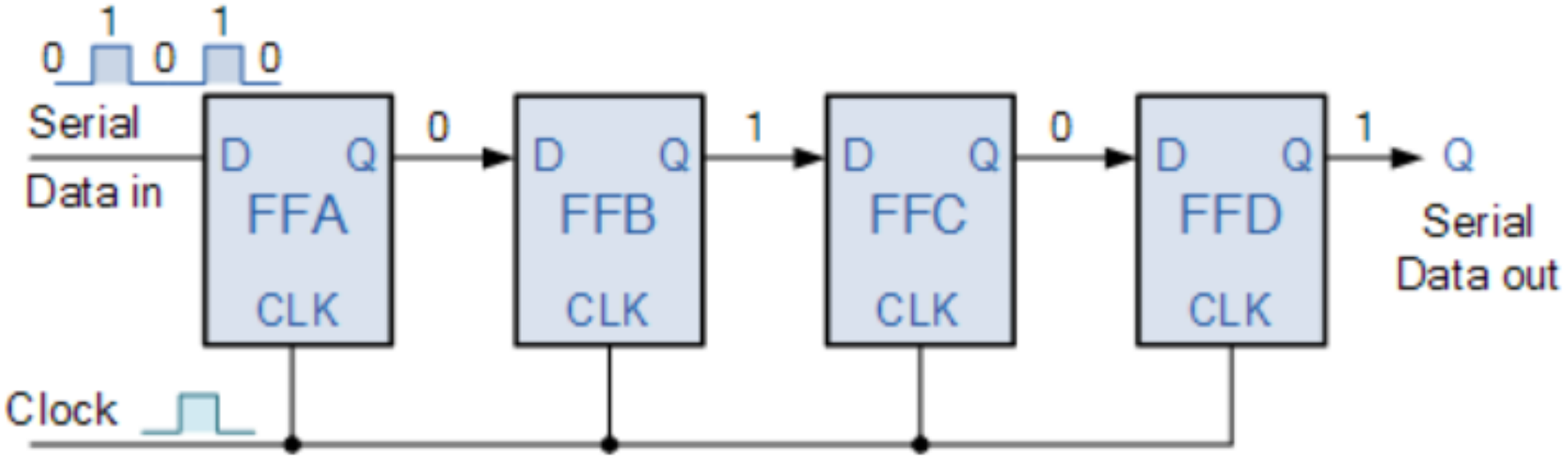


4 bit-serial in Parallel Out (SIPO) Shift Register

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

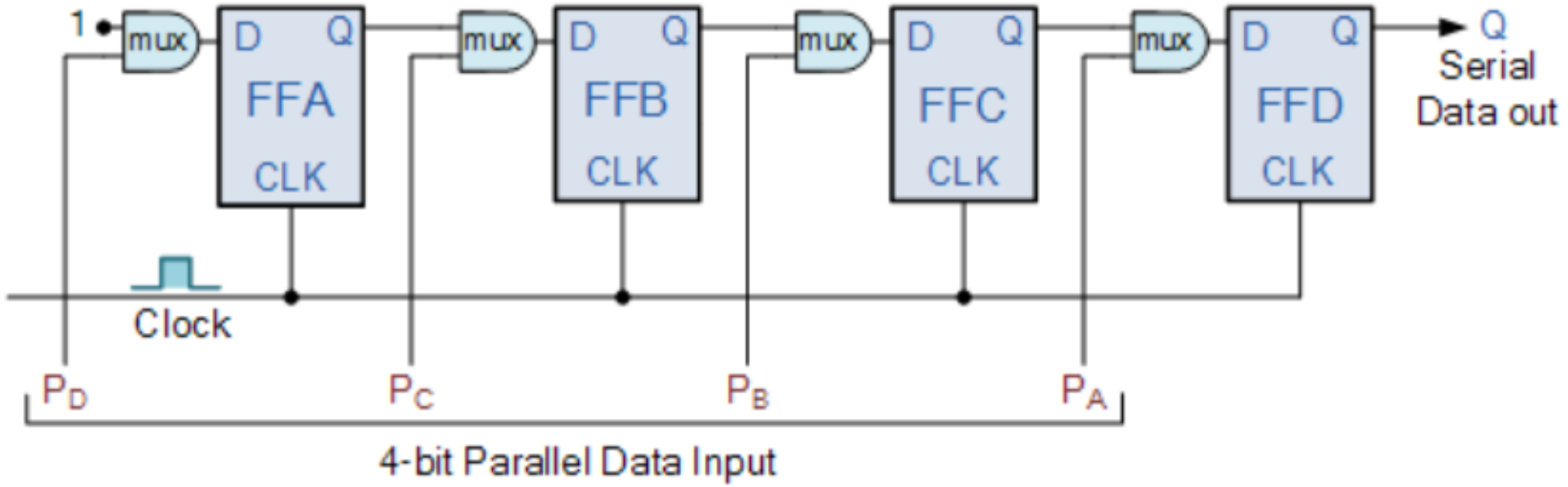


4-bit Serial-in to Serial-out Shift Register

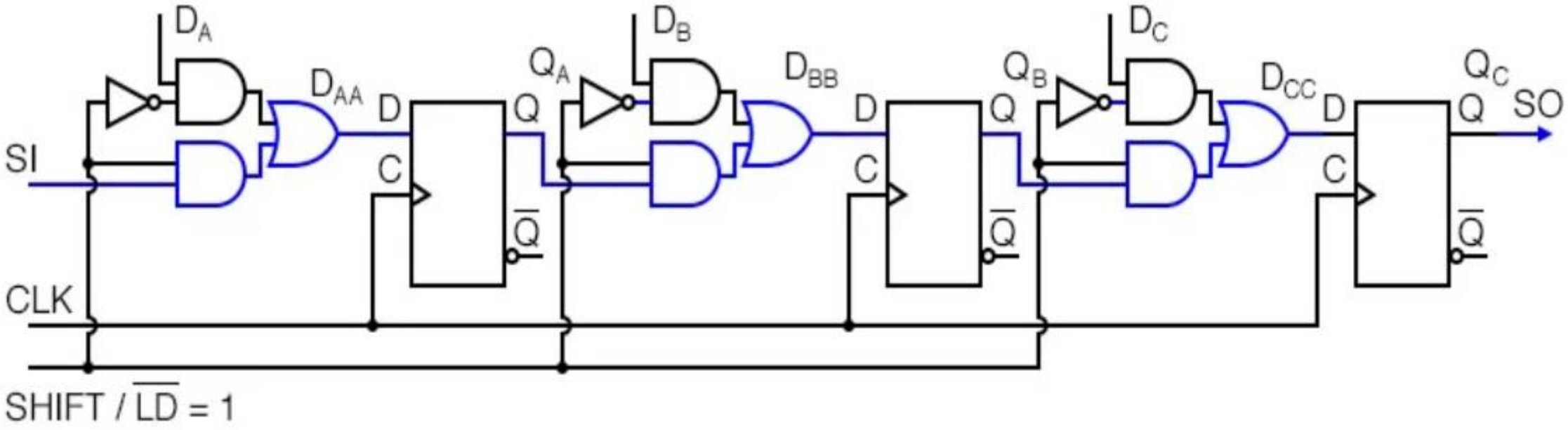


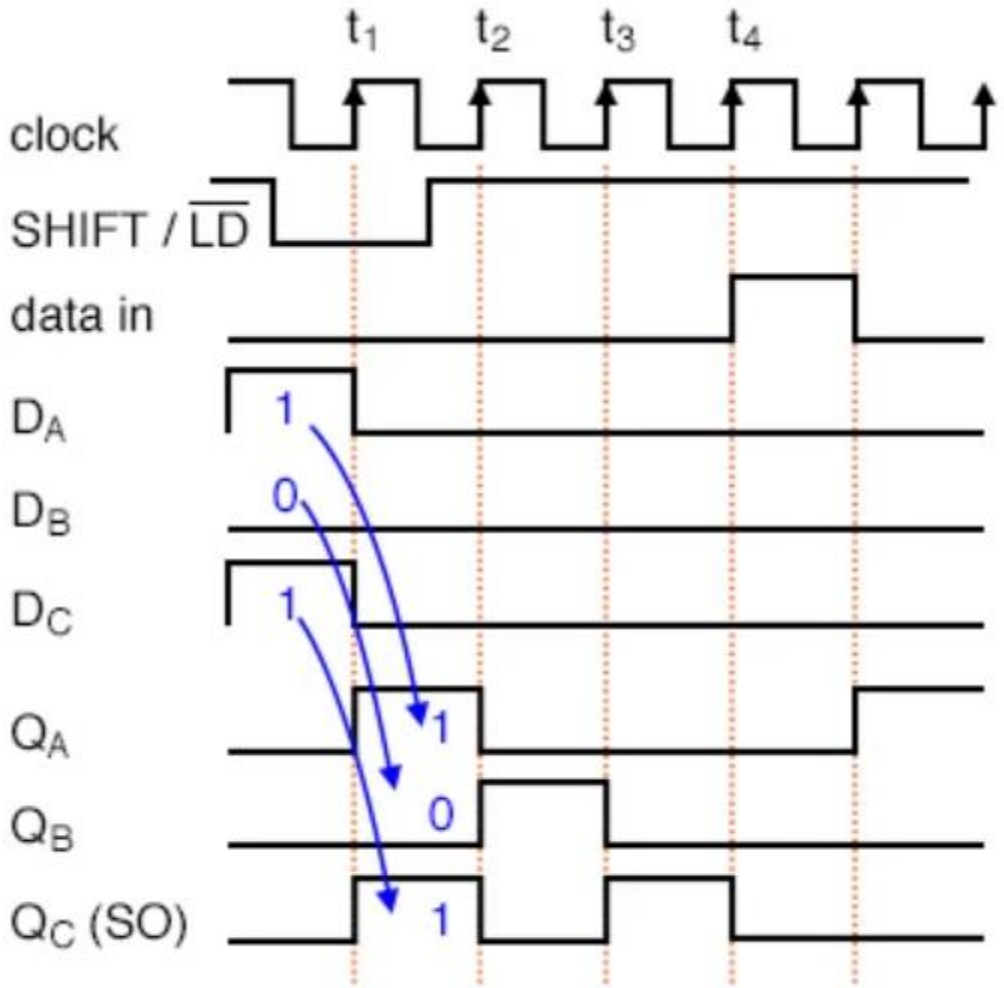
This type of **Shift Register** also acts as a temporary storage device or it can act as a time delay device for the data

4-bit Parallel-in to Serial-out Shift Register



4-bit Parallel-in to Serial-out Shift Register





Parallel-in/ serial-out shift register load/ shift waveforms

4-bit Parallel-in to Parallel-out Shift Register