Part A

1. **MAR**- register contains the data to be written into or read from a addressed location
2. A **BUS** is a communication pathway connecting two or more devices
3. The acronym SCSI stands for-**Small Computer System Interface**
4. Name any four input devices-**KEYBOARD,MOUSE,SCANNER,JOYSTICK**
5. The individual control word in the micro routine is referred as **Microinstructions**
6. A program counter(PC) is defined as------- **which has the address of the next instruction to be executed from memory**
7. Pentium processor uses ---**Superscalar architecture**------and hence can issue multiple Instructions per cycle
8. List any 2 application of Multicore Processors-
    a. **3D gaming**
    b. **Video altering**
9. Name general purpose registers of 8086 -general-purpose registers **AX, BX, CX and DX**.
   (AH, AL; BH, BL; CL, CH and DL, DH.)

Part B

1. List memory hierarchy with respect to speed, size and cost
   REFER NOTE:Draw the memory hierarchy diagram and write down short notes and add these key points

   In terms of Speed

   Internal Memory > Cache Memory > Main Memory > Secondary Memory

   In terms of Cost

   Internal Memory > Cache Memory > Main Memory > Secondary Memory

   In terms of Capacity

   Internal Memory < Cache Memory < Main Memory < Secondary Memory

2. Illustrate connection of memory to the processor

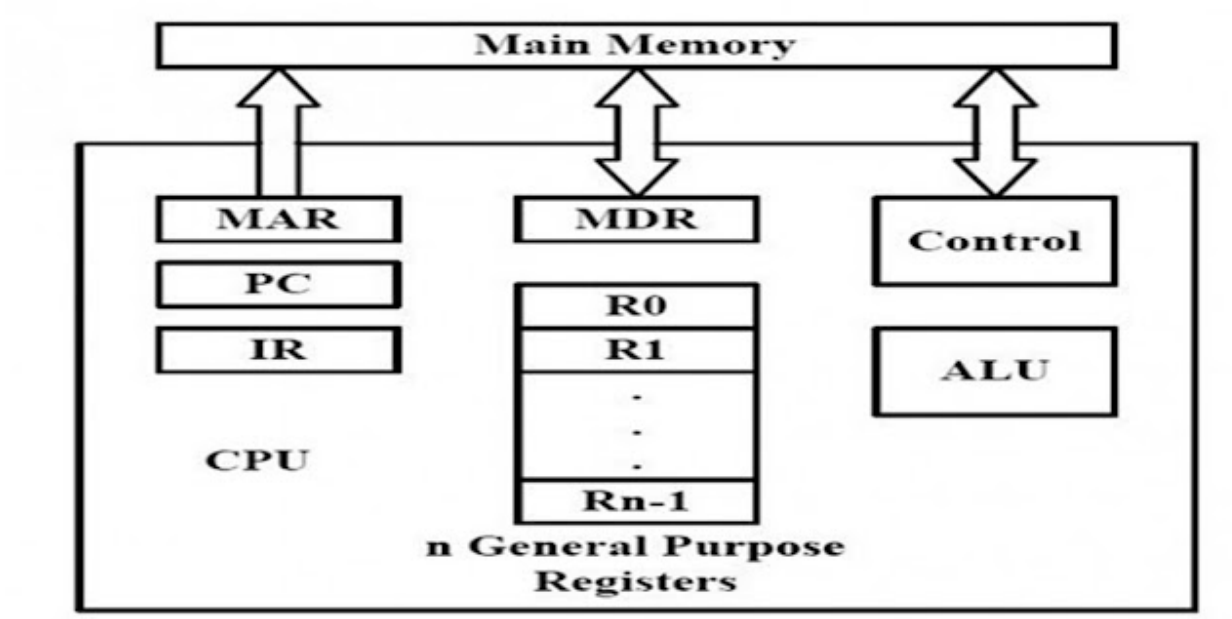


Figure: Connection between MM & Processor

i) PC: Program counter contains the memory address of the instruction to be executed.

(ii) MAR: Memory address register holds the address of the location to or from which data are to be transferred.

(iii) MDR: Memory data register contains the data to be written or read out of the address location.

(iv)IR: The instruction register contains the instruction that is being executed.

(v)ALU: ALU is the part of the computer which performs different basic operation and arithmetic calculations.

3. List the features of PCI
   - ➡It uses 64 bit addressing scheme.
   - ➡It works on synchronous bus architecture.
   - ➡It supports linear burst mode data transfer.
   - ➡It offers large bandwidth and higher speed.
   - ➡It supports full bus mastering.
   - ➡It supports plug and play.

➡PCI uses shared bus topology in order to allow for communication among different devices on the single bus. Once a device becomes master, it can use PCI bus to communicate with CPU or memory.

4. Define DMA and list the 3 registers in a DMA controller for data transfer operation
   REFER NOTE: write down note on DMA and add these points

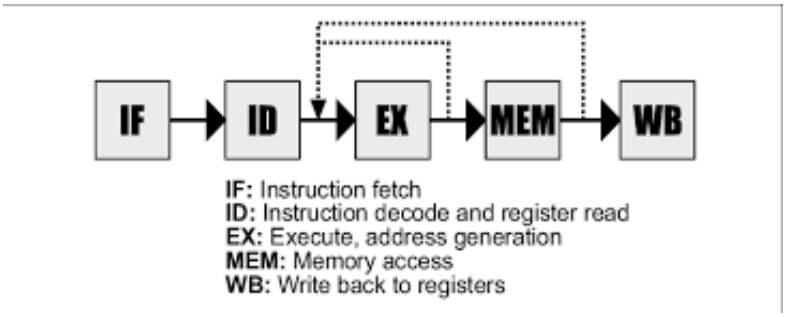
   The DMA controller has three registers as follows.

   Address register – It contains the address to specify the desired location in memory.

   Word count register – It contains the number of words to be transferred.

   Control register – It specifies the transfer mode.

5. Draw the sequence of 4 stage pipeline



   Stage 1 (Instruction Fetch) In this stage the CPU reads instructions from the address in the memory whose value is present in the program counter.
   Stage 2 (Instruction Decode) In this stage, instruction is decoded and the register file is accessed to get the values from the registers used in the instruction.
   Stage 3 (Instruction Execute) In this stage, ALU operations are performed.
   Stage 4 (Memory Access) In this stage, memory operands are read and written from/to the memory that is present in the instruction.
   Stage 5 (Write Back) In this stage, computed/fetched value is written back to the register present in the instructions.

6. write 3 action sequence need to execute the instruction MOV [R2],R1
   - MAR <=[R2]
   - Start a read operation on the memory bus & wait for WFC response

- Load MDR from the memory bus,R2<=[MDR]

7. List and define basic functional registers in the processor

REFER NOTE:-SHORT NOTE ON IR,PC,MAR,MDR ETC

8. Give the names of segment registers of 8086
   - 8086 addresses a segmented memory
   - Complete I MB memory is divided into 16 logical segments,
   - each of 64 KB.
   - There are 4 segment registers: Code Segment (CS), Data Segment (DS), Extra Segment (ES) and Stack Segment (SS).
   - Segment Registers hold the offset address of the respective
   - segments.

   CS, *code segment:* Machine instructions exist at some offset into a code segment. The segment address of the code segment of the currently executing instruction is contained in CS.

   DS, *data segment:* Variables and other data exist at some offset into a data segment. There may be many data segments, but the CPU may only use one at a time, by placing the segment address of that segment in register DS.

   SS, *stack segment:* The stack is a very important component of the CPU used for temporary storage of data and addresses. Therefore, *the stack has a segment address*, which is contained in register SS.

   ES, *extra segment:* The extra segment is exactly that: a spare segment that may be used for specifying a location in memory.

9. Describe Role of Microprocessor in Micro Computer

   A microprocessor is a computer processor which incorporates the functions of a computer's central processing unit (CPU) on a single integrated circuit (IC), or at most a few integrated circuits
   The microprocessor is a multipurpose, clock driven, register based, digital-integrated circuit which accepts binary data as input, processes it according to instructions stored in its memory, and provides results as output. Microprocessors contain both combinational logic and sequential digital logic. Microprocessors operate on numbers and symbols represented in the binary numeral system.

10. List any 3 features of Multicore Processors

    It is capable to perform more tasks compare to single core processors.
    ● It plays best performance for multi thread applications.
    ● It can perform multiple works in simultaneous with using of low frequency.
    ● It is able to process huge data compare to single core processor.

- Low consumption of energy while completing multiple tasks at a same time
- It uses Instruction level parallelism.
- It is supported by Moore’s law.
- Higher speed while using of small circuit
- Lesser capacitance

PART C