HDL Concepts

* Area vs latency
* Behavioral vs structural
* Structural, hierarchical, architectural, behavioral
* Testbench vs DUT vs hardware targeting
* Breadboard vs HDL
* Processor vs FPGA execution speeds
* Combinational vs synchronous
* Concurrent vs sequential
  + All statements in a process are sequential
* Register transfer level [RTL] high level design flow
* Event driven simulation
* Generates
* Asserts
* Generics
* Data Types

Worked Problems

* RTL ⬄ Block Diagram ⬄ Waveform
* Variables vs Signals

Engineering Concepts

* Version control
* No tabs
* Naming conventions

HDL Code Samples

* generic\_counter
* four\_paradigmns
* concurrency
* prop\_delay
* sensivitity
* edge\_detector
* variable\_demo
* synchronizer
* rising\_edge\_synchronizer
* falling\_edge\_synchronizer