Digital Design Lab

ECE 315

Lab/Project 2

Seven Segment Display

Group # 9

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Overview

Purpose of this lab is to design a circuit that generates the numbers from 0 to 9 on a display. The circuit will be designed using Quartus Prime and then uploading it to a DE1 board making sure all the pins are set up accordingly and using the switches on the board to generate the appropriate numbers. This is our first lab using quartus prime and the De1-SoC board, so it is meant to familiarize ourselves with how to use the program, and how to download our project and use the board.

Equipment

Tool	Quantity
Quartus Prime	1
DE1-SoC FPGA Board	1

Description

In order to implement a 7 segment display circuit, the first step is to create a decoder that is able to translate 4 binary inputs into 7 distinct outputs. To do this we created a truth table that mapped each input in binary to its corresponding 7 segment display pattern. Once that was finished, we created k-maps for each output in order to reduce the circuit complexity. Next we had to simulate the boolean functions on Quartus Prime. To do so we used the schematics provided by Quartus Prime to draw out the circuit and then use their simulation function to test the circuit. Once any errors or bugs were fixed the program was downloaded onto the DE1-SoC FPGA Board and implemented.

Design Synthesis

Truth Table:

	Input $x_3x_2x_1x_0$	Display D_0 D_1 D_2 D_3 D_4 D_5D_6
0	0 0 0 0	0 0 0 0 0 0 1
1	0 0 0 1	1 0 0 1 1 1 1
2	0 0 1 0	0 0 1 0 0 1 0
3	0 0 1 1	0 0 0 0 1 1 0
4	0 1 0 0	1 0 0 1 1 0 0
5	0 1 0 1	0 1 0 0 1 0 0
6	0 1 1 0	0 1 0 0 0 0 0
7	0 1 1 1	0 0 0 1 1 1 1
8	1 0 0 0	0 0 0 0 0 0 0
9	1 0 0 1	0 0 0 0 1 0 0
10	1 0 1 0	X X X X X X X
11	1 0 1 1	X X X X X X X
12	1 1 0 0	X X X X X X X
13	1 1 0 1	X X X X X X X
14	1 1 1 0	X X X X X X X
15	1 1 1 1	X X X X X X X

K-Maps: (‘ = complement)

D_0: $x_1x_0\backslash x_3x_2$	00	01	11	10
00	0	1	x	0
01	1	0	x	0
11	0	0	x	x
10	0	0	x	x

$D_0 = x_2x_1’x_0’ + x_3’x_2’x_1’x_0$

D_1: $x_1x_0\backslash x_3x_2$	00	01	11	10
00	0	0	x	0
01	0	1	x	0
11	0	0	x	x
10	0	1	x	x

$D_1 = x_2x_1x_0’ + x_2x_1’x_0$

D_2: $x_1x_0 \backslash x_3x_2$	00	01	11	10
00	0	0	x	0
01	0	0	x	0
11	0	0	x	x
10	1	0	x	x

$D_2 = x_2'x_1x_0'$

D_3: $x_1x_0 \backslash x_3x_2$	00	01	11	10
00	0	1	x	0
01	1	0	x	0
11	0	1	x	x
10	0	0	x	x

$D_3 = x_2x_1'x_0' + x_2x_1x_0 + x_3'x_2'x_1'x_0$

D_4: $x_1x_0 \backslash x_3x_2$	00	01	11	10
00	0	1	x	0
01	1	1	x	1
11	1	1	x	x
10	0	0	x	x

$D_4 = x_2x_1' + x_0$

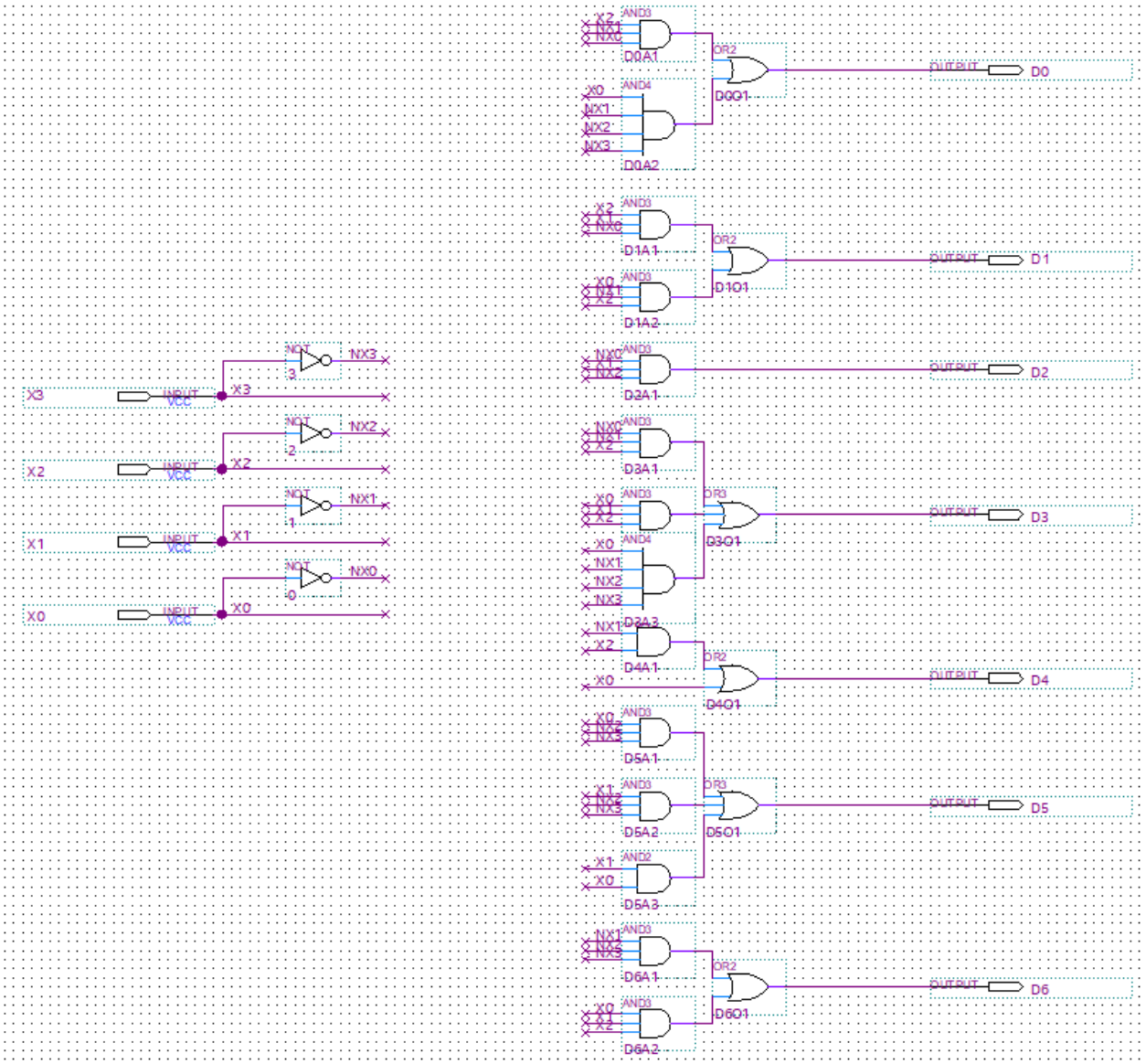
D_5: $x_1x_0 \backslash x_3x_2$	00	01	11	10
00	0	0	x	0
01	1	0	x	0
11	1	1	x	x
10	1	0	x	x

$D_5 = x_3'x_2'x_0 + x_3'x_2'x_1 + x_1x_0$

D_6: $x_1x_0\backslash x_3x_2$	00	01	11	10
00	1	0	x	0
01	1	0	x	0
11	0	1	x	x
10	0	0	x	x

$D_6 = x_3'x_2'x_1' + x_2x_1x_0$

Complete Logic Diagram



Results and Simulations

7 Segment Display Video

Conclusion

As a result, this lab allowed us to better understand the Quartus Prime software and its connections with the De1-SoC Board. It allowed us to further solidify our understanding of boolean logic through the errors and corrections made while creating the circuit. This lab successfully shows how to implement a seven segment display using Quartus Prime and the DE1-SoC FPGA Board.