Digital Design Lab

ECE 315

Lab/Project 4

4 Bit Adder/Subtractor

Group # 6

Alex Smith, Gunter Weisenber, Brandon Rubio, Richard Chin

Zeinab Ramezani, TA

University of Miami

3/7/22

Overview

The purpose of this lab is to further build upon our previous projects and our accumulated knowledge from these projects. The focus of this one is to implement a full 4-bit adder/subtractor to multiple seven segment displays, as our value can reach up to +/- 15, on the DE1-SoC board. The 4-bit circuit has already been designed and implemented in Quartus Prime in the previous lab, therefore all that was needed was to set up the displays on the DE1 board accordingly to display decimal numbers. The idea was not to only output a value, but one that was calculated from simple addition of two numbers that can either be positive or negative.

Equipment

Tool	**Quantity**
Quartus Prime (Pin planner, symbols/blocks)	1
De1-soc board	1

Description

The primary focus of this lab is to create a 4 bit adder / subtractor that displays its results onto multiple seven segment displays using the DE1-SoC board. To do this we need to incorporate a BCD (Binary Coded Decimal) circuit into our 4 bit adder / subtractor from our previous lab. Ultimately the BCD circuit is implementing an 8 bit Shift add 3 algorithm which performs the following: 1. Shifts left one to the binary input, 2. Adds 3 to the BCD if it's greater than 4, 3. Go to 1. As a result the BCD can be created by connecting seven Add 3 circuits in tandem. The truth table and the K-maps for the Add 3 circuit are provided in the Design Synthesis portion of the report. Once the Add 3 circuits were connected correctly the BCD was completed and is capable of converting an 8 bit input into decimal. However for this design, the four most significant inputs of the BCD were set to 0 as our adder subtractor can only take 4 bits. Now once the BCD was complete we needed to implement a Sign Display and a Magnitude Display Circuit. The Sign Display circuit was simply created by setting each segment on the led display to Vcc except for S_6, which outputs the inverse of the sign bit from our 4 bit adder/subtractor. Then, the Magnitude Display circuit was created by using a copy of our 4 bit adder/subtractor with the initial carry bit set to one. Finally once these circuits were built we took

our display circuit from lab 2 and connected the circuit accordingly. The final schematic can be seen in the “Complete Logic Diagram” portion of the report.

Extra Credit: Much like the implemented subtractor, allowing the other set of input to be negative required another set of four 2:1 MUXs as well as another select line along with a basic 4-bit adder to convert from one’s complement to two’s complement.

Design Synthesis

Truth Table: Add 3 Circuit

Input	Output
$X_3X_2X_1X_0$	$P_3P_2P_1P_0$
0000	0000
0001	0001
0010	0010
0011	0011
0100	0100
0101	1000
0110	1001
0111	1010
1000	1011
1001	1100
1010	xxxx
1011	xxxx
1100	xxxx
1101	xxxx
1110	xxxx
1111	xxxx

K-Maps: (‘ = complement)

P_3: $x_1x_0\backslash x_3x_2$	00	01	11	10
00	0	0	x	1
01	0	1	x	1
11	0	1	x	x
10	0	1	x	x

$P_3 = x_3 + x_2x_1 + x_2x_0$

P_2: $x_1x_0\backslash x_3x_2$	00	01	11	10
00	0	1	x	0
01	0	0	x	1
11	0	0	x	x
10	0	0	x	x

$P_2 = x_3x_0 + x_2x_1’x_0’$

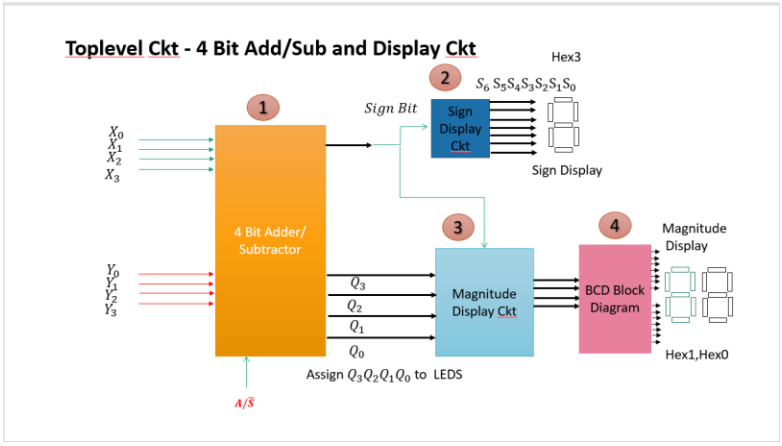
P_1: $x_1x_0\backslash x_3x_2$	00	01	11	10
00	0	0	x	1
01	0	0	x	0
11	1	1	x	x
10	1	0	x	x

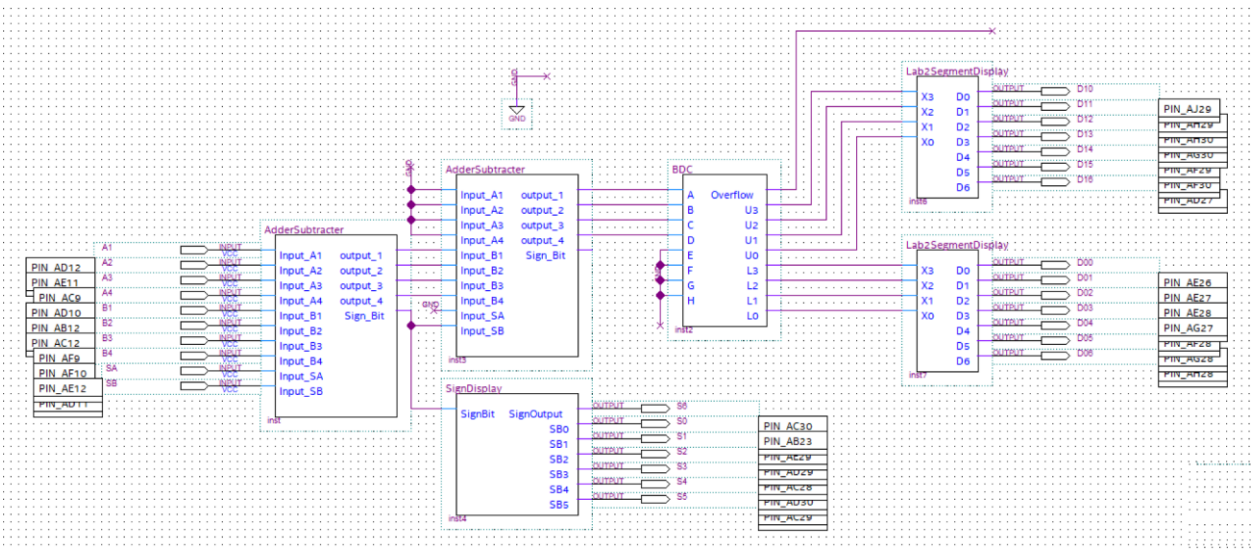
$P_1 = x_1x_0 + x_3’x_2’x_1 + x_3x_1’x_0’$

P_0: $x_1x_0\backslash x_3x_2$	00	01	11	10
00	0	0	x	1
01	1	0	x	0
11	1	0	x	x
10	0	1	x	x

$P_0 = x_3x_0’ + x_3’x_2’x_0 + x_2x_1x_0’$

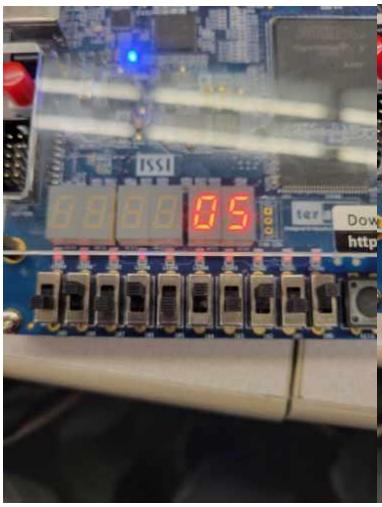
Complete Logic Diagram



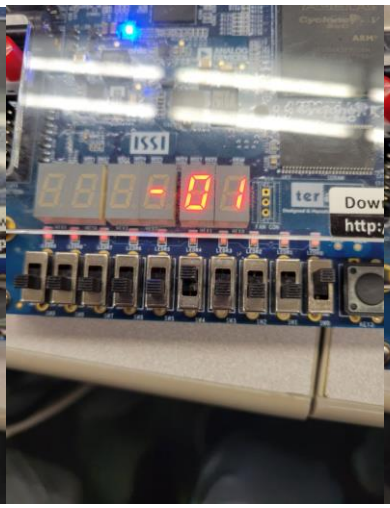


Results and Simulations:

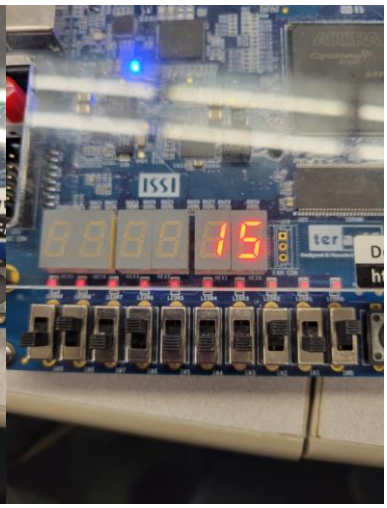
Switches from left to right: $A_{Sign\ Bit}$, A_3 , A_2 , A_1 , A_0 , $B_{Sign\ Bit}$, B_3 , B_2 , B_1 , B_0 *(A_3 and B_3 most significant)*



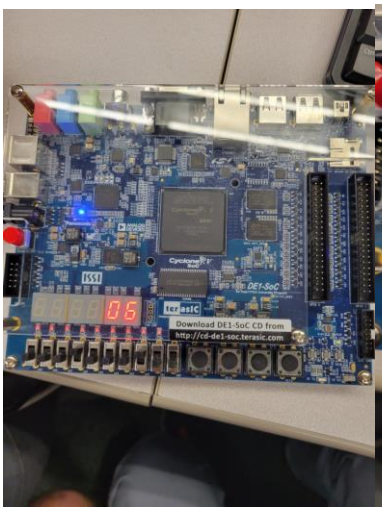
1. (10 - 5 = 5)



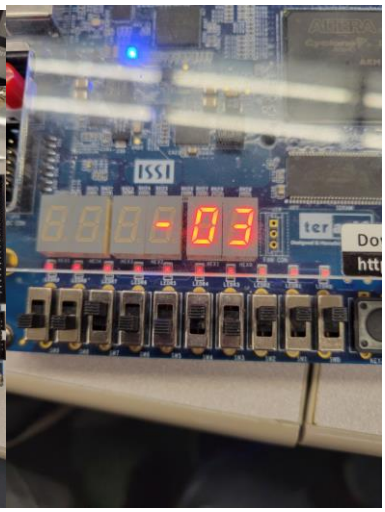
2. (0 - 1 = -1)



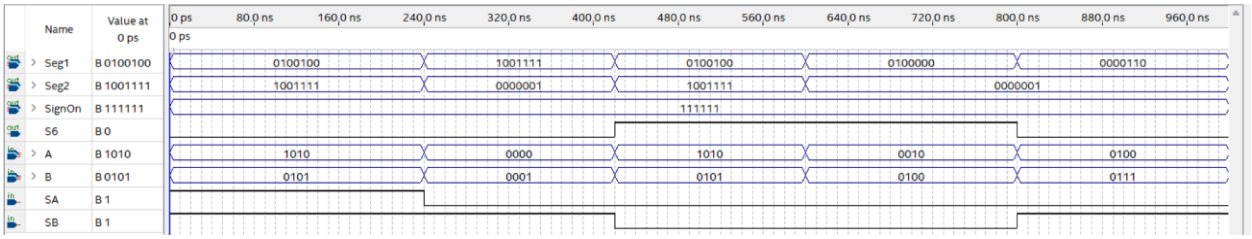
3. (10 + 5 = 15)



4. (2 + 4 = 6)



5. (4 - 7 = -3)



The first section represents (*-10 - 5 = -15*), the rest corresponds to 2 -> 5 of the above images.

Conclusion

In the end, we designed and built a simple four bit adder that was capable of adding two positive numbers, two negative numbers, or one positive and one negative number (regardless of the order of the numbers). Then, this adder was loaded onto the DE1-SoC board and was represented on the display. Design and implementation went relatively smoothly, with the trickiest bit being the circuits required to interpret numbers on the display. The final design can add or subtract any two four-bit numbers, positive or negative, with the only limitation being that the result of the addition has to also be a four-bit number, otherwise there is an overflow. This lab was a good experience in designing practical adders; it required an understanding of the DE1-SoC board and how to display numbers on a BCD display. It was the first step in designing circuits that could be by anyone, not just those that designed it.

*LAB 4: **A 4 Bit Adder/Subtractor***

& Seven Segment Display and BCD Circuit

Student Group Number: 6

Student Name	Student C #	Contribution	Signature
Gunti Weissenbacher	C12175610		
Alex Smith	C23717443		
Brandon Rubio	C23727769		
Richard Chin	C23709160		

To Be Submitted:

- ☐ Final circuit performs the addition and subtraction on the decimal numbers (Max decimal number 15).
- ☐ Display and BCD Circuits Simulation on Quartus Prime.
- ☐ Final circuit Simulation on Quartus Prime.
- ☐ Final circuit successfully download to DE1 board.

Comments:

works with extra credit.

Sign Off Date	Sign Off Time	TA Signature
3-4-2022	11:30	