Digital Design Lab

ECE 315

Lab/Project 5

3-bit Counter and 8-bit Register

Group # 6

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Overview

This lab is a design/implementation of a 3-bit counter and an 8-bit register. Using prior knowledge and experience gained in previous labs, we produced a circuit that counts from 0 to 3, holds and then restarts the count, as long as the “load” in the register is zero. If the load is one, it stops the count. The purpose of the lab is to design a crucial element in the next lab, which is to build a multiplier, which is the last building block in developing a calculator for our final project.

Equipment

Tool	**Quantity**
DE1-SoC board	1
Quartus Prime (Schematic, Symbol, Pins)	1

Description

In order to create the 3-bit counter we created the truth table below. From there we were able to extrapolate the k-maps for the three D flip-flops and derive the input equations for the flip flops. Next, we implemented each of the counter flip-flops in Quartus Prime using the input equations. After we tested the counter and determined that it worked properly, we moved on to designing and implementing the 8-bit register.

Using the truth table from the Lab 5A powerpoint as a reference, we modified the D flip-flops to accommodate our extra “load” input. This new modified circuit included an AND gate that combined the clock and the inverse of the “load” input. This ensured that the counter would only progress if the “load” was set to zero.

Design Synthesis

Truth Table: 3-bit Counter

Present State	Next State
CBA	$C^+B^+A^+$
000	001
001	010
010	011
011	100
100	100
101	000
110	000
111	000

K-Maps: (‘ = complement)

DFF C	CB			
A	00	01	11	10
0	0	0	0	1
1	0	1	0	0

P_3 = CB’A’ + C’BA

DFF B	CB			
A	00	01	11	10
0	0	1	0	0
1	1	0	0	0

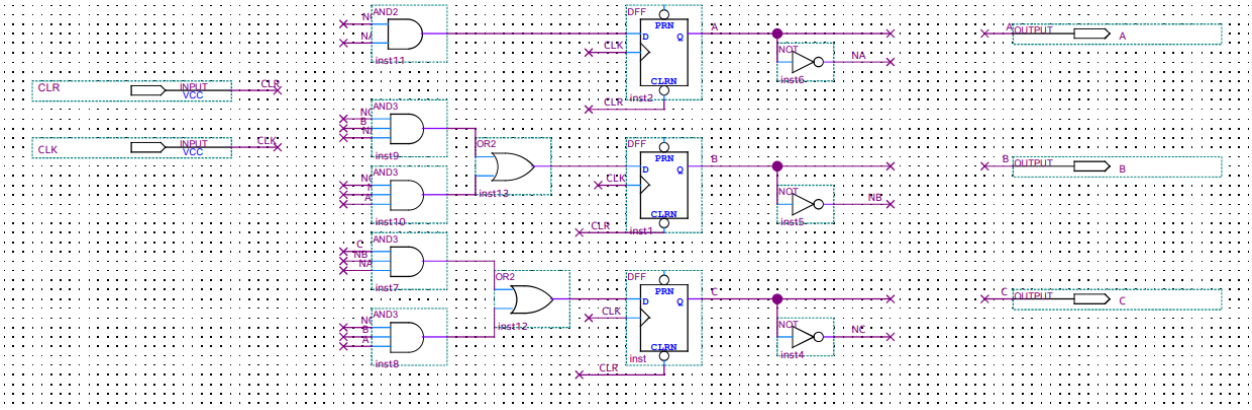
P_2 = C’BA’ + C’B’A

DFF A	CB			
A	00	01	11	10
0	1	1	0	0
1	0	0	0	0

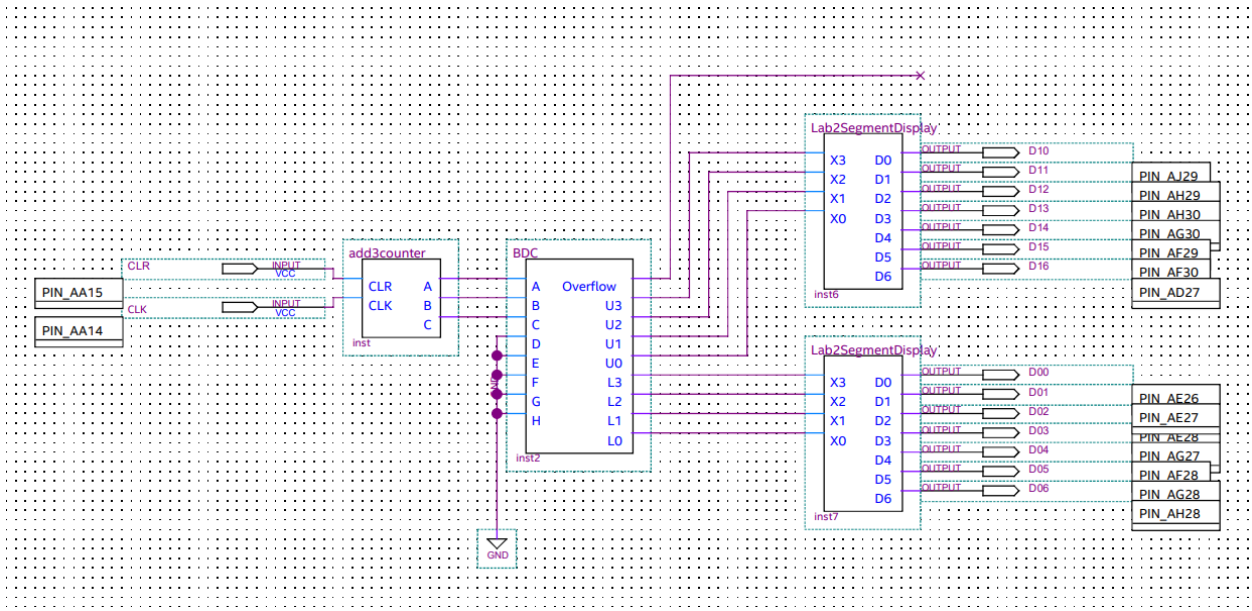
$P_1 = C'A'$

Complete Logic Diagram

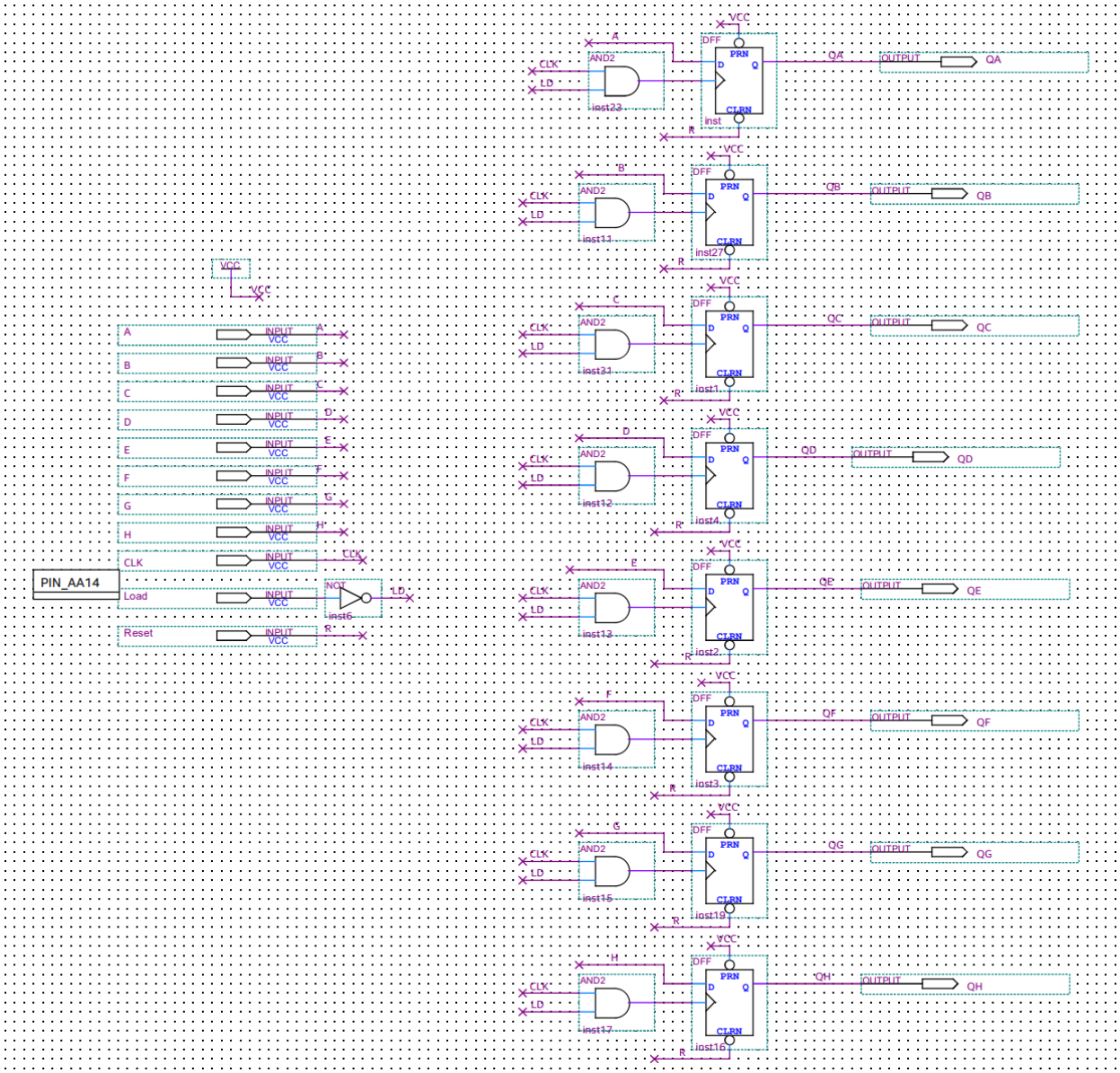
3-bit Counter (A being least significant)



3-bit Counter to Seven-Segment Display on DE1-SoC

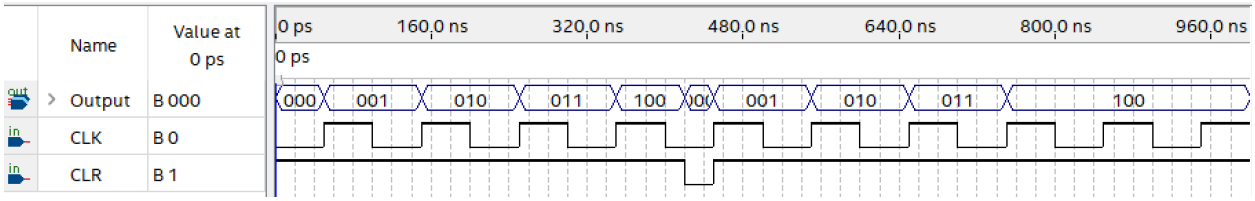


8-bit Register

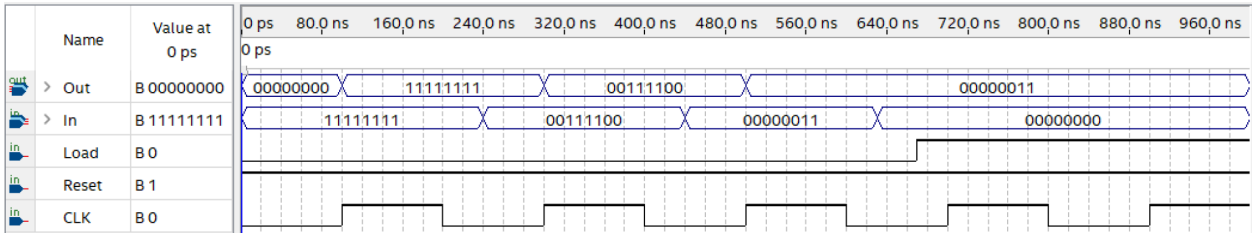


Results and Simulations:

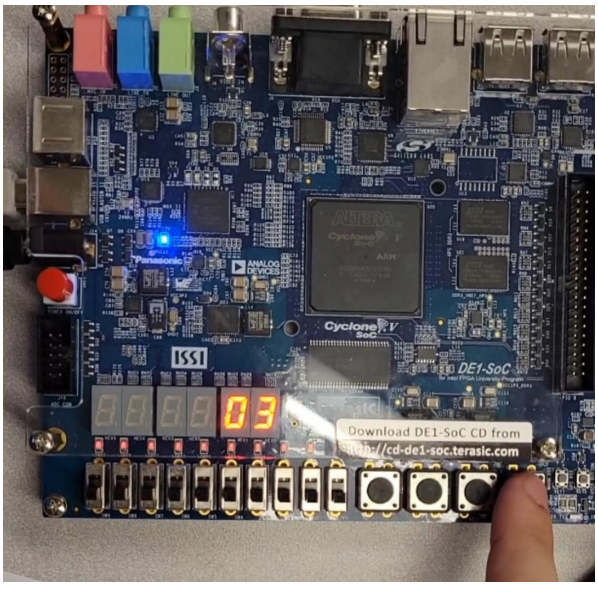
3-bit Counter Simulation



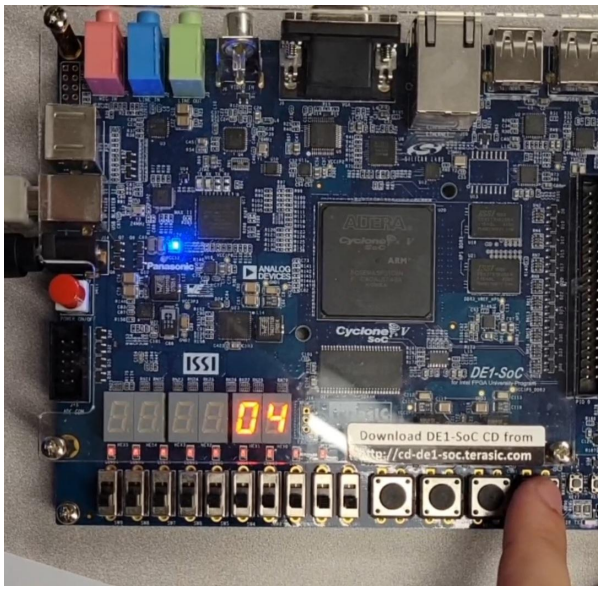
8-bit Register Simulation



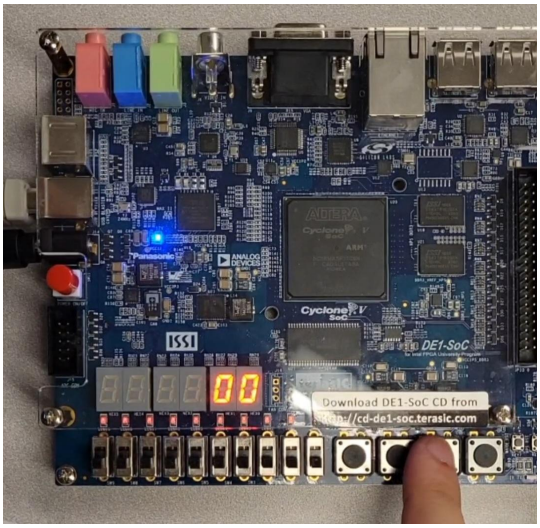
3-bit Counter (DE1-SoC Board)



Far right button (button 0) is connected to CLK



Holds counter at decimal value 4



Reset (button 1) is adjacent to CLK, will set counter to 0 once pressed

Conclusion

In this lab, our group built a simple 3-bit counter and 8-bit register. The circuit would count up from 0 to 3 if an input “Load” was set to zero. When the counter reached 3, it would hold there until a reset button was pressed. The lab was designed in Quartus Prime, and implemented on a DE1-SoC board. The design process went smoothly with minimal complications, however there was an error that took some time to fix upon running the simulation on Quartus Prime. The circuit was also impossible to test until it was loaded onto the board because the delay on the counter was not represented properly in the waveform simulation. In the end, our group overcame these issues and produced a perfectly functioning 3-bit counter that used an 8-bit register in order to increment the counter only when an input was set. This problem not only taught us how to design a counter and a register, but it also gave us a foundational building block in the next lab, which is to design a multiplier. Having learned how to design a register, designing and implementing lab 5B will be significantly easier with the knowledge gained during lab 5A.

LAB 5A: A 3 Bit Up Binary Counter, 8 bit Register

Student Group Number: 6

Student Name	Student C #	Contribution	Signature
Guntram Weissenberger	C12128510		
Brandon Rubio	C23727769		
Richard Chin	C23709160		
Alex Smith	C23717443		

To Be Submitted:

- ☐ Fully functional simulation waveform for a 3 bit up binary counter and a 8 bit register.
- ☐ Final BCD circuit running on DE1 Board.

Comments:

clock counter works

Sign Off Date	Sign Off Time	TA Signature
3-23-22	5:00	