Digital Design Lab

ECE 315

Lab/Project 3

4 Bit Adder- 4 bit subtractor

Group # 9

Alex Smith, Guntram Weisenberger, Brandon Rubio

Zeinab Ramezani, TA

University of Miami

2/28/22

Overview

The purpose of this lab is to design and implement a 4-bit adder/subtractor with he goal to be able to combine any two 4-bit numbers and either add or subtract. This will be done using quartus prime to design the circuit which includes combining four 1-bit adders with an overflow and sign bit.

Equipment

Quartus prime

Description

The first step of the lab was to implement four 1 bit adders. Each adder is made up of three inputs: bits ‘A’, ‘B’, and carry bit ‘Cin’, and 2 outputs: the sum of A and B, ‘sum’ and carry bit ‘Cout’. To implement this, a truth table is required for the adder and used to construct the k-maps that will derive our input and output equations. Once 4 of these were connected in series, this resulted in 8 inputs: A1, A2, A3, A4, B1, B2, B3, B4, 4 outputs: Q1, Q2, Q3, Q4 (most significant to least significant), and 1 carry in/output. In order to implement the 4-bit subtractor we needed to find the 2’s complement of our B input. To do this we used 4 MUX’s that would switch between B (for addition) and B complement (for subtraction). When subtraction is selected, the carry bit on the first adder is set to one in order to complete the 2’s complement for the B input.

Design Synthesis

Truth Table:

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-Maps: (‘ = complement)

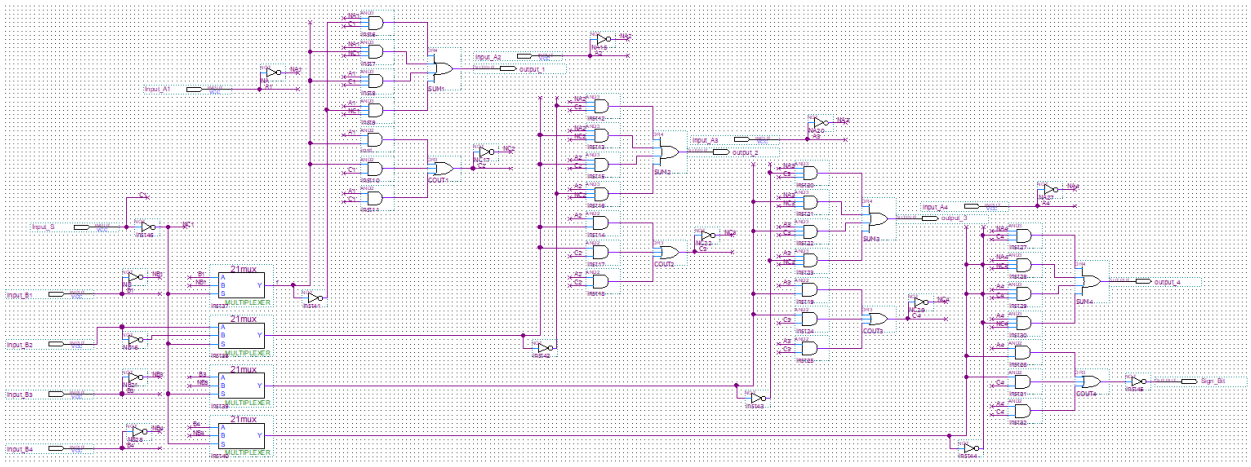
Sum: C_{in}\AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

Sum = $A'B'C_{in} + A'BC_{in}' + ABC_{in} + AB'C_{in}'$

C_{out}: C_{in}\AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$C_{out} = AB + BC_{in} + AC_{in}$

Complete Logic Diagram

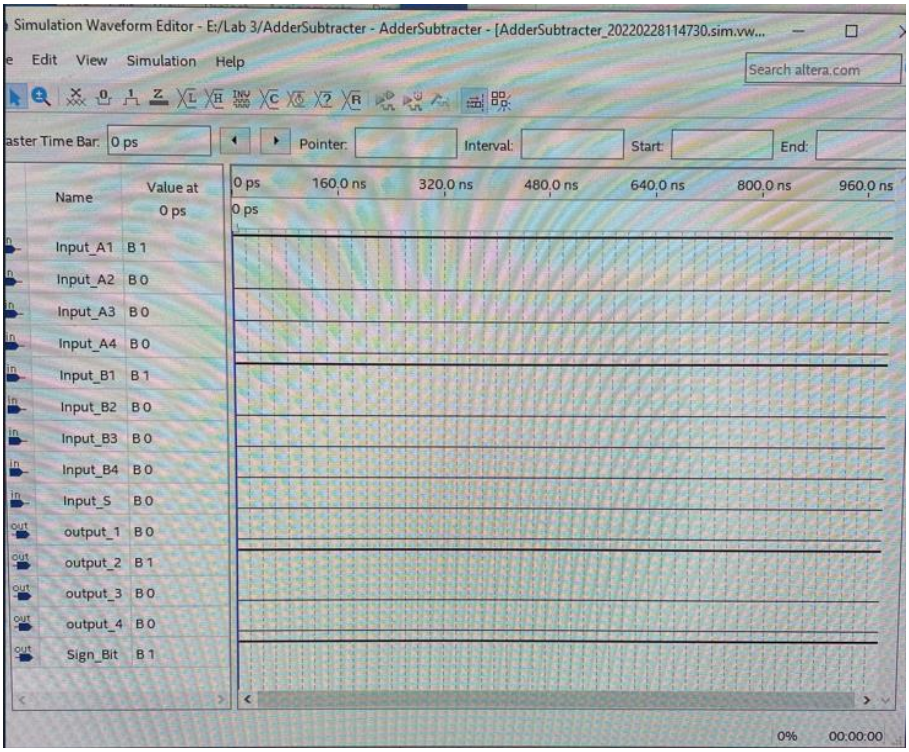


Results and Simulations

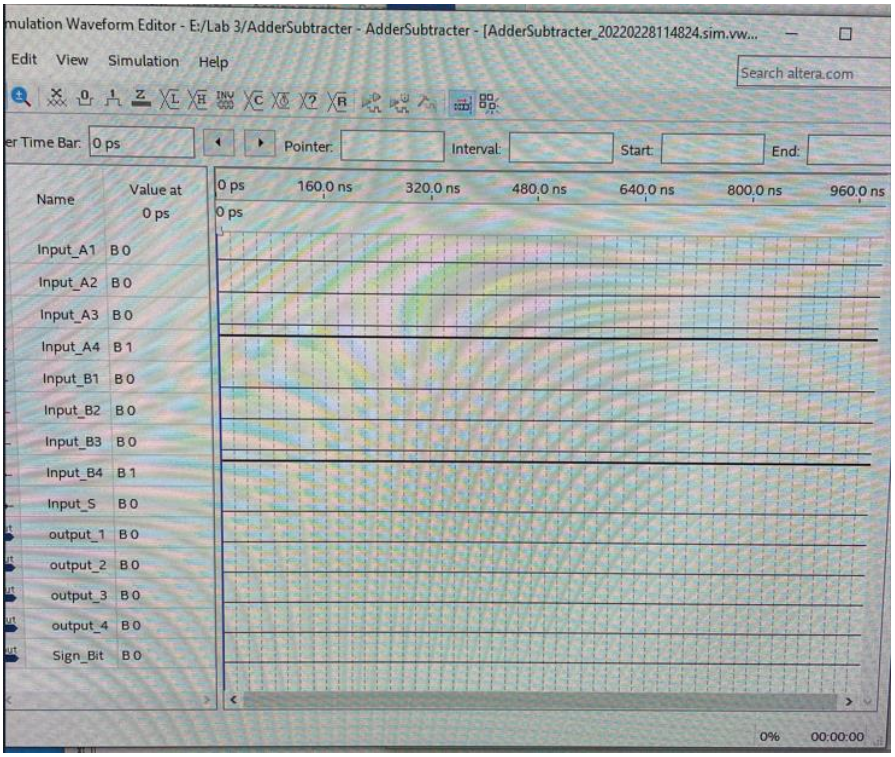
Input_A1, Input_B1, output_1 are the least significant bits

Input_S = 0 (addition), Input_S = 1 (subtraction)

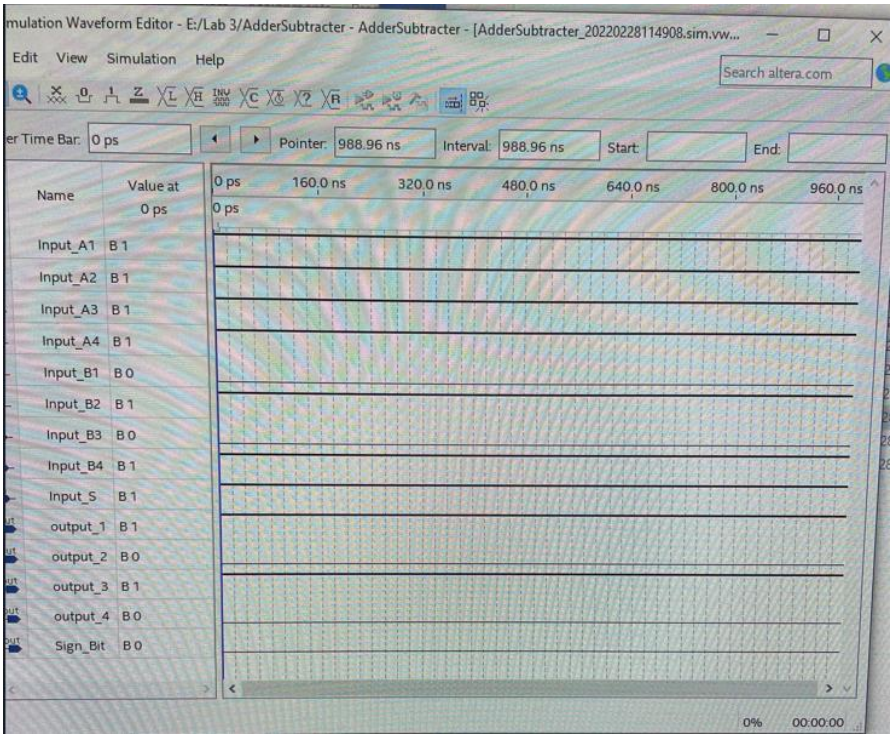
Sign_Bit = C_{out}', therefore if addition without overflow Sign_Bit = 1. Otherwise if Sign_Bit = 1 result is negative



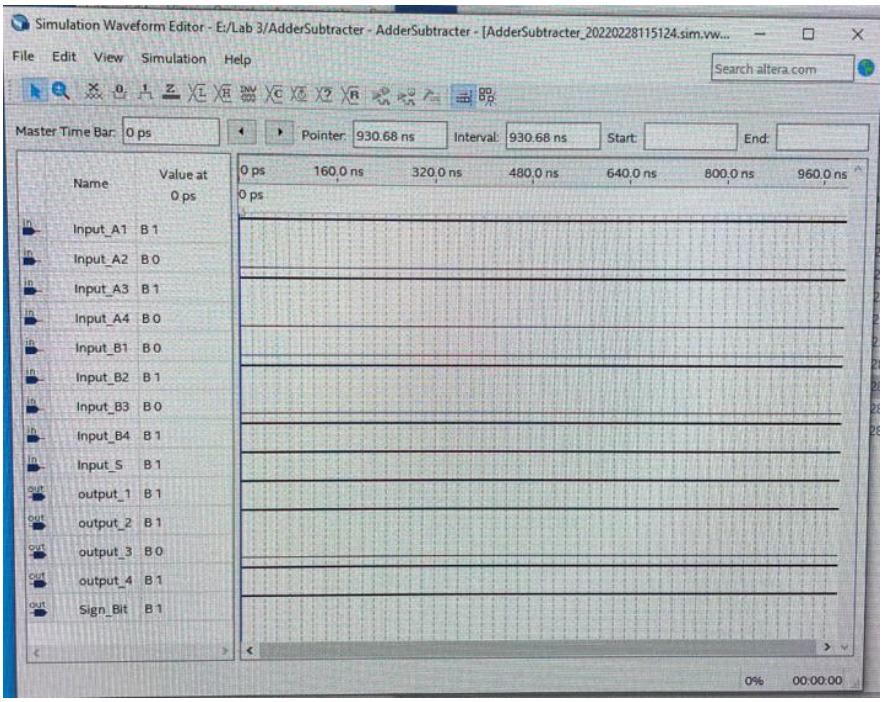
1 + 1 = 2, addition without overflow



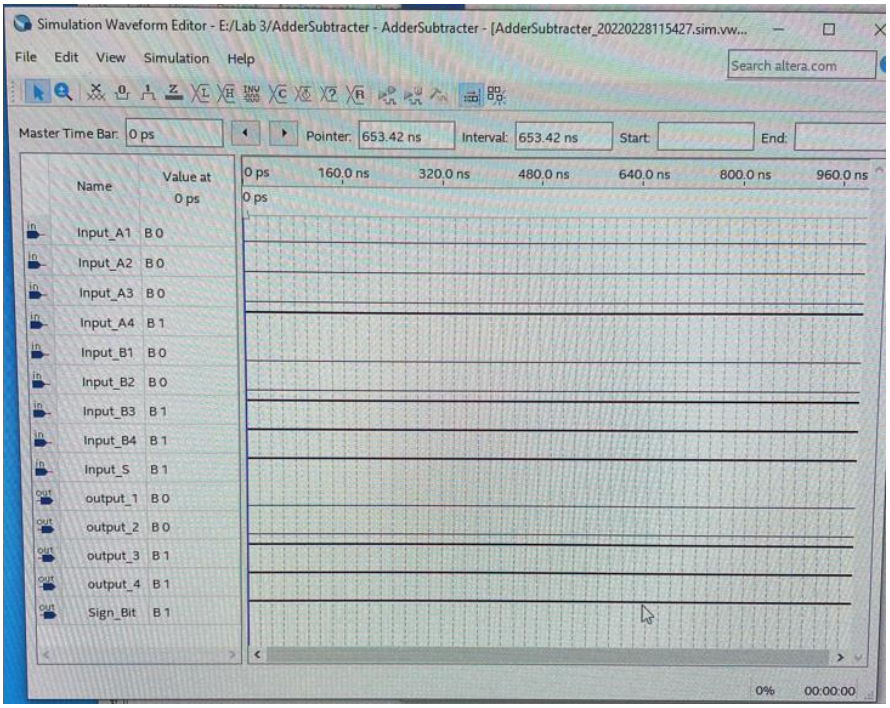
8 + 8 = 0, addition with overflow therefore Sign_Bit = 0



15 - 10 = 5, result using 2's complement is positive, therefore Sign_Bit = 0



5 - 10 = -5, result stored as 2's complement, Sign_Bit = 1 since result is negative



8-10 = -2

Conclusion

In this lab, we implemented a four bit adder in quartus prime. To do this, we implemented a one bit adder, and set them back to back in order to make a four bit adder. We also used two bit MUXes in order to allow subtraction by 2's complement. The implementation of the adders went smoothly, as all we had to do was plug in the equations for the 1-bit adders that we found, but the implementation of the MUXes was less simple. At first, we had it backwards, so that the carry bit was indicating a negative number while the bits were not flipped by the MUXes. To fix this, we had an overly complicated circuit for the S bit and the carry bit, however we simplified it down and got a functioning product. In the end, our circuit can add any two 4-bit numbers, as long as the result can be represented in 4 bits, otherwise there is an overflow. The other limitation in our design, although small, is that only the second number can be negative.

This lab was very helpful in understanding how to use k-maps and boolean equations in order to implement a physical circuit. We learned how to figure out the circuit for a simple adder/subtractor from scratch, and this information can now presumably be used to implement an adder or a subtractor of any size.

LAB 3: 4 Bit Adder-4 Bit Subtractor

Student Group Number: _____

Student Name	Student C #	Contribution	Signature
Alex S	C23717443		
Curtis	C12125610		C.W.S.
Brandon	C23727269		BR

To Be Submitted:

- ☑ Final circuit performs the addition on the decimal numbers (Max decimal number 15).
- ☑ Final circuit performs the subtraction on the decimal numbers (Max decimal number 15).
- ☑ Final Circuits Simulation on Quartus Prime.

Comments:

Sign Off Date	Sign Off Time	TA Signature
2/25/22	3:30	A Kosmack