Digital Design Lab

ECE 315

Lab/Project 5b

4 Bit Multiplier

Group # 6

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3/30/22

Overview

The purpose of this lab is to create a 4 bit multiplier using an add shift algorithm. Using circuits built from the previous labs, such as the 4-bit adder, 8 bit register and 3 bit up counter, we combined them to create the add shift algorithm. Once combined with the BCD and segment display circuits we successfully created a 4-bit multiplier on Quartus Prime and ran the simulation through the DE1-SoC Board.

Equipment

Tool	**Quantity**
DE1-SoC board	1
Quartus Prime (Schematic, Symbol, Pins)	1

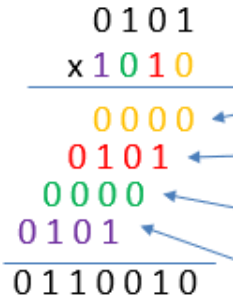
Description

To create a shift add algorithm the circuit would require our 4-bit adder and 8-bit register from previous labs. The way the algorithm works is that it takes one bit (goes from least significant to most significant) from the multiplier and multiplies it by the multiplicand. Since it's in binary if the single bit is a zero the result is a zero but if the single bit is 1 the result is just the multiplicand. The output (our result) of the 4-bit adder is composed of 4 bits and a carry bit. So in order to complete the shift aspect of our algorithm we store these 5 bits into the register (Carry bit as most significant) and then only return the four most significant bits into the adder. This will cycle through until every individual bit of the multiplier is multiplied with the multiplicand and return with an 8 bit value as the result.

Given the way this algorithm works we needed to add a few components to the circuit to make this work. First we added a four to one MUX to cycle through every bit of the multiplier which we then ANDed to our Multiplicand. Here, the output will only be one if both the multiplier bit and the corresponding multiplicand bit are both one, otherwise it outputs a zero. Next, in order to synchronize the MUX clock and the 8-bit Register clock we needed to implement our 3 bit up counter. The resulting bits of “00”, “01”, “10”, and “11” from the counter were fed into the select lines of the MUX so that it cycled through every bit of the Multiplier. Finally, we combined the resulting Multiplier circuit with our previous BCD and led segment

display circuits as well as a clock and reset input to create a 4-bit multiplier that displays its result onto the De1-SoC. We then mapped the button and pin assignments of the De1-SoC board in Quartus Prime and proceeded to run the simulation on the board.

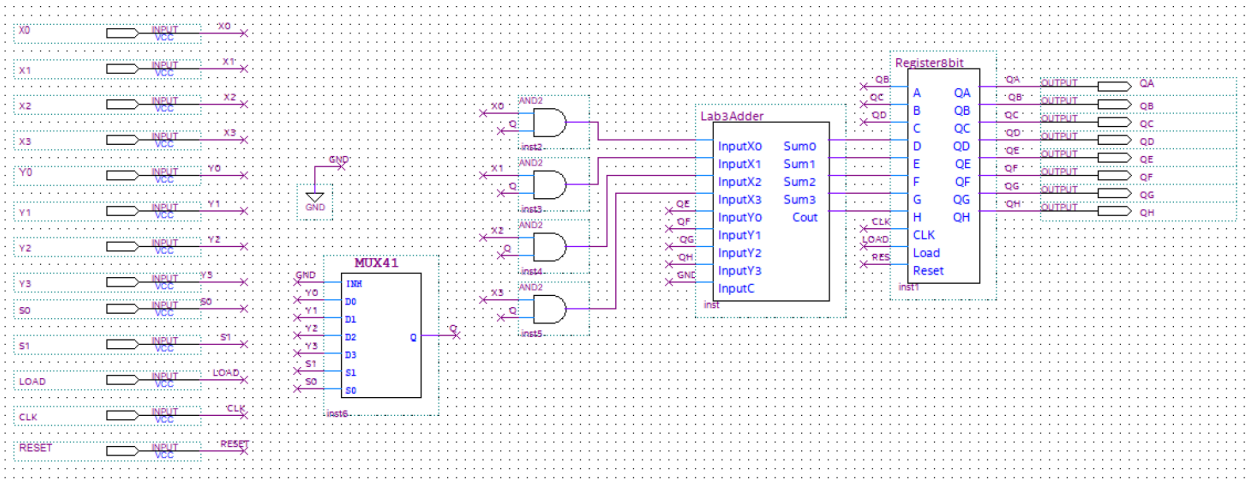
Design Synthesis



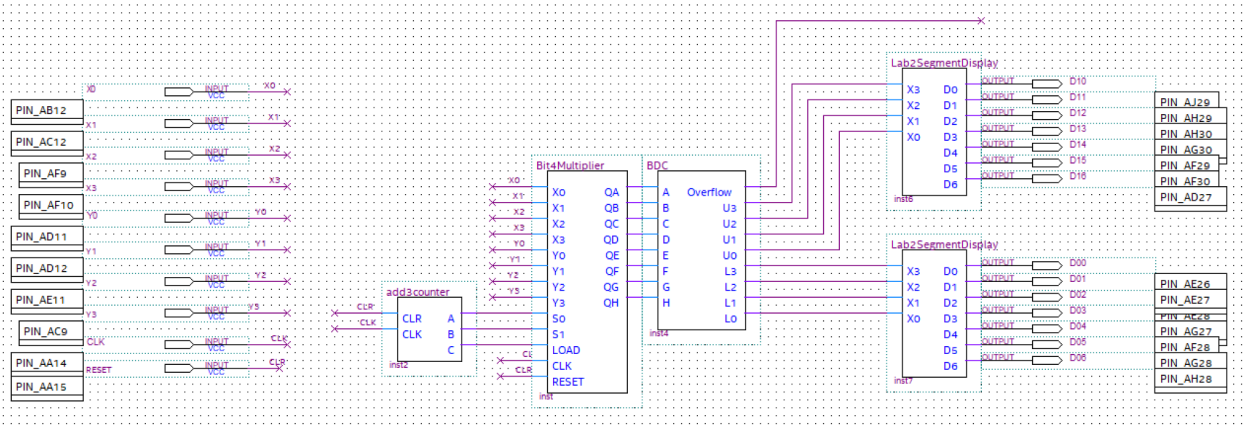
	H	G	F	E	D	C	B	A
Initialize Z	0	0	0	0	0	0	0	0
X and Y0	0	0	0	0				
Z + (X and Y0)	0	0	0	0	0	0	0	0
Shift >>	0	0	0	0	0	0	0	0
X and Y1	0	1	0	1				
Z + (X and Y1)	0	1	0	1	0	0	0	0
Shift >>	0	0	1	0	1	0	0	0
X and Y2	0	0	0	0				
Z + (X and Y2)	0	0	1	0	1	0	0	0
Shift >>	0	0	0	1	0	1	0	0
X and Y3	0	1	0	1				
Z + (X and Y3)	0	1	1	0	0	1	0	0
Shift >>	0	0	1	1	0	0	1	0

Complete Logic Diagram

4-bit Multiplier

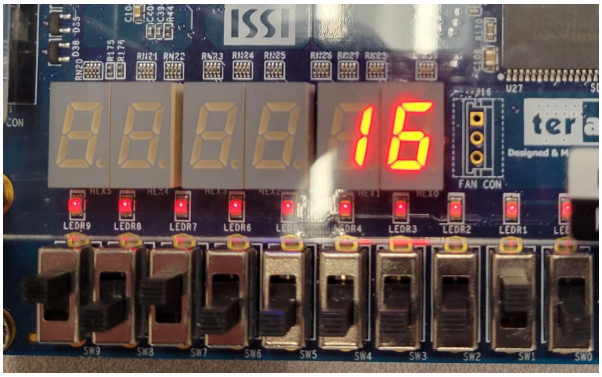


4-bit Multiplier to Seven-Segment Display on DE1-SoC

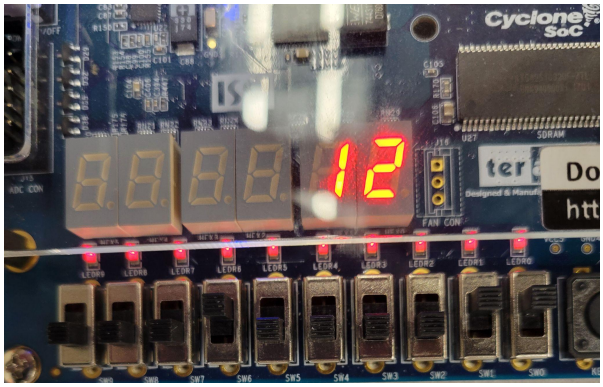


Results and Simulations:

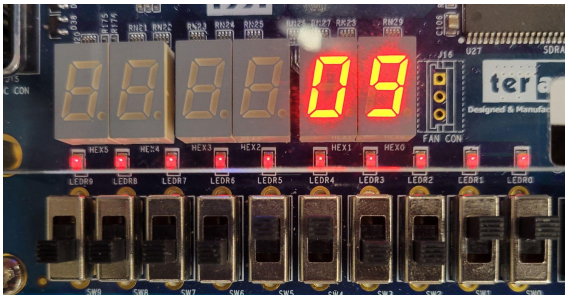
4-bit Multiplier (DE1-SoC Board)



4x4 multiplication using switches, multiplicand is the right 4 and the multiplier is the following 4



3x4 multiplication



3x3 multiplication

Conclusion

In this lab, using the circuits built in the previous lab, we were able to build a 4-bit multiplier. The design went rathner smoothly but we had difficulties with the implementation. We were very certain that the design was correct but struggled to get the correct outputs. After debugging we were able to solve the issue finding a bug while trying to upload to the DE1-Soc Board. Once this was solved we were able to complete the project successfully being able to multiply two 4-bit numbers using the switches and display the result

LAB 5B: A 4 Bit Multiplier

Student Group Number: 6

Student Name	Student C #	Contribution	Signature
Richard Chin	23709160		Richard
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To Be Submitted:

☐ Fully functional 4 bit multiplier on DE1 Board

Comments:

works, no negatives

Sign Off Date	Sign Off Time	TA Signature
3-31-22	1:25 pm	Isaac