ECE 414 Computer Organization and Design

EXPERIMENT 4. STOPWATCH

Steps	Grade
1	/5.0
2	/2.0
3	/2.0
4	/1.0

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on:
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Objective

In this experiment, you are required to design and verify the correct operation of a digital stopwatch using mixed modeling techniques in Verilog. Coding, verification, simulation, synthesis and timing analysis will be carried out using Xilinx ISE tools. Verified designs will be implemented on Digilent's NEXSYS-4 FPGA boards for demonstration of correct operation.

Procedure

- A stopwatch is a device that is designed to measure the amount of time elapsed from a particular time when activated to when it is deactivated. In its simplest form, a stopwatch contains digits of numbers counting up in a predetermined format and it employs a switch/button to start or pause the counting operation. You are required to design an accurate 10 minute-stopwatch with the digits shown in Figure 1. The design should have an asynchronous clear and a pause/start count button/switch to control the device. Since four of the 7-segment displays on the boards will be used simultaneously, you are required to multiplex the inputs to each display, similar to what we did in Lab 2. Set the refresh rate of each display to about 50 times per second. This means that you need to shift the enabled 7-segment display every 5 ms. In addition to these stopwatch functions, your design should also have a blinking mode that is controlled by a switch. When this mode is on, the displays should blink at a rate of 1 Hz when the stopwatch is paused.

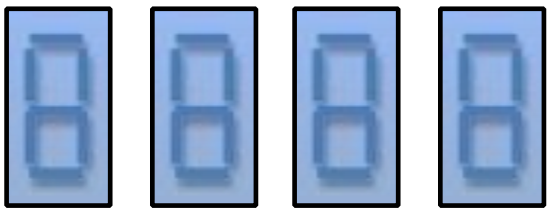

Figure 1. Stopwatch 4-digit display. Minutes can go up to 9 and rolls over to 0 after that.

1.

- **a.** Develop a testbench for the design that creates stimuli for all possible input combinations. That is, show clearly that you can control the device properly with the inputs (start/stop, reset, and blinking mode).
- **b.** Using the testbench you developed, run a functional verification using ISim. Verify the correct functional operation by presenting snapshots of sample waveforms.

2.

- **a.** Identify pad-to-pad timing constraints and define a time budget for your design.
- **b.** Using the Xilinx ISE Synthesis tool, synthesize the design and obtain device utilization summary.
- **c.** Obtain the RTL and technology schematics showing the block level and register level implementation of your design.

3.

- **a.** Using the PlanAhead tools of Xilinx ISE, run the post-place and route static timing analysis and obtain the report. Verify that all the constraints are met and list down the best and worst delay paths.
- **b.** Run the post-place and route simulation and obtain the waveforms in ISim. Compare and contrast the results of this simulation with the simulation results of functional verification step.
- **c.** Using XPower analyzer obtain the power report for your design.

4. Generate the programming file and download your design to NEXSYS-4 board. Verify the operation of your design by applying input combinations using the switches/push buttons and observing the outputs on the LEDs or 7-segments.