ECE 414 Computer Organization and Design

EXPERIMENT 1. MULTIPLEXER Design

Steps	Grade
1	/1.5
2	/1.0
3	/1.5
4	/1.0
5	/2.0
6	/3.0
Total	/10

Submitted by:
on:
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Objective

In this experiment, you are required to design and verify the correct operation of several multiplexer units using structural and dataflow modeling techniques in Verilog. Coding, verification, simulation, synthesis and timing analysis will be carried out using Xilinx ISE tools. Verified designs will be implemented on Digilent's NEXSYS-4 FPGA boards for demonstration of correct operation.

Procedure

1.
- **a.** Design a 2-to-1 Multiplexer using *structural* (gate level) modeling technique in Verilog HDL.
- **b.** Develop a testbench for the designed multiplexer that creates stimuli for all possible input combinations.
- **c.** Using the testbench you developed, run a functional verification using ISim. Verify the correct functional operation by presenting snapshots of sample waveforms.

2.
- **a.** Identify pad-to-pad timing constraints and define a time budget of 20 ns for your design.
- **b.** Using the Xilinx ISE Synthesis tool, synthesize the design and obtain device utilization summary.
- **c.** Obtain the RTL and technology schematics showing the block level and register level implementation of your design.

3.
- **a.** Using the PlanAhead tools of Xilinx ISE, run the post-place and route static timing analysis and obtain the report. Verify that all the constraints are met and list down the best and worst delay paths.
- **b.** Run the post-place and route simulation and obtain the waveforms for all combinations in ISim. Compare and contrast the results of this simulation with the simulation results of functional verification step.
- **c.** Using XPower analyzer obtain the power report for your design.

4. Generate the programming file and download your design to NEXSYS-4 board. Verify the operation of your design by applying input combinations using the switches/push buttons and observing the outputs on the LEDs or seven segments.

5. Design a 2-to-1 Multiplexer using *dataflow* modeling technique in Verilog HDL. Carry out the steps 1- 4 for this design.

6. Design a 4-to-1 Multiplexer using instances of 2-to-1 Multiplexers you designed. For the first stage selection operation use the *structural* design and for the second stage use the *dataflow* design. Carry out the steps 1-4 for this design.