ECE 414 Computer Organization and Design

EXPERIMENT 2. ADDER/SUBTRACTOR with 7-SEGMENT DISPLAY

Steps	Grade
1	/4.0
2	/2.0
3	/2.0
4	/2.0
Total	/10

Submitted by:

on:

to : Dr. Onur Tigli

Objective

In this experiment, you are required to design and verify the correct operation of an adder/subtractor unit using structural and dataflow modeling techniques in Verilog. Coding, verification, simulation, synthesis and timing analysis will be carried out using Xilinx ISE tools. Verified designs will be implemented on Digilent's NEXSYS-4 FPGA boards for demonstration of correct operation.

Procedure

- Design a half-adder unit using gate primitives in Verilog. Carry out only step 1 for this design.

- Design a full-adder using the instances of the half adder designed in the previous step. The full adder module will have three single bit binary inputs (a_i, b_i, c_i) and two single bit outputs (c_{i+1}, s_i). Carry out only step 1 for this design. Please remember to get RTL and technology schematic snapshot for the full adder.

- Design a 4-bit adder/subtractor unit using the full-adders designed in the previous step plus any other necessary logic gates. This 4-bit adder/subtractor unit will have two 4-bit data inputs (A and B) and a single bit control input (E) that is used to determine the operation of choice (E=0 gives A+B, E=1 gives A-B). The unit will have a 4-bit sum output (S) and a single bit carry output (C_{out}). Carry out step 1 for this design.

- Design a 7-segment display driver that takes three 4-bit numbers and displays them simultaneously on three displays. Note that you need to switch between three displays; so you need a slightly different driver than the one provided with Tutorial 2. Carry out all steps (1-4) for this design.

- Develop the system design that uses the adder/subtractor unit with the 7-segment decoders for A, B and S as depicted in Figure 1. You are expected to show the sign and overflow bits using the decimal points on the 7-segment displays as shown in the figure. Carry out all the steps (1-4) for this design.

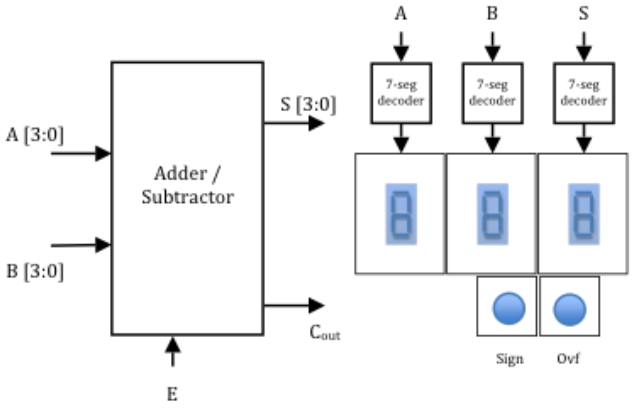

Figure 1. Adder/subtractor system with 7-segment displays.

1.
   a. Develop a testbench for the design that creates stimuli for all possible input combinations. (For the 4-bit adder/subtractor unit, there are too many possible input combinations, use 8 addition and 8 subtraction operations to verify your design)
   b. Using the testbench you developed, run a behavioral simulation using ISim. Verify the correct functional operation by presenting snapshots of sample waveforms. (For the 4bit adder/subtractor unit, it is sufficient to show 8 addition and 8 subtraction operations using different inputs)

2.
   a. Identify pad-to-pad timing constraints and define a time budget of 20 ns for your design.
   b. Using the Xilinx ISE Synthesis tool, synthesize the design and obtain device utilization summary.
   c. Obtain the RTL and technology schematics showing the block level and register level implementation of your design (For half adder and full adder only).

3.
   a. Using the PlanAhead tools of Xilinx ISE, run the post-place and route static timing analysis and obtain the report. Verify that all the constraints are met and list down the best and worst delay paths.
   b. Run the post-place and route simulation and obtain the waveforms for all combinations in ISim. Compare and contrast the results of this simulation with the simulation results of functional verification step.
   c. Using XPower analyzer, obtain the power report for your design.

4. Generate the programming file and download your design to NEXSYS-4 board. Verify the operation of your design by applying input combinations using the switches/push buttons and observing the outputs on the LEDs or seven segments.

Report

- Behavioral simulation results showing proper operation of these individual blocks
  - **i.** Half adder
  - **ii.** Full adder
  - **iii.** 4-bit adder/subtractor unit
  - **iv.** 7-segment display driver

- Device utilization summary of **only** the top module, which includes 4-bit adder subtractor and 7segment display decoder

- RTL and technology schematics of **only** the full adder

- Post place and route static timing report of **only** the top module

- Post place and route simulation results showing the operation of these **individual** blocks
  - **i.** 4-bit adder subtractor unit
  - **ii.** 7-segment display driver

- Power data of **only** the top module