University of Miami

ECE 414 Computer Organization and Design

EXPERIMENT #1 MULTIPLEXER DESIGN

Submitted by: Brandon Rubio, Isabela Bandrich, Rainier Young, Nikeem Dunkelly-Allen
On: 9/16/22
to : Dr. Onur Tigli

Objective

The goal of this lab is to use structural and dataflow design techniques in Verilog to instantiate and test the proper operation of several multiplexer units. The Xilinx ISE tools software will be used for: coding, verification, simulation, synthesis, and timing analysis. For the purpose of demonstrating proper operation, verified designs will be implemented using Digilent's Nexys-4 FPGA boards[1].

Verilog HDL and Testbench Code

Mux 2-to-1:

- **Structural Design Verilog Code:**

```
21  module Mux_2to1(
22      input [1:0] In,
23      input S,
24      output Out
25      );
26      wire a, b, c;
27
28      and(a, In[1], S);
29      not(c, S);
30      and(b, In[0], c);
31      or(Out, a, b);
32
33  endmodule
```

- **Dataflow Design Verilog Code:**

```
21  module DF_Mux_2to1(
22      input [1:0] In,
23      input S,
24      output Out
25      );
26     assign Out = (S)?In[1]:In[0];
27
28  endmodule
```

- **Testbenches (Same (except for module names) for both Structural and Dataflow Design):**

```
module tb_Mux_2to1;

    // Inputs
    reg [1:0] In;
    reg S;

    // Outputs
    wire Out;

    // Instantiate the Unit Under Test (UUT)
    Mux_2to1 uut (
            .In(In),
            .S(S),
            .Out(Out)
    );

    initial begin
            // Initialize Inputs
            In = 0;
            S = 0;

            // Wait 100 ns for global reset to finish
            #100

            In = 0;
            S = 0;
            #100;

            In = 1;
            S = 0;
            #100;

            In = 2;
            S = 0;
            #100;

            In = 3;
```

```
                S = 0;
                #100

                In = 0;
                S = 1;
                #100

                In = 1;
                S = 1;
                #100;

                In = 2;
                S = 1;
                #100;

                In = 3;
                S = 1;
                #100;

            end

        endmodule
```

Mux 4-to-1:

- **Verilog Code:**

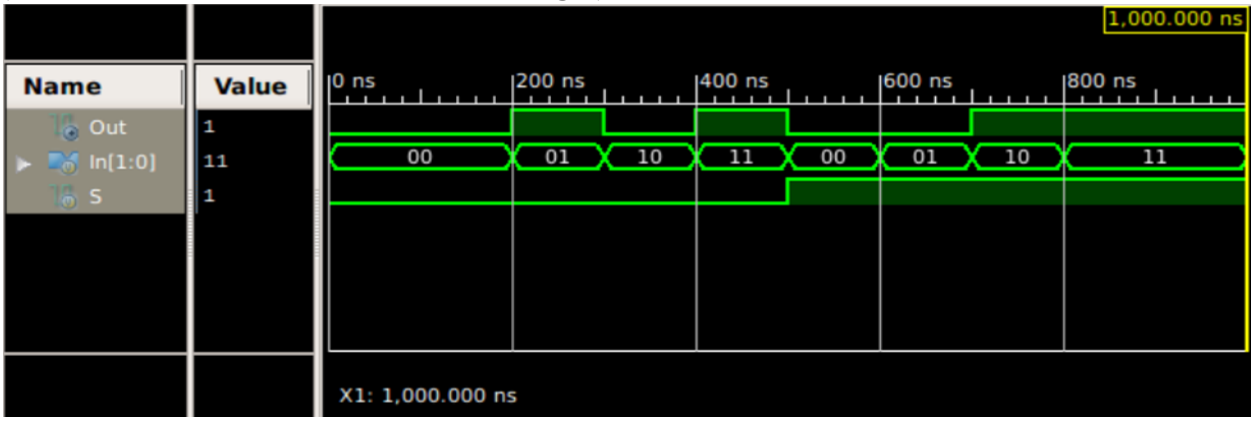
```
21  module Mux_ST_2to1(
22      input [1:0] In,
23      input S,
24      output Out
25      );
26      wire a, b, c;
27      and(a, In[1], S);
28      not(c, S);
29      and(b, In[0], c);
30      or(Out, a, b);
31  endmodule
32
33  module Mux_DF_2to1(
34      input [1:0] In,
35      input S,
36      output Out
37      );
38      assign Out=(S)?In[1]:In[0];
39  endmodule
40
41  module MUX_4to1(
42      input [3:0] In,
43      input [1:0] S,
44      output Out
45      );
46      wire d, e;
47      wire [1:0] f;
48      Mux_DF_2to1 m1(In[3:2],S[0],d);
49      Mux_DF_2to1 m2(In[1:0],S[0],e);
50      assign f = {d,e};
51      Mux_ST_2to1 m3(f,S[1],Out);
52  endmodule
```

- **Testbench:**

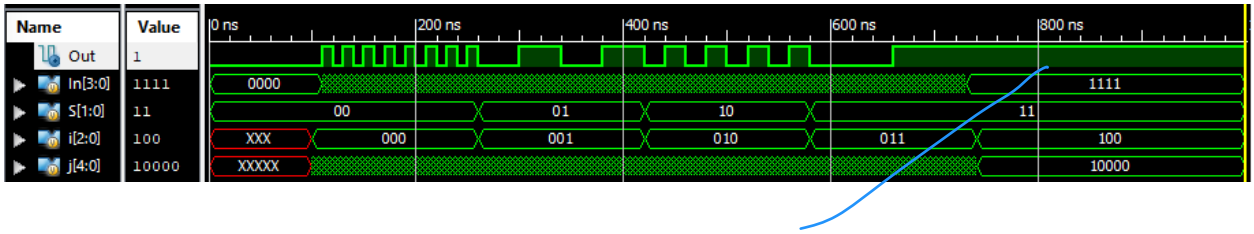
```
25  module tb_MUX_4to1;
26
27      // Inputs
28      reg [3:0] In;
29      reg [1:0] S;
30
31      // Outputs
32      wire Out;
33
34      // Instantiate the Unit Under Test (UUT)
35      MUX_4to1 uut (
36          .In(In),
37          .S(S),
38          .Out(Out)
39      );
40
41      reg [2:0] i; //for S bits
42      reg [4:0] j; //for In bits
43      initial begin
44          // Initialize Inputs
45          In = 0;
46          S = 0;
47
48          // Wait 100 ns for global reset to finish
49          #100;
50
51          // Add stimulus here
52          for (i = 0; i < 4; i = i + 1) begin
53              S = i;
54              for (j = 0; j < 16; j = j + 1) begin
55                  In = j;
56                  #10;
57              end
58          end
59      end
60
61  endmodule
62
```

Simulation Results

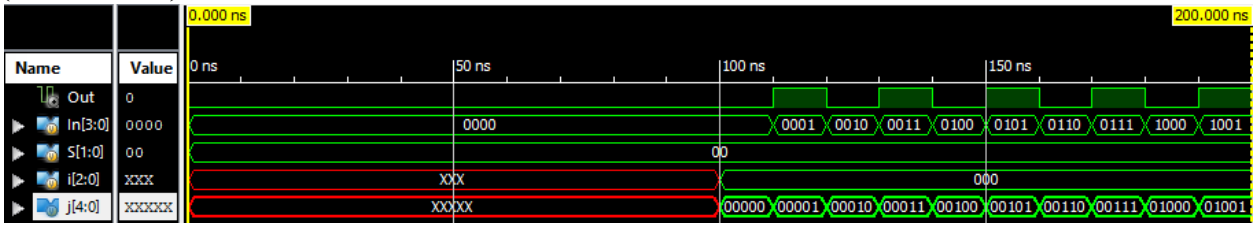
Mux 2-to-1:
(Same for both Structural and Dataflow designs)



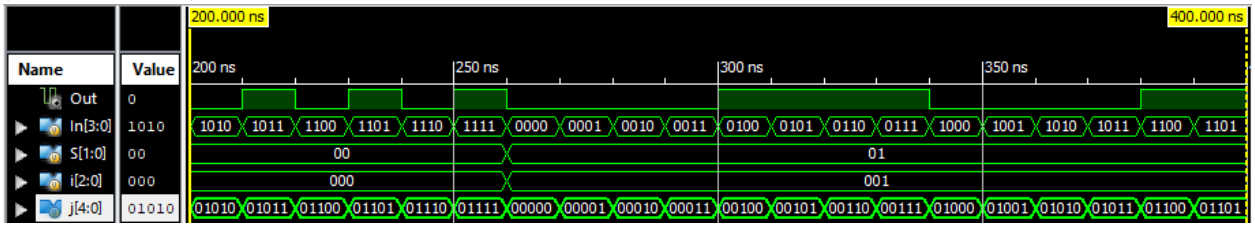
Mux 4-to-1:
(Overview)



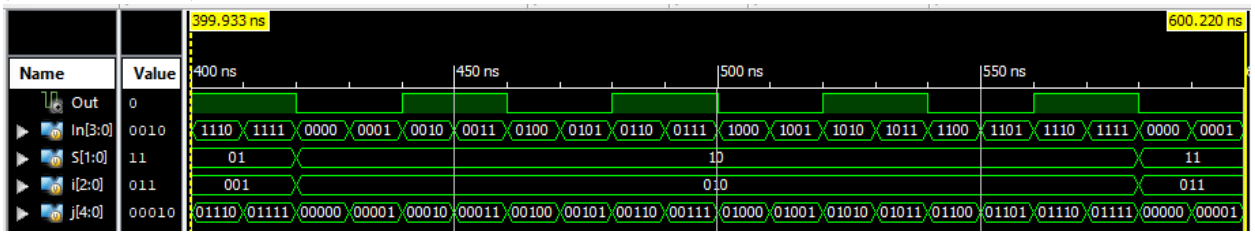
(0ns to 200 ns)



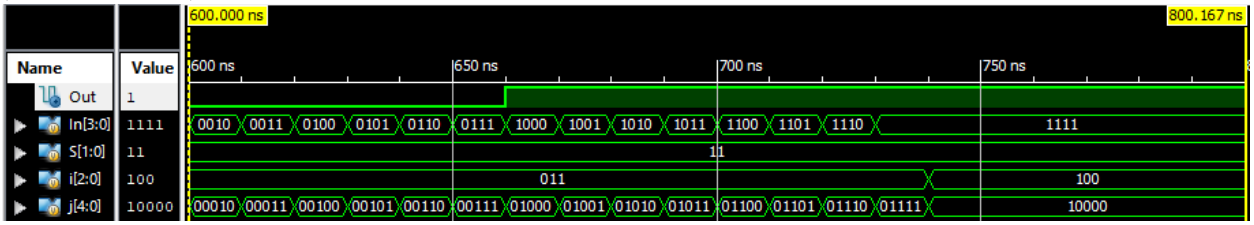
(200ns to 400ns)



(400ns to 600ns)



(600ns to 800ns)



Device Utilization Summary

Mux 2-to-1:
(Same for both Structural and Dataflow designs)

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	1	63400	0%
Number of fully used LUT-FF pairs	0	1	0%
Number of bonded IOBs	4	210	1%

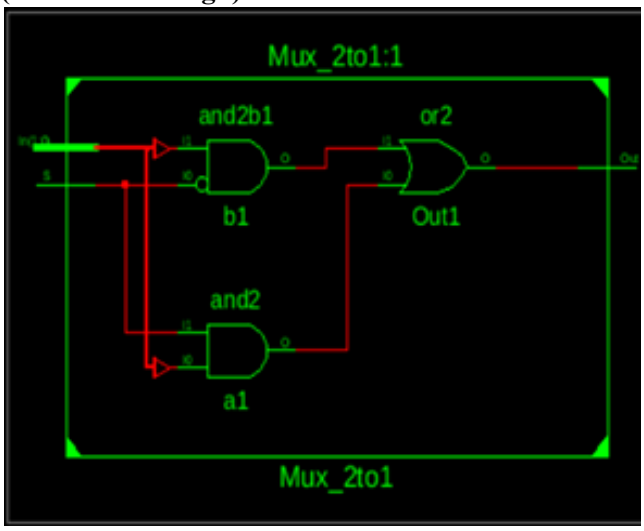
Mux 4-to-1:

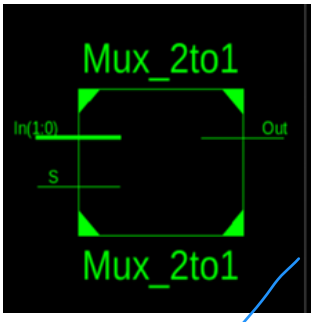
Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	1	63400	0%
Number of fully used LUT-FF pairs	0	1	0%
Number of bonded IOBs	7	170	4%

RTL Schematic and Technology Schematic

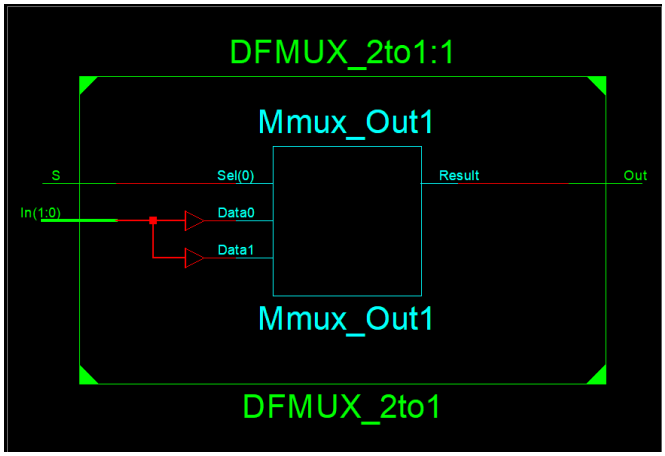
Mux 2-to-1:

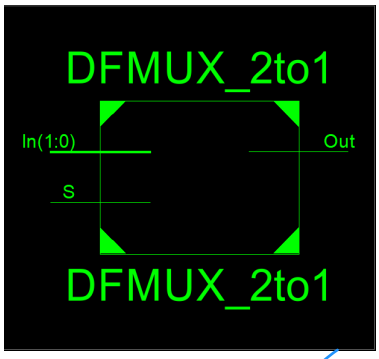
- **RTL Schematic:**
  (Structural Design)



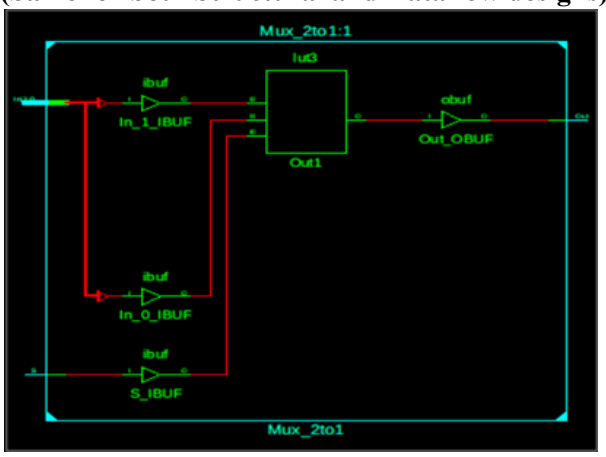


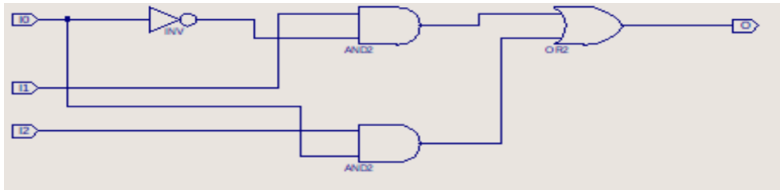
(DataFlow Design)





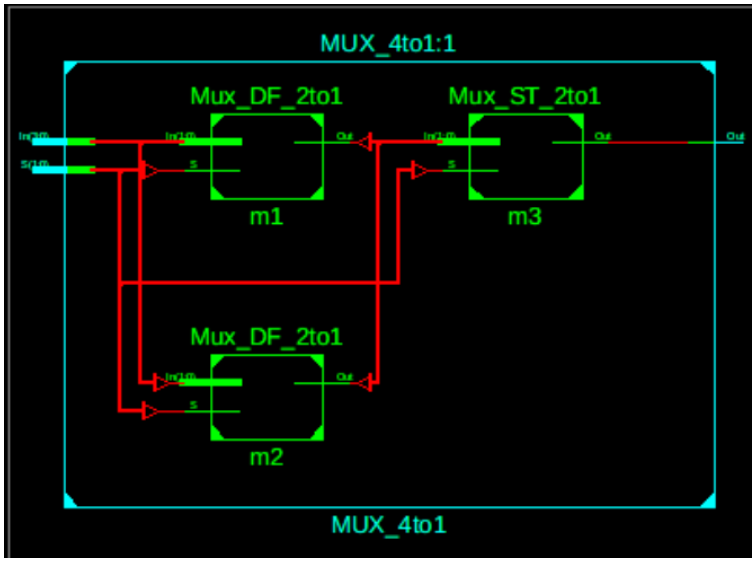
- **Technology Schematic:**
  (Same for both Structural and Dataflow designs)

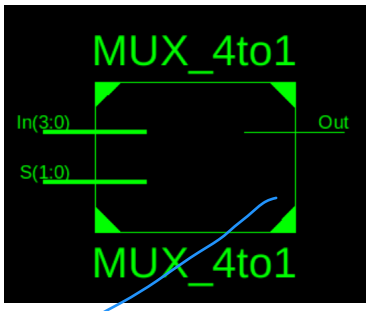




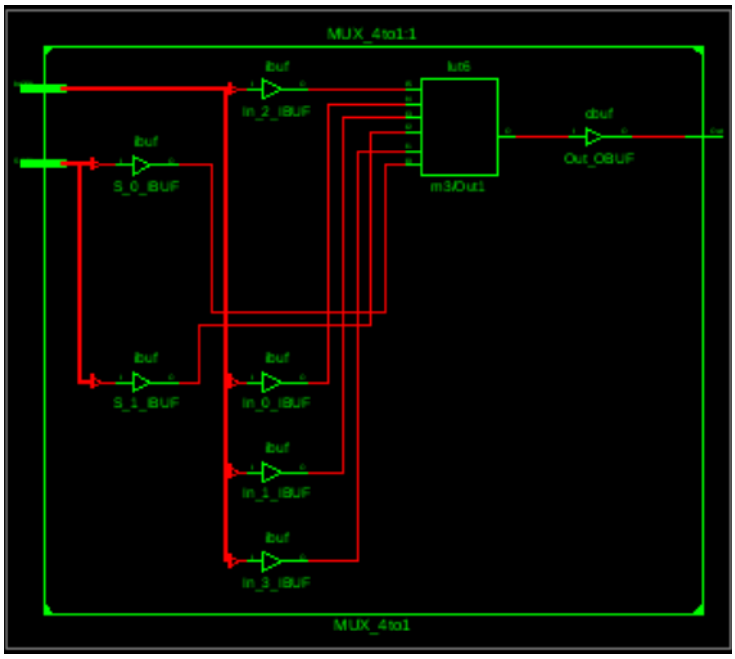
Mux 4-to-1:

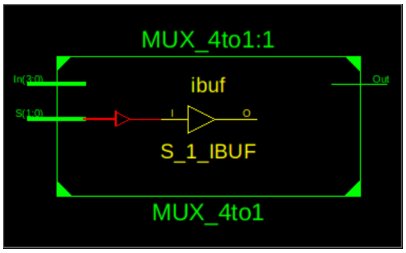
- **RTL Schematic:**

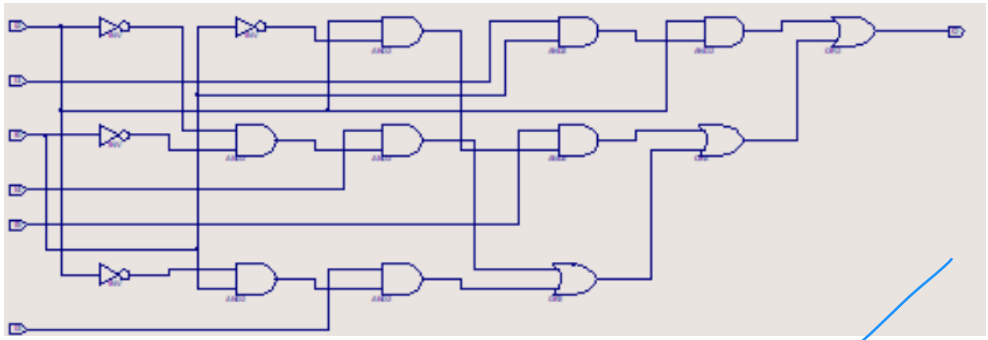




- **Technology Schematic:**







Post Place and Route Static Timing

Mux 2-to-1:
(Structural Design)

```
================================================================================
Timing constraint: TS_pad2pad = MAXDELAY FROM TIMEGRP "inputs" TO TIMEGRP "outputs" 20 ns;
For more information, see From:To (Multicycle) Analysis in the Timing Closure User Guide (UG612).
 3 paths analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Maximum delay is   8.446ns.
--------------------------------------------------------------------------------
```

```
Data Sheet report:
------------------
All values displayed in nanoseconds (ns)

Pad to Pad
---------------+---------------+---------+
Source Pad     |Destination Pad|  Delay  |
---------------+---------------+---------+
In<0>          |Out            |    8.380|
In<1>          |Out            |    8.446|
S              |Out            |    7.979|
---------------+---------------+---------+
```

(Data Flow Design)

```
================================================================================
Timing constraint: TS_pad2padDF = MAXDELAY FROM TIMEGRP "inputsDF" TO TIMEGRP "outputsDF" 20 ns;
For more information, see From:To (Multicycle) Analysis in the Timing Closure User Guide (UG612).
 3 paths analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Maximum delay is   8.204ns.
--------------------------------------------------------------------------------
```

```
Data Sheet report:
------------------
All values displayed in nanoseconds (ns)

Pad to Pad
---------------+---------------+---------+
Source Pad     |Destination Pad|  Delay  |
---------------+---------------+---------+
In<0>          |Out            |    7.899|
In<1>          |Out            |    8.204|
S              |Out            |    7.979|
---------------+---------------+---------+
```

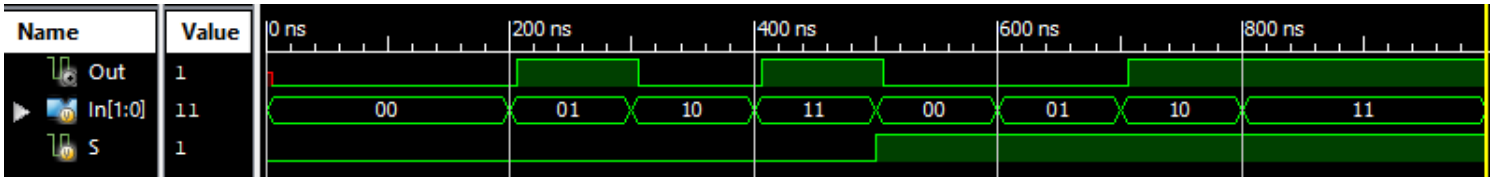
Mux 4-to-1:

```
================================================================================
Timing constraint: TS_MUX_4to1 = MAXDELAY FROM TIMEGRP "inputs" TO TIMEGRP "outputs" 20 ns;
For more information, see From:To (Multicycle) Analysis in the Timing Closure User Guide (UG612).
 6 paths analyzed, 1 endpoint analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Maximum delay is   8.343ns.
--------------------------------------------------------------------------------
```

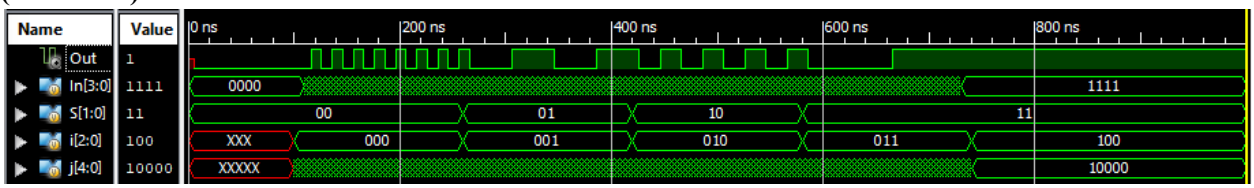
```
Data Sheet report:
------------------
All values displayed in nanoseconds (ns)

Pad to Pad
---------------+---------------+---------+
Source Pad     |Destination Pad|  Delay  |
---------------+---------------+---------+
In<0>          |Out            |    8.124|
In<1>          |Out            |    8.046|
In<2>          |Out            |    8.343|
In<3>          |Out            |    8.309|
S<0>           |Out            |    7.951|
S<1>           |Out            |    8.120|
---------------+---------------+---------+
```

Post Place and Route Simulation Results

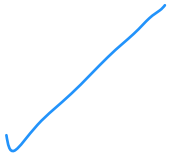
Mux 2-to-1:
(Same for both structural and data flow designs)

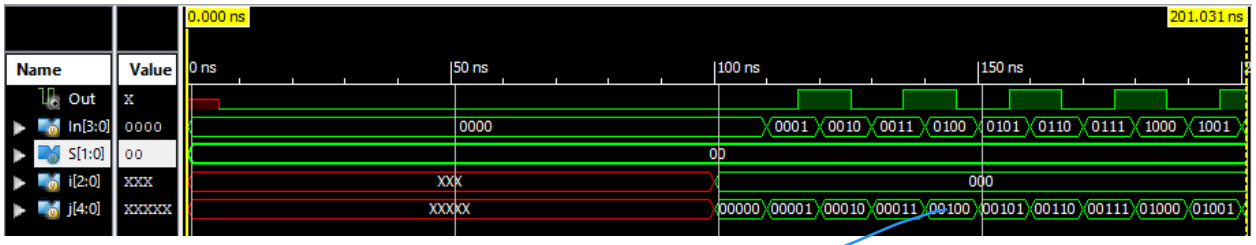


Mux 4-to-1:
(Overview)

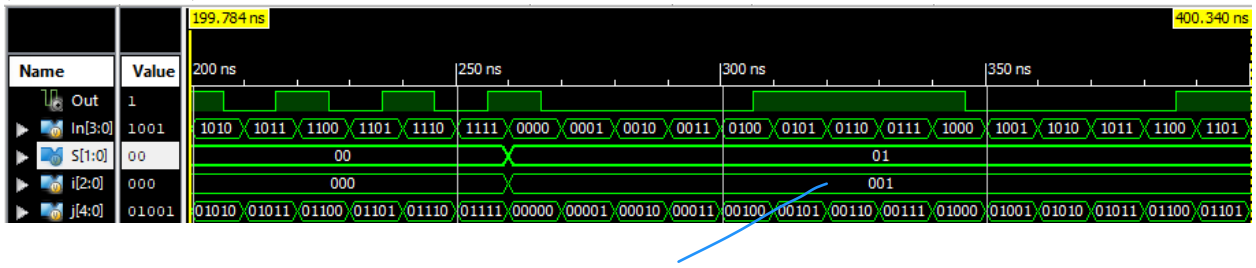


(0ns to 200ns)

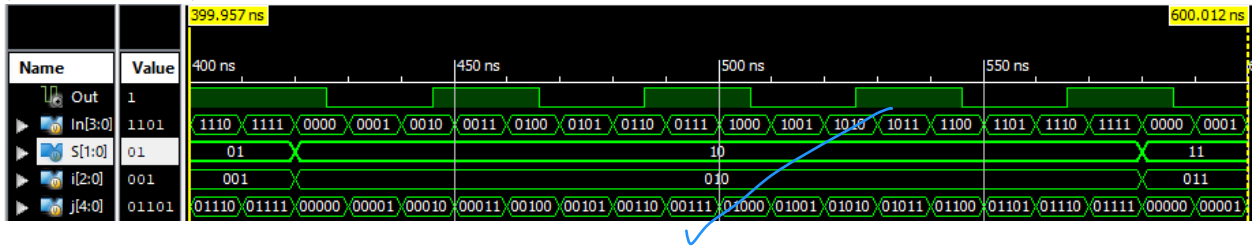




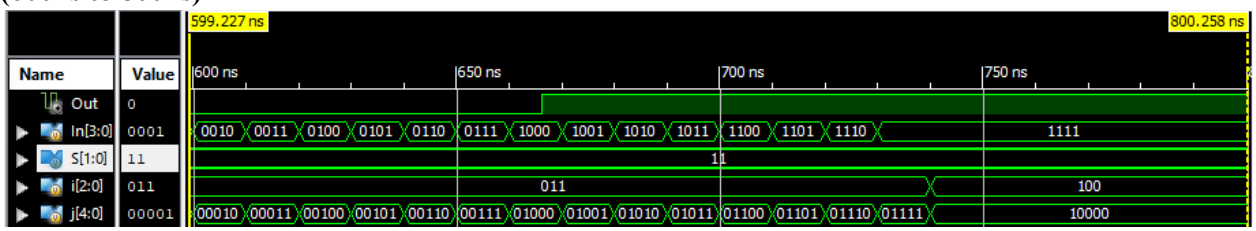
(200ns to 400ns)



(400ns to 600ns)

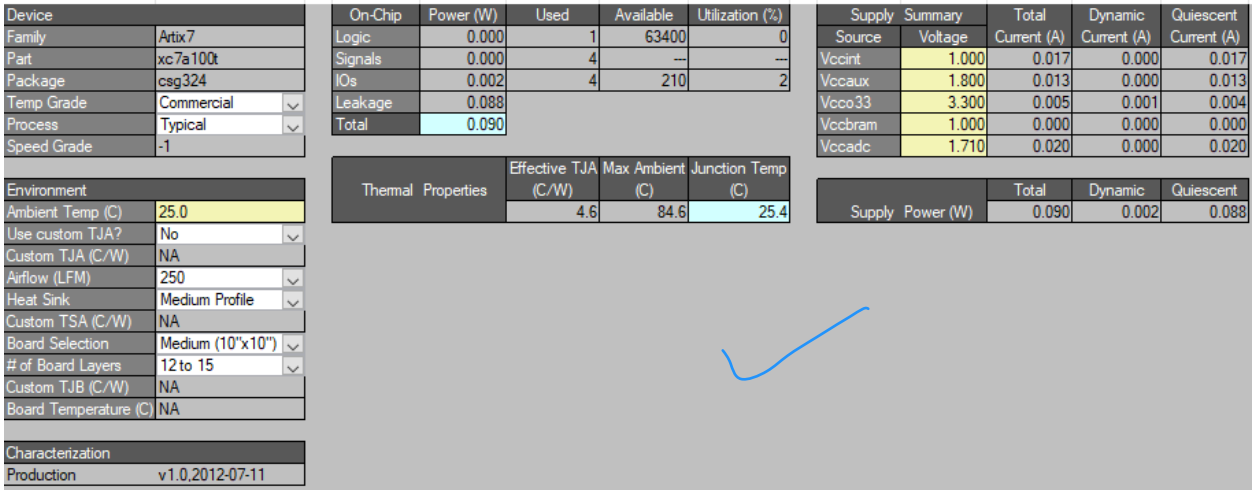


(600ns to 800ns)



Power Data

Mux 2-to-1:
(Same for both structural and data flow designs)



Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-1

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Characterization	
Production	v1.0,2012-07-11

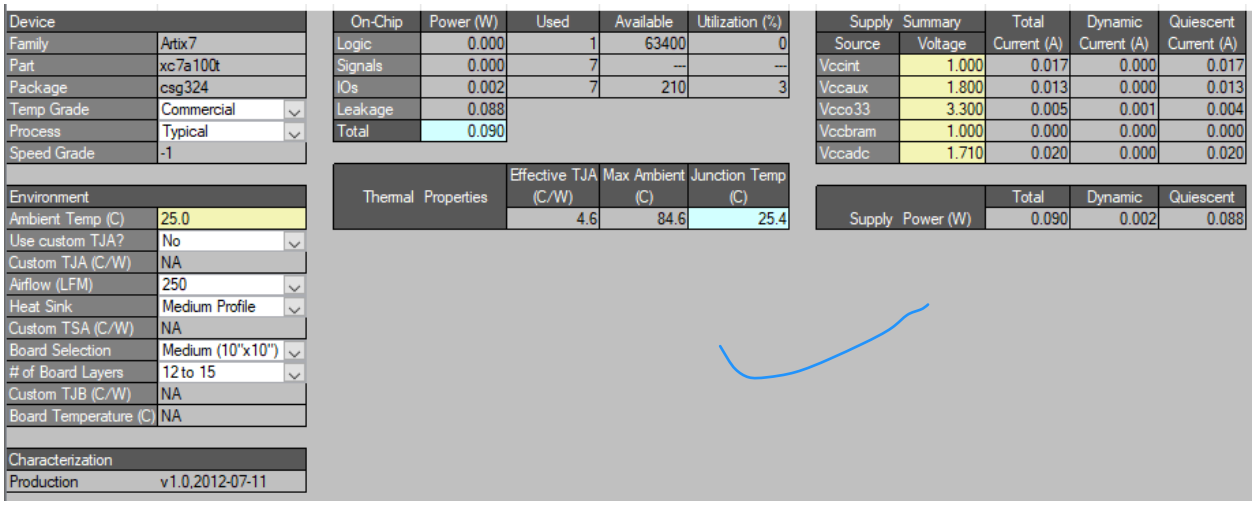
On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	1	63400	0
Signals	0.000	4	---	---
IOs	0.002	4	210	2
Leakage	0.088			
Total	0.090			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco33	3.300	0.005	0.001	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

	Total	Dynamic	Quiescent
Supply Power (W)	0.090	0.002	0.088

Mux 4-to-1:



Device	
Family	Artix7
Part	xc7a100t
Package	csg324
Temp Grade	Commercial
Process	Typical
Speed Grade	-1

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	12 to 15
Custom TJB (C/W)	NA
Board Temperature (C)	NA

Characterization	
Production	v1.0,2012-07-11

On-Chip	Power (W)	Used	Available	Utilization (%)
Logic	0.000	1	63400	0
Signals	0.000	7	---	---
IOs	0.002	7	210	3
Leakage	0.088			
Total	0.090			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	4.6	84.6	25.4

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.017	0.000	0.017
Vccaux	1.800	0.013	0.000	0.013
Vcco33	3.300	0.005	0.001	0.004
Vccbram	1.000	0.000	0.000	0.000
Vccadc	1.710	0.020	0.000	0.020

	Total	Dynamic	Quiescent
Supply Power (W)	0.090	0.002	0.088

Conclusions

After following the procedures given, several multiplexor designs were created and tested to ensure correct operations through–simulations, timing analysis, and then implemented upon the Nexys4FPGA board[1]. As for errors, some difficulties arose when downloading the program to the board, reading the Introduction to FPGA[2] manual gave clarity to our problem and then it was promptly solved.

References

[1]: Nexys4™ FPGA Board Reference Manual, Nexys-4 rev. B; Revised November 19, 2013 by Diligent Beyond Theory

[2]: Introduction to FPGA ECE414 - Fall 2020 pdf by Randil Gajasinghe and Prof. Onur Tigli

ECE414 Computer Organization and Design Lab
Responsibility and Demonstration Sheet

Lab #	1
Lab Description	Multiplexer Design

Lab Responsibility Assignment

Student Name	Responsibility	Signature
Rainier Young	4x1 code and 2x1 dataflow	
Brandon Rubio	4x1 code. 4x1 Simulation/Post-Place and Route Simulation Results	Brandon Rubio
Nikeem Dunkley-Allen	2x1 code Lab report	
Isabela Bendrich	2x1 code Report	Isabela Bendrich

Lab Demonstration

Teaching Assistant Signature	Date
	16-09-22

Comments:

Demonstration shown - (16-09-22)
Fei Batch.