Fall 2022

ECE414 Computer Organization and Design Lab Requirements

Lab schedule: Monday, 2:30 – 4:50 pm & Friday, 5:05 – 6:20pm

Teaching Assistant: Bhuvana Venkatappa **E-mail:** bxv493@miami.edu

Office: TBA **Office Hours:** TBA

Lab Description:

The goal of this lab is to give you some hands-on experience of designing and implementing digital circuits using FPGAs. You will get familiar with a number of tools from Xilinx ISE software throughout this lab.

Lab Requirements:

1. Lab work will be done in groups of 4 students.
    a. It is up to you to coordinate with each other to finish the lab assignments.
    b. If you need to meet with the TA in-person this will be coordinated separately.

2. Hands-on part of the lab work consists of a few stages: (1) Planning/designing the module, (2) Writing the Verilog code, (3) Simulating the Verilog code to verify its proper operation, (4) Assigning I/O pins to physical ports such as switches and LEDs, (5) Creating and downloading the bit file onto the FPGA board, and (6) Testing the design on the FPGA board.

3. Each group will get a Digilent Nexys 4 FPGA board to use throughout the semester. Therefore, you will be able to test the blocks and sub-blocks of your designs at any time. You are expected to demonstrate the operation of your design on the FPGA board during the lab sessions or office hours. Therefore, please read the lab materials and get prepared before the lab in order to finish the lab work successfully. Lab materials will be posted on Blackboard in advance.

4. In addition to demonstrating proper operation of your designs, you are expected to turn in a report for each lab prior to the beginning of the next lab. Some labs will take more than one week, in which case the report will be due the second or third week. A lab report template will be posted on Blackboard. Please submit the electronic version of your lab report along with a zip file containing your entire project folder to blackboard. Name your report and project zip file as follows:
    a. ECE414_GroupNumber_LabNumber_report.pdf
    b. ECE414_GroupNumber_LabNumber_project.zip

5. There will be a final project, which will be done in groups as well. Details will be announced later in the semester.

Grading Policy:

Grades will be given according to class participation, Verilog code, and lab reports (all lab reports are graded out of 10 points).

Late Assignment Submission Policy:

Minus 20% of the total marks for each day late