ECE 414 Computer Organization and Design

EXPERIMENT 6. ALGORITHMIC STATE MACHINE

Steps	Grade
1	/2.5
2	/2.5
3	/2.0
4	/1.0
5	/2.0

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on:
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Objective

In this experiment, you are required to apply algorithmic state machine (ASM) design and optimization techniques in Verilog HDL. The experiment consists of the design and optimization of a simple finite state machine (FSM). Coding, verification, simulation, synthesis and timing analysis will be carried out using Xilinx ISE tools. Verified designs will be implemented on Digilent's NEXYS-4 FPGA boards for demonstration of correct operation.

Procedure

Design an FSM with inputs *data_in*_A, *data_in_B* and an output *count_out.* The function of this state machine is to compare the two input sequences on the two inputs. If *data_in_A = data_in_B* during any four consecutive clock cycles the circuit produces *count_out =1*; otherwise *count_out = 0*.

data_in_A = 0 1 1 0 1 1 1 0 0 0 1 1 0

data_in_B = 1 1 1 0 1 0 1 0 0 0 1 1 1

count_out = 0 0 0 0 1 0 0 0 0 1 1 1 0

Develop a state diagram that indicates clearly all the state transitions, their corresponding conditions and operations to be carried out during each state. Model this state machine in Verilog according to the following:

1. Design, simulate and synthesize the same state machine by first using a single state variable (*state*) approach and then a two state variable (*present_state, next_state*) approach.
2. Design, simulate and synthesize the same state machine by using three state coding styles: s*equential*, *gray*, and *one-hot.*

3. For each approach complete the following table:

Best path delay	Worst path delay	Area	Power

4. For each approach compare the RTL and technology schematics obtained from the synthesis. Note the differences and similarities. Comment on the best and worst approach based on your findings.

5. Implement the "best" design approach. Generate the programming file and download your design to NEXYS-4 board. Verify the operation of your design by applying input combinations using the switches/push buttons and observing the outputs on the LEDs or seven segments.

References

[1]: Brown, S., Vranesic, Z., "Fundamentals of Digital Logic with VHDL Design," McGraw Hill, 2000.