# CS2100 Computer Organisation Lab #10: Using Logisim II

Remember to bring this along to your lab!

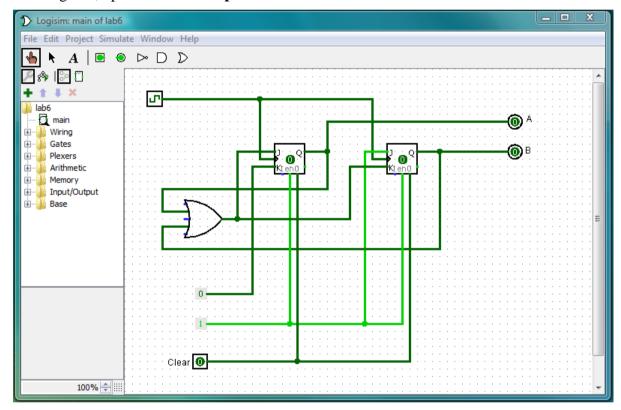
(Week 13: 12 – 16 April 2021)

[ This document is available on LumiNUS and module website <a href="http://www.comp.nus.edu.sg/~cs2100">http://www.comp.nus.edu.sg/~cs2100</a> ]

No.:
sequential circuits.

#### Part I

1. Run Logisim, open the file **lab10part1.circ**. The circuit is shown below.



- 2. The circuit consists of two JK flip-flop and an OR gate. Note the following:
  - The outputs of the two JK flip-flops are labelled A and B, which form the state of the circuit.
  - The Clock is connected to the clock inputs of the flip-flops.
  - The logic constant 1 is connected to the Enable inputs of the flip-flops.
  - The Clear switch is connected to the clear inputs of the flip-flops. Hence when Clear = 1, it clears the contents of both flip-flips to 0, bringing the circuit to the initial state of AB=00.
  - The flip-flop inputs are as follows:

For flip-flop A: JA = A + B; KA = 0

For flip-flop B: JB = 1; KB = A + B

## 3. Complete the following table:

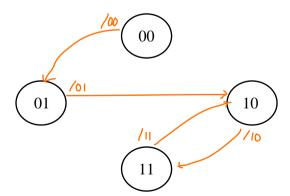
[6 marks]

Present state		Flip-flop inputs				Next state	
A	В	JA	KA	JB	KB	$A^+$	$B^{\scriptscriptstyle +}$
0	0	0	Ō	1	0	0	1
0	1		0		- 1	1	0
1	0		0	i		J	1
1	1		O	1	1	I	σ

- 4. Verify the correctness of your table above by testing the circuit in Logisim.
  - a) Click on "Clear" input to get 1. This clears both flip-flops to 0, bringing the circuit to the initial state of AB=00.
  - b) Click on "Clear" input to get 0 before you proceed. This puts the flip-flops in their normal operation mode.
  - c) Clicking the "Clock" input toggles its value. When the "Clock" value changes from 0 to 1 (i.e. a rising edge), the flip-flops react according to the commands at their J and K inputs.
  - d) Click the "Clock" input several times to simulate the square wave, and watch the outputs of the flip-flops change their values. Do the values follow your table above?
  - e) If at any point of time you want to reset the flip-flops to the initial state of 00, go to step (a) above.

### 5. Complete the state diagram below.

[4 marks]



## Part II

6. You will design a sequential circuit using JK flip-flops. The flip-flop inputs are given below:

For flip-flop 
$$A$$
:  $JA = 1$ ;

$$KA = A \cdot B$$

$$JB = 0$$
;

$$KB = (A \cdot B)'$$

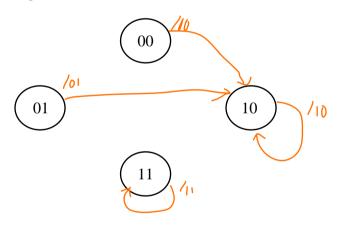
7. Complete the following table:

[6 marks]

Present state		Flip-flop inputs				Next state	
A	В	JA	KA	JB	KB	$A^+$	$B^{\scriptscriptstyle +}$
0	0		D	0		1	0
0	1	- 1	O	0		1	0
1	0		0	۵		1	O
1	1	L	(	0	0	0	

8. Complete the state diagram below.

[4 marks]



- 9. Implement the circuit on Logisim and show it to your lab TA. In your circuit, you should also include a "Preset" input so that you can set both flip-flops to 1. [5 marks]
- 10. As this is your final lab, your lab report will not be returned to you.

Total: 25 marks