

Synthesis Tutorial for windows

In this tutorial, we are going to synthesis a full adder and please make sure you have run.tcl and fa.v files and connection to Internet.

1 Putty

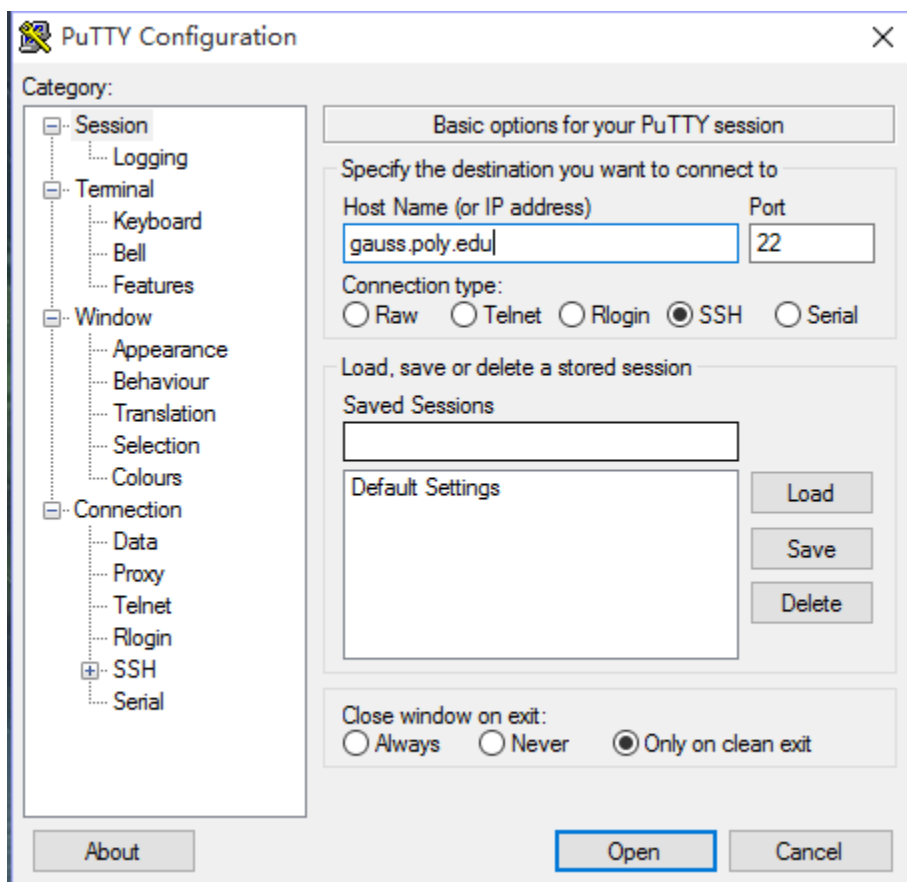
Download Putty from the following link:

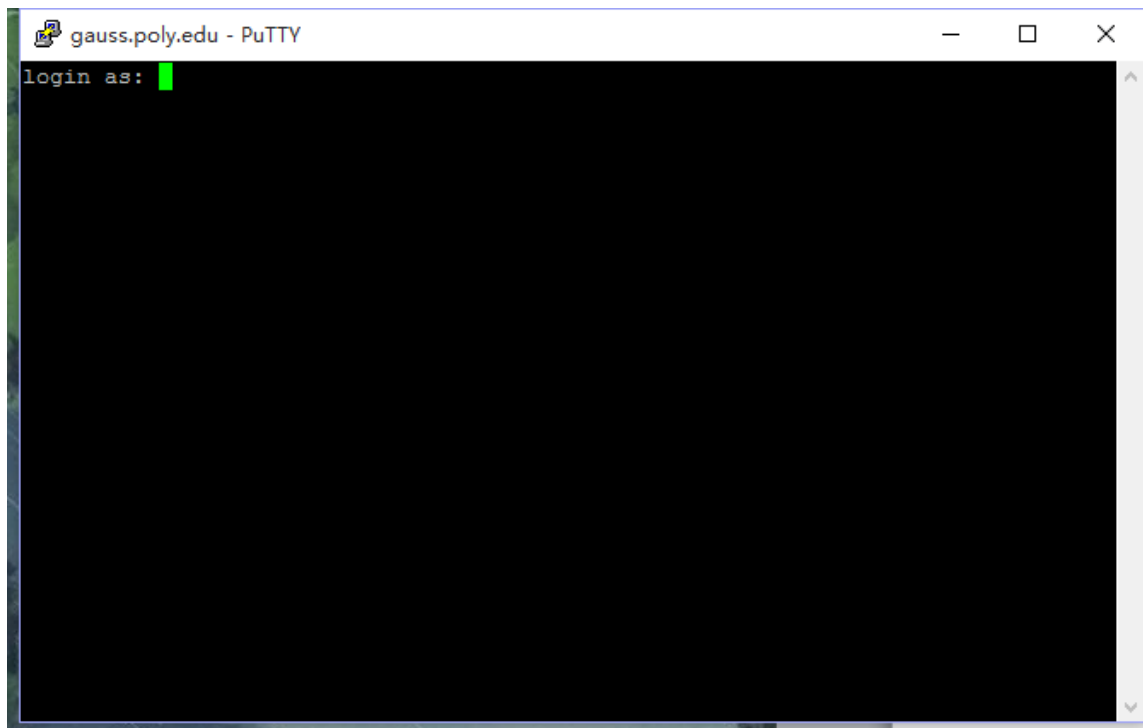
<http://www.chiark.greenend.org.uk/~sgtatham/putty/download.html>

Install PuTTY by double clicking the downloaded file.

Double click and open it.

Enter the Host Name as: gauss.poly.edu and click Open

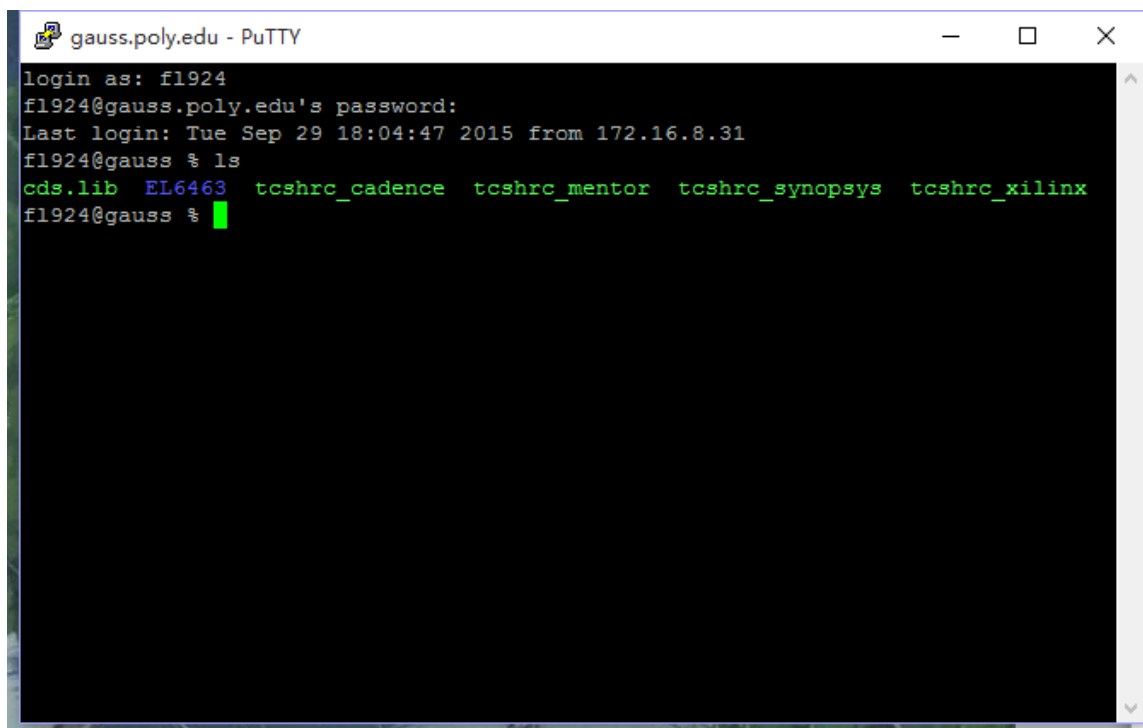




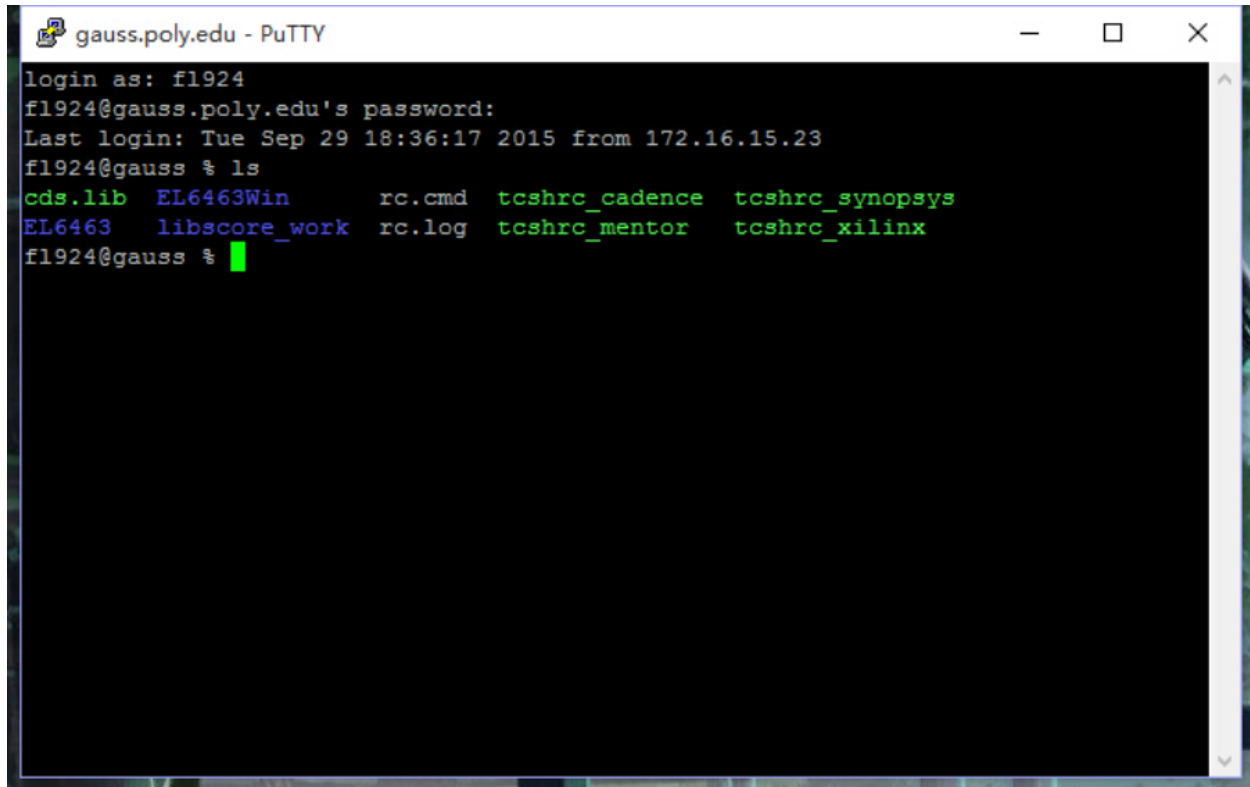
This window should open if you have done everything correct.

Login using your NetID and Password (N number, example: N12345678).

You can use command: **ls** , to check what is in your root folder



create a project for your project using command: **mkdir EL6463Win** (You can name the folder what ever you want).



```
gauss.poly.edu - PuTTY
login as: f1924
f1924@gauss.poly.edu's password:
Last login: Tue Sep 29 18:36:17 2015 from 172.16.15.23
f1924@gauss % ls
cds.lib  EL6463Win      rc.cmd  tcshrc_cadence  tcshrc_synopsys
EL6463  libscore_work    rc.log  tcshrc_mentor   tcshrc_xilinx
f1924@gauss %
```

2. Copy project files (run.tcl and fa.v)to Guass

Download FileZilla to transfer local files to Gauss.

<https://filezilla-project.org/download.php?type=client>

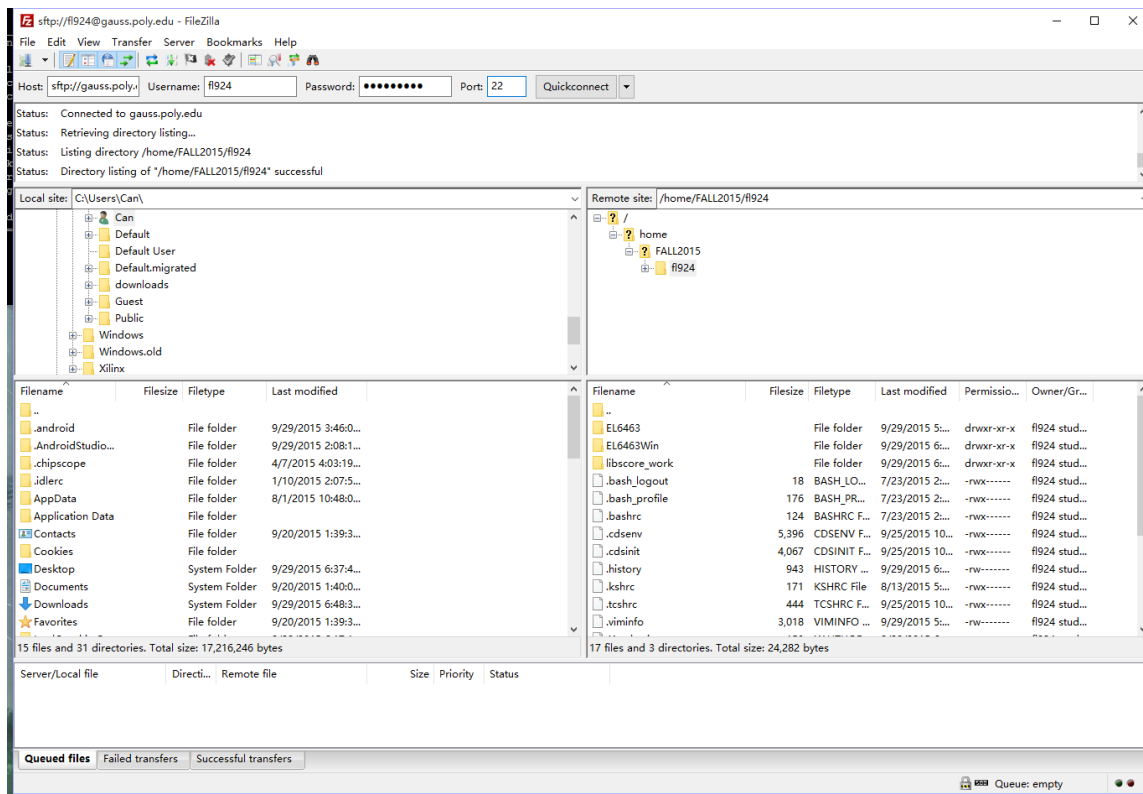
After you install it, start FileZilla and Quickconnect to Gauss.

Connection Info:

Host: gauss.poly.edu

Username: NetID

Password: N number (example: N12894649)

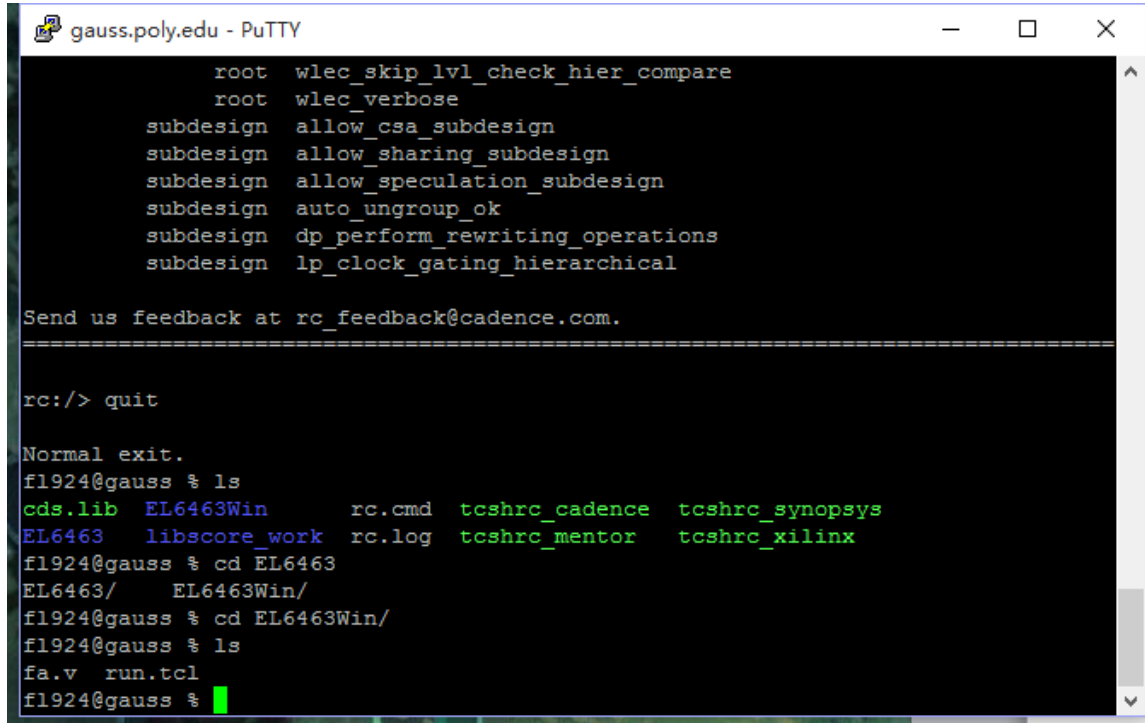


Drag run.tcl and fa.v to our project folder: EL6463Win

3 Synthesis on Putty

login to Gauss and go to project folder

cd EL6463Win



```
root wlec_skip_lvl_check_hier_compare
root wlec_verbose
subdesign allow_csa_subdesign
subdesign allow_sharing_subdesign
subdesign allow_speculation_subdesign
subdesign auto_ungroup_ok
subdesign dp_perform_rewriting_operations
subdesign lp_clock_gating_hierarchical

Send us feedback at rc_feedback@cadence.com.
=====

rc:/> quit

Normal exit.
fl924@gauss % ls
cds.lib  EL6463Win  rc.cmd  tcshrc_cadence  tcshrc_synopsys
EL6463  libscore_work  rc.log  tcshrc_mentor  tcshrc_xilinx
fl924@gauss % cd EL6463
EL6463/  EL6463Win/
fl924@gauss % cd EL6463Win/
fl924@gauss % ls
fa.v  run.tcl
fl924@gauss %
```

run synthesis using command:

rc -f run.tcl

After finished, you should see the following window

```
gauss.poly.edu - PuTTY

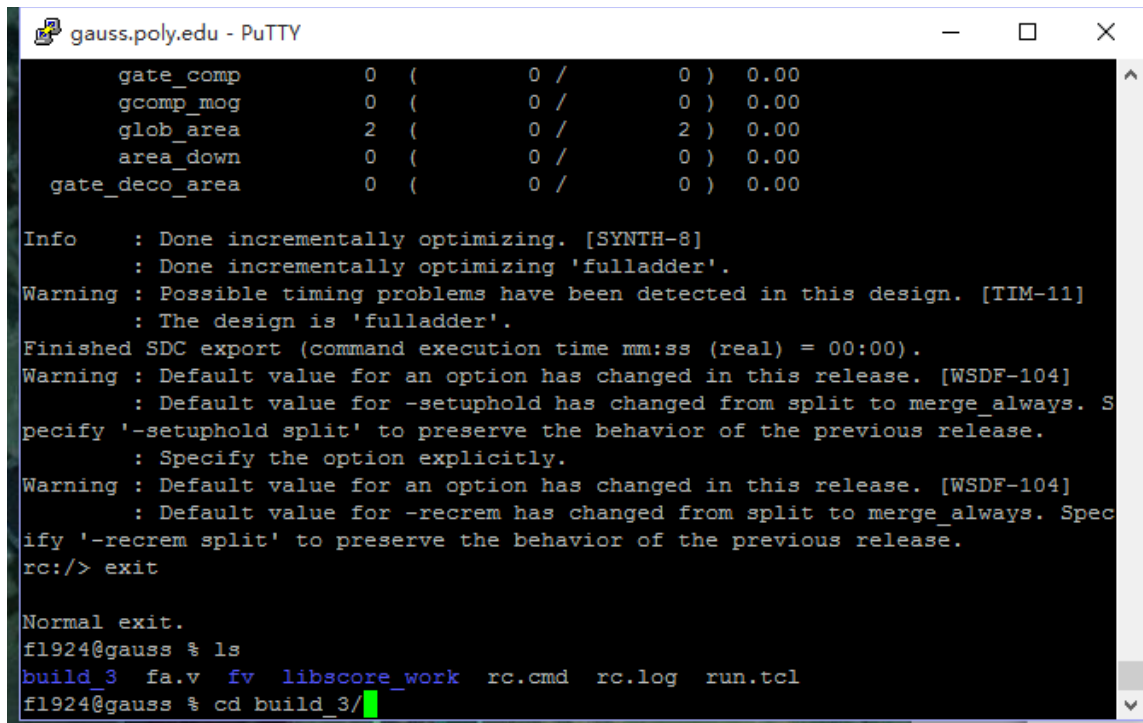
    rem_buf      0 (      0 /      0 ) 0.00
    rem_inv      0 (      0 /      0 ) 0.00
    merge_bi     0 (      0 /      0 ) 0.00
    rem_inv_qb   0 (      0 /      0 ) 0.00
    io_phase     0 (      0 /      0 ) 0.00
    gate_comp    0 (      0 /      0 ) 0.00
    gcomp_mog    0 (      0 /      0 ) 0.00
    glob_area    2 (      0 /      2 ) 0.00
    area_down    0 (      0 /      0 ) 0.00
    gate_deco_area 0 (      0 /      0 ) 0.00

Info      : Done incrementally optimizing. [SYNTH-8]
          : Done incrementally optimizing 'fulladder'.
Warning   : Possible timing problems have been detected in this design. [TIM-11]
          : The design is 'fulladder'.
Finished SDC export (command execution time mm:ss (real) = 00:00).
Warning   : Default value for an option has changed in this release. [WSDF-104]
          : Default value for -setuphold has changed from split to merge_always. Specify '-setuphold split' to preserve the behavior of the previous release.
          : Specify the option explicitly.
Warning   : Default value for an option has changed in this release. [WSDF-104]
          : Default value for -recrem has changed from split to merge_always. Specify '-recrem split' to preserve the behavior of the previous release.
rc:/>
```

Quit rc mode using command: **exit**

4. Check synthesis result.

Go to folder build_3 using command: **cd build_3**



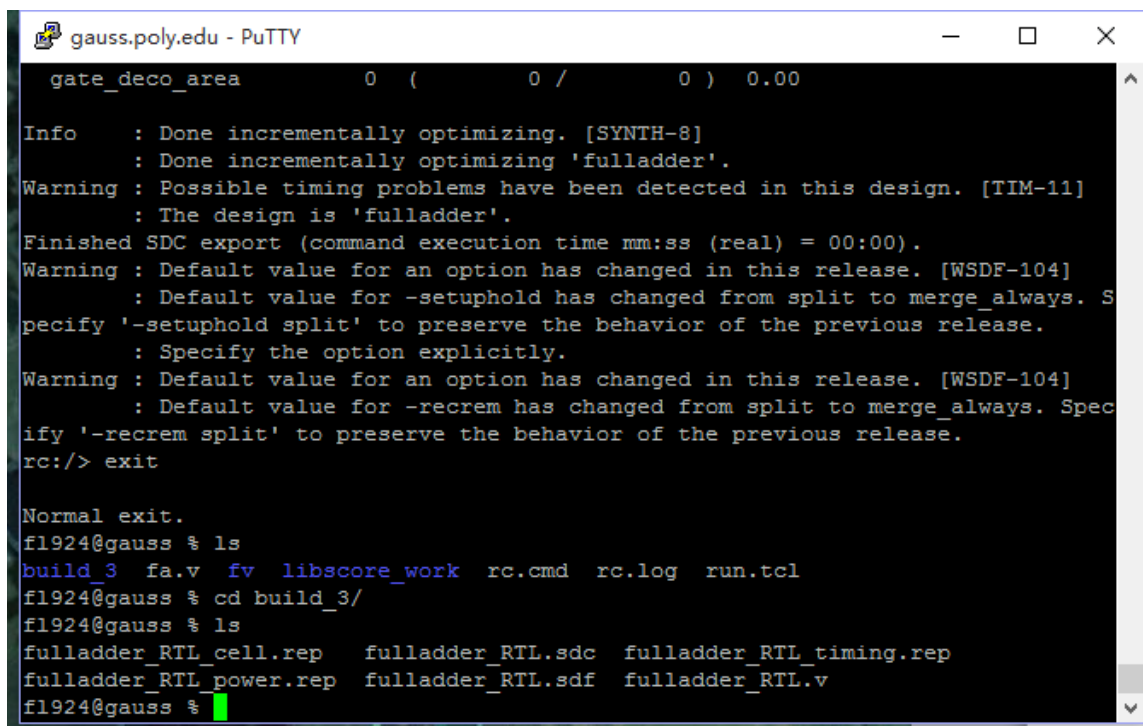
```
gauss.poly.edu - PuTTY

gate_comp      0 (      0 /      0 ) 0.00
gcomp_mog      0 (      0 /      0 ) 0.00
glob_area      2 (      0 /      2 ) 0.00
area_down      0 (      0 /      0 ) 0.00
gate_deco_area  0 (      0 /      0 ) 0.00

Info      : Done incrementally optimizing. [SYNTH-8]
           : Done incrementally optimizing 'fulladder'.
Warning   : Possible timing problems have been detected in this design. [TIM-11]
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Warning   : Default value for an option has changed in this release. [WSDF-104]
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           : Specify the option explicitly.
Warning   : Default value for an option has changed in this release. [WSDF-104]
           : Default value for -recrem has changed from split to merge_always. Spec
ify '-recrem split' to preserve the behavior of the previous release.
rc://> exit

Normal exit.
fl924@gauss % ls
build_3  fa.v  fv  libscore_work  rc.cmd  rc.log  run.tcl
fl924@gauss % cd build_3/
```

There are several files in build_3 and open fulladder_RTL.v using **vim fulladder_RTL.v**

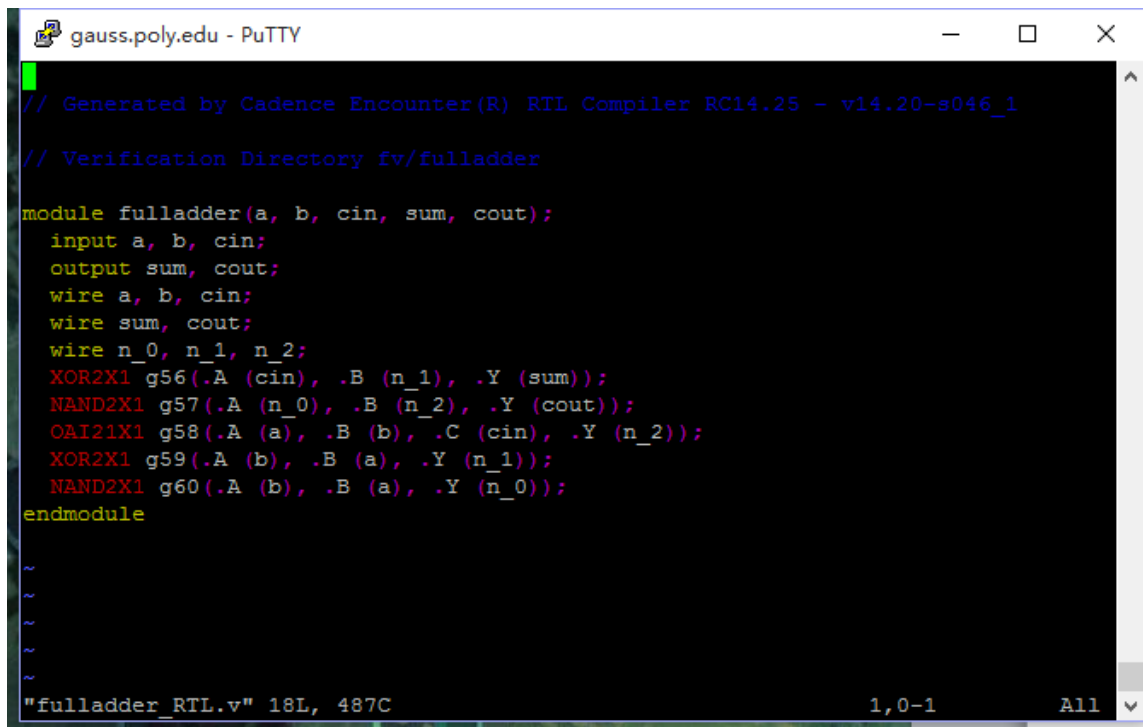


```
gauss.poly.edu - PuTTY

gate_deco_area  0 (      0 /      0 ) 0.00

Info      : Done incrementally optimizing. [SYNTH-8]
           : Done incrementally optimizing 'fulladder'.
Warning   : Possible timing problems have been detected in this design. [TIM-11]
           : The design is 'fulladder'.
Finished SDC export (command execution time mm:ss (real) = 00:00).
Warning   : Default value for an option has changed in this release. [WSDF-104]
           : Default value for -setuphold has changed from split to merge_always. S
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           : Specify the option explicitly.
Warning   : Default value for an option has changed in this release. [WSDF-104]
           : Default value for -recrem has changed from split to merge_always. Spec
ify '-recrem split' to preserve the behavior of the previous release.
rc://> exit

Normal exit.
fl924@gauss % ls
build_3  fa.v  fv  libscore_work  rc.cmd  rc.log  run.tcl
fl924@gauss % cd build_3/
fl924@gauss % ls
fulladder_RTL_cell.rep  fulladder_RTL.sdc  fulladder_RTL_timing.rep
fulladder_RTL_power.rep  fulladder_RTL.sdf  fulladder_RTL.v
fl924@gauss %
```



```
gauss.poly.edu - PuTTY
// Generated by Cadence Encounter(R) RTL Compiler RC14.25 - v14.20-s046_1
// Verification Directory fv/fulladder

module fulladder(a, b, cin, sum, cout);
  input a, b, cin;
  output sum, cout;
  wire a, b, cin;
  wire sum, cout;
  wire n_0, n_1, n_2;
  XOR2X1 g56(.A (cin), .B (n_1), .Y (sum));
  NAND2X1 g57(.A (n_0), .B (n_2), .Y (cout));
  OAI21X1 g58(.A (a), .B (b), .C (cin), .Y (n_2));
  XOR2X1 g59(.A (b), .B (a), .Y (n_1));
  NAND2X1 g60(.A (b), .B (a), .Y (n_0));
endmodule

~
~
~
~
~
"fulladder_RTL.v" 18L, 487C 1,0-1 All
```

This is the RTL result after synthesis.