New York University Polytechnic School of Engineering

Electrical and Computer Engineering
Course Outline EL GY 6463 Advanced Hardware
Fall 2015
Professor Siddharth Garg
Mondays 12:30PM-3:00PM; Rogers Hall 215 (RGSH 215)

To contact professor: Email: sg175@nyu.edu
Office: 2 Metrotech, 10.076
Office hours: Mondays 3PM-5PM or by appointment
(Skype: siddharth.j.garg)

Teaching Staff

Zahra Ghodsi (Office Hours Tue 6:00PM-8:30PM) ghodsi@nyu.edu
Neha Rohilla (Office Hours Thu 2:30PM – 5:00PM) neha.rohilla@nyu.edu
Fuyang Liu (Office Hours Fri 2:30PM – 5:00PM) fl924@nyu.edu
Venkata Haareeth Parimi (Office Hours Wed 2:30PM-5:00PM) haareeth.p@nyu.edu

(Location of office hours to be determined soon and will be announced online.)

Course Pre-requisites: The course has no formal pre-requisites, but students are expected to be familiar with Boolean logic, digital logic gates, finite-state machines and be comfortable with at least one software programming language (example, C, C++, etc.)

Course Description

This course shows how a hardware-description language (for example, Verilog) can be used for computer hardware modeling, logic synthesis, register-level synthesis and simulation. A design project is required and students make a written and oral presentation.

Course Objectives
By the end of this course, students will be able to:

1) Describe and synthesize complex hardware modules using hardware description languages like Verilog and SystemVerilog, and using high level synthesis tools.
2) Understand critical hardware building blocks (arithmetic units, decoders, memories and communication fabric) and important hardware concepts including pipelining and parallelism
3) Verify the correctness of the designs using testbenches, assertions and formal techniques.
4) Appreciate and design for multiple metrics of hardware quality metrics including power, energy and reliability

Readings
The required text for the course is:

The Verilog® Hardware Description Language 5th Edition by Thomas and Moorby. Springer US. (http://www.springer.com/us/book/9780387849300)

In addition, instructors lecture slides and handouts/tutorials will be posted online.

Course Structure

The course has three primary pedagogical components: (1) weekly lectures; (2) biweekly programming assignments; (3) half semester long project.

Assessment is based on three components: (1) 5 assignments, on a biweekly basis; (2) a midterm and a final exam; and (3) a semester long project. Although the relevant theory will be discussed and taught in class, all assessments, including the midterm and final examinations are based on hands-on problems to emphasize the practical nature of this course.

The structure of the course below is tentative and subject to change depending on the pace of progress through the

09/14 Introduction and Basics

- Introduction, historical perspective, Moore's law
- Basic combinational logic and finite state-machines in Verilog
- Assignment 1 released.

09/21 Verilog (continued), Synthesis and Discrete Event Simulations

- Combinational logic and FSMs in Verilog (continued)
- Basic synthesis and writing synthesizable Verilog
- Introduction to discrete event simulation

09/28 Advanced Verilog

- Behavioral modeling: control flow, tasks and functions
- Concurrent processes
- Hardware module: RAMs and FIFOs
- Assignment 1 due. Assignment 2 released.

10/05 (Away) TA class

- Examples illustrating concepts so far
- Pre-recorded lecture: writing testbenches

10/13 (Note: Tuesday class) Advanced Verilog

- Module hierarchy, parameters and generate blocks
- On-chip communication: buses
- Assignment 2 due. Assignment 3 released

10/19 On-chip communication: Networks-on-chip

- Why networks-on-chip?
- Router design, network topology, industry example

10/26 Midterm Examination (In-class)

11/02 System Verilog Basics

- New System Verilog constructs and features
- Design example using System Verilog
- Final Project Released.
- Assignment 3 due. Assignment 4 released.

11/09 Verification using System Verilog

- Randomized testing and coverage in System Verilog
- Assertions and assertion based verification
- Project discussion

11/16 Reconfigurable logic design (FPGAs)

- FPGA architectures, synthesis for FPGA.
- Assignment 5 (FPGA assignment) released. Assignment 4 due.

11/23 Advanced Synthesis and Timing Analysis

- What's inside a CAD tool: two/multi-level synthesis, tech. mapping
- Static timing analysis and timing optimization.

11/30 Power and Energy Consumption

- Understanding and modeling dynamic and leakage power
- Power optimization techniques: clock gating, power gating, DVFS
- Assignment 5 due.

[Thanksgiving Break]

12/07 High Level Synthesis

- What is high level synthesis?
- Control and data flow graph (CDFG) representation
- Allocation, binding, scheduling, resource allocation
- Assignment 6 due.

12/14 Project Presentations

- Each group presents for 5 minutes.

Moses Center Statement of Disability

If you are student with a disability who is requesting accommodations, please contact New York University's Moses Center for Students with Disabilities at 212-998-4980 or mosescsd@nyu.edu. You must be registered with CSD to receive accommodations. Information about the Moses Center can be found at www.nyu.edu/csd. The Moses Center is located at 726 Broadway on the 2nd floor.