CMOS Process and Device Simulation Design Assignment

EE4623 Assignment

Group: F63/F61

Group Member	Contribution
Jiao Yubiao (U2223043B)	Oxidation Time, Optimization
Gao Yuxiang (U2221919J)	Intro, Oxidation temperature, script
Tao Ran (U2221029A)	Intro, Gate Length, SWB setup
Wang Beiyi (U2222955G)	Implantation Energy, Conclusion
Wang Yaoli (U2223433C)	Intro, Implant dose, Optimization

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

Introduction

This report aims to investigate the complete NMOS process-device investigation by using Sentaurus (SWB), based directly on the default parameters given and requirements provided in the exercise document. The entire workflow is structured into clear numbered tasks, each defining a specific DOE or simulation stages.

All default parameters given in the documents are

- Substrate doping: p-type: $N_A \approx 1.35 \times 10^{16}\,\mathrm{cm}^{-3}$ $(10\ \Omega \cdot \mathrm{cm})$
- Gate oxide thickness: $t_{ox} = 300$ Å
- V_T-adjust implant energy: $E = 30$ keV
- V_T-adjust implant dose: $Q = 2 \times 10^{12}$ cm^{-2}
- Gate oxide Temperature: $\mathrm{temp}_{ox} = 900°\mathrm{C}$

The work begins with restructuring the baseline process flow, followed by theoretical threshold-voltage V_{T0} estimation. And with a series of DOEs, they are constructed to study the influence of gate oxidation conditions, V_T-adjust implant parameters, and channel doping profiles on the device characteristics. Using these process variations, the V_{T0} behavior, cross-sectional structures and doping concentration distributions are extracted and analyzed.

Meanwhile, to evaluate how the major process affects the threshold behavior and short-channel behavior, two separated DOEs are conducted for both long-channel (10μm) and short-channel (1μm) NMOS devices:

1) V_T-adjust implantation DOE: this is to vary the V_T-adjust implantation dose with a fixed gate oxide time and to extract data related.

2) Oxidation DOE: this is to vary the oxidation time with fixed V_T-adjust implantation dose and extract the data related.

For both DOEs, the resulting dataset are plotted as "scattered" optimization figures, including: $\log(I_{DS})$ vs. I_{on}, SS_{lin} vs. $g_{m,lin}$, V_{Tgm} vs. V_{Tlin}. And to observe and analyze the variation trends of V_{Tlin} roll-off as well as DIBL as the function of oxidation time and implant dose.

Finally, for the short-length 1um transistor, DOEs are used to determine the most suitable combination of oxidation time and implant dose. The optimization conclusion is based on the trends observed in the mentioned plots. Therefore, the objective of this report is to develop and validate an optimized process recipe for the 1 um NMOS transistor that preserves its long-channel V_{T0} while improving the on/off current characteristics and reducing short-channel effects across all investigated gate lengths.

Theoretical V_{T0} Equation

$$V_{T0} = -\frac{Q_{dep,\max}}{C_{ox}} + 2\Phi_F = \frac{1}{C_{ox}}\sqrt{4kT\varepsilon_{si}N_A \ln\left(\frac{N_A}{n_i}\right)} + 2\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

Parameter definitions:

- $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$: Gate-oxide capacitance per unit area

- $Q_{dep,\max}$: The maximum charge stored in the bulk in the depleted region
- $\Phi_F = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$: Fermi potential of the substrate
- N_A: Channel acceptor doping concentration
- n_i: Intrinsic carrier concentration
- ε_{si}, ε_{ox}: Permittivities of Silicon and Silicon Oxide

Theoretical V_{T0} Calculation

Parameters	Symbol/Formula	Value/Unit
Doping Concentration	N_A	1.35×10^{16} cm^{-3}
Gate oxide Thickness	t_{ox}	300 Å $= 3.0 \times 10^{-6}$ cm
Oxide permittivity	$\varepsilon_{ox} = 3.9\varepsilon_0$	3.45×10^{-13} F/cm
Oxide Temperature	T	300 K
Intrinsic Concentration	n_i	1.45×10^{10} cm^{-3}

$$2\frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right) = 2(0.02585)(11.4415) = 0.5916 \text{ V}$$

$$\ln\left(\frac{N_A}{n_i}\right) = \ln\left(\frac{1.35 \times 10^{16}}{1.45 \times 10^{10}}\right) = 11.4415$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.9\varepsilon_0}{3.0 \times 10^{-6}} = 1.15 \times 10^{-7} \text{ F/cm}^2$$

$$V_{T0} \approx 0.73 \text{ V}$$

Long-Channel Threshold Voltage V_{Tlin} Calculation

From $L_{gate} = 2\ \mu m$ and default values, the estimated average channel doping from the doping profile is:

$$N_A = 4.3 \times 10^{16} \text{ cm}^{-3}$$

The equation used for calculating long-channel Threshold Voltage V_{Tlin} is

$$V_{Tlin} = V_{FB} + \gamma\sqrt{2\Phi_{Fp}} + 2\Phi_{Fp}$$

Because there is no body bias, $V_{SB} = 0$, thus:

$$V_{Tlin} = V_{FB} + \gamma\sqrt{2\Phi_{Fp}} + 2\Phi_{Fp}$$

With:

$$V_{FB} = \Phi_{MS}$$

$$\Phi_{MS} = \Phi_M - (\chi_{Si} + E_g/2 + \Phi_{Fp})$$

Parameter table:

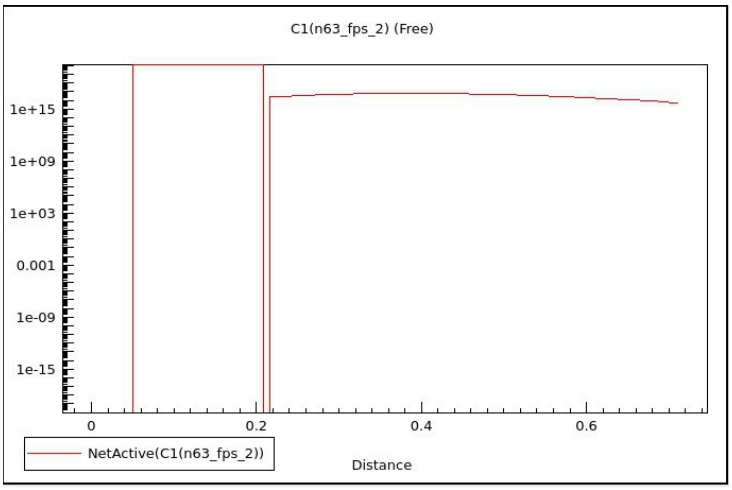

Figure 1: Doping Profile for average channel doping level.

Parameter	Value
Φ_M	4.05 eV
χ_{Si}	4.05 eV
E_g	1.12 eV
n_i	1.45×10^{10} cm^{-3}
N_A	4.3×10^{16} cm^{-3}
t_{ox}	3.0×10^{-6} cm
ε_{ox}	3.45×10^{-13} F/cm

Thus:

$$V_{Tlin} = -0.945 + 0.91\sqrt{2 \times 0.384} + 0.770 = 0.74 \text{ V}$$

Simulation value:

$$V_{Tlin,num} = 0.679 \text{ V}$$

$$\Delta V_T = 0.74 - 0.679 = 0.061 \text{ V} \approx 9\%$$

Two values are reasonably close (within 0.1V), fully consistent with 2D electrostatic effects, graded channel doping and polysilicon depletion not captured by the long-channel analytic model.

Effective Channel Doping Extraction

Using numerical $V_{Tlin} = 0.679$ V:

$$V_{FB} + \gamma\sqrt{2\Phi_{Fp}} + 2\Phi_{Fp} = 0.679$$

Solving gives:

$$N_{A,eff} \approx 3.8 \times 10^{16} \text{ cm}^{-3}$$