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Thin film ferroelectric photonic-electronic memory

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Abstract

To reduce system complexity and bridge the interface between electronic and photonic circuits, there is a high demand for a non-volatile memory that can be accessed both electrically and optically. However, practical solutions are still lacking when considering the potential for large-scale complementary metal-oxide semiconductor compatible integration. Here, we present an experimental demonstration of a non-volatile photonic-electronic memory based on a 3-dimensional monolithic integrated ferroelectric-silicon ring resonator. We successfully demonstrate programming and erasing the memory using both electrical and optical methods, assisted by optical-to-electrical-to-optical conversion. The memory cell exhibits a high optical extinction ratio of 6.6 dB at a low working voltage of 5 V and an endurance of 4×10^4 cycles. Furthermore, the multi-level storage capability is analyzed in detail, revealing stable performance with a raw bit-error-rate smaller than 5.9×10^{-2}. This ground-breaking work could be a key technology enabler for future hybrid electronic-photonic systems, targeting a wide range of applications such as photonic interconnect, high-speed data communication, and neuromorphic computing.

Introduction

In the era of big data and artificial intelligence, conventional electronic computers based on Von-Neumann architecture struggle to meet the stringent demands of data-intensive and massive parallel tasks[1–3]. To address this challenge, photonic integrated circuits (PICs) hold tremendous promise to offer a potential solution to the increasing need for computing power in the coming decades. Exploring transmission, manipulation, processing, and storage of information using optics and photonics could provide powerful solutions[4–7], leveraging the inherent properties such as high bandwidth, high power efficiency, low latency, and high parallelism[8–10]. Notable successes have already been achieved in demonstrating PICs for accelerating tasks, such as non-linear programming[11], signal processing[12–14], photonic neural networks[15–17], and quantum computing[18,19]. However, the lack of optically accessible memory poses a significant hurdle in system design, as it necessitates additional electro-optical and opto-electrical conversion processes during computing. This has led to a growing interest in non-volatile photonic-electronic memory as a means to bridge the gap between the electronic and photonic circuits. Currently, control and data processing predominately occur electrically due to the absence of optical memory. This results in additional loss, latency, and power consumption due to moving the data between different components and hinders the realization of optical in-memory computing. Therefore, an ideal memory for hybrid electronic-photonic systems should possess the following features: (a) Non-volatile nature with high endurance, long retention, multi-level storage capabilities, and zero energy consumption to maintain the data storage; (b) The ability to be programmed and erased both electrically and optically; (c) The non-destructive electrical and optical read processes that can occur simultaneously without conflict; (d) Fully compatible with the fabrication process of both electronic and photonic components.

There have been a few existing reports to realize the non-volatile photonic memory[20–22], with chalcogenide phase change materials (PCM), such as $Ge_2Sb_2Te_5$ (GST) receiving the most attention in recent years[23–30]. They take advantage of the different absorption coefficients of

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GST in its amorphous and crystallization states to modify the intensity of the guided light in the waveguide. However, the reported low extinction ratio (ER) could be one of the drawbacks that limit its applications. In addition, the program/erase processes require pulse engineering, increasing the complexity of peripheral circuit design[23]. Moreover, challenges such as resistance drifting[31,32] arising from structural relaxation, as well as the thermal crosstalk[33,34] in high-density integration of the PCM memories, are yet to be solved. Another method involves the use of the floating-gate structure, where carrier injection into the floating gate changes the refractive index (RI) of the waveguide in a non-volatile way[35,36]. However, they generally require a high working voltage of a few tens of volts and operate at a low speed of a few Hz. Low program/erase endurance is another issue arising from the accumulation of interface traps in the carrier injection process[37,38]. Another method employs the memristor structure where a conductive bridge is created inside the a-Si cladding layer above the Si waveguide using electrical force, resulting in non-volatile modulation of the waveguide[39–41]. However, this approach faces the challenges of poor retention, low endurance, highly stochastic switching, etc[42]. Importantly, most reported non-volatile photonic memory implementations are not electrically readable and electrically controllable, which further narrows their scope of applications in optoelectronic circuits. Furthermore, all the non-volatile photonic memory demonstrations lack a systematic investigation of the endurance and retention properties of the memory cell, which are the key figures of merit (FOMs) in all memory applications.

Ferroelectricity discovered in the doped-HfO_2 thin film has garnered significant attention as a technology enabler for emerging ferroelectric (FE) memory[43–46]. Compared with FE materials in complex perovskite systems[47–49], doped-HfO_2 shows great promise and better performances for non-volatile device applications due to its full CMOS compatibility, high scalability, advantage of retention characteristics, and the ability to maintain ferroelectric properties down to nanometer-level thickness[50,51]. In this work, we demonstrate a non-volatile multi-level photonic-electronic memory by introducing an Al-doped HfO_2 (HAO) FE thin film onto a silicon photonic platform. A 3D monolithic integrated structure introduces the non-volatile property directly on the silicon waveguide, without any additional energy to maintain the optical information. The memory is programmable and erasable both electrically and optically at 1550 nm telecom wavelength, assisted by optical-to-electrical-to-optical (OEO) conversion, while the optical read function is completely optical. The electrical read and optical read processes do not conflict and can happen at the same time. Using a ring resonator structure, the memory cell

achieves one of the highest ERs of 6.6 dB with a low working voltage of 5 V. The performance of the memory is analysed in detail, demonstrating multi-level storage capability with minimal errors. The device exhibits a decent endurance of 4×10^4 cycles. No noticeable change can be observed during the measured 1000 s retention time, and the fitted retention time is estimated to be more than 10 years, proving its good stability and non-volatility. Moreover, our design ensures that the FE thin film is on top of the waveguide and fabrication condition does not affect other photonic components. The fabrication simplicity, size of the unit cell, and the mature large wafer capability provide great potential for our design to scale up. Based on our current results, our non-volatile memory could pave the way for hybrid electronic-photonic systems, with applications including photonic interconnect, high-speed data communication, and neuromorphic computing.

Results

Design of non-volatile photonic-electronic memory cell

The non-volatile photonic-electronic memory cell is based on a ring resonator structure, as illustrated in Fig. 1a, while Fig. 1b provides the zoom-in cross-section of the ring region. The microscope image of the fabricated memory cell is shown in Fig. 1c. Ring resonators are used for their advantage of better tunability, easier design, and fabrication. Light is coupled in and out of the chip by using two partially etched grating couplers. In the ring resonator region shown in Fig. 1b, an FE capacitor is directly fabricated on the Si waveguide using 10 nm-thick HAO as the dielectric layer, offering an effective modulation of the silicon waveguide by the FE polarization. In the capacitor, a 13 nm indium tin oxide (ITO) serves as the top transparent electrode, while the p-type lightly doped Si waveguide with a hole concentration (N_h) around $1 \times 10^{17}\,cm^{-3}$ serves as the bottom electrode. A larger area of nickel is deposited on the Si bottom electrode to lower the parasitic resistance in the measurement. It should be noted that the fabrication of the FE capacitor is independent of the fabrication of waveguide components, and can be fabricated after all the foundry processes. The anneal of the HAO layer requires only 650 °C temperature, minimizing any effect on other photonic active and passive components.

Upon applying different voltages on top and bottom electrodes, the dipoles inside the HAO film can be switched, after which a remnant polarization (P_r) corresponding to the applied electric field maintains. This P_r modifies the N_h in the p-type Si waveguide underneath the HAO, and thereby changes the RI of the waveguide. The free-carrier concentration is changed and held in place by the electrostatic force from the ferroelectric layer, namely the electrostatic doping effect[52]. As shown by the
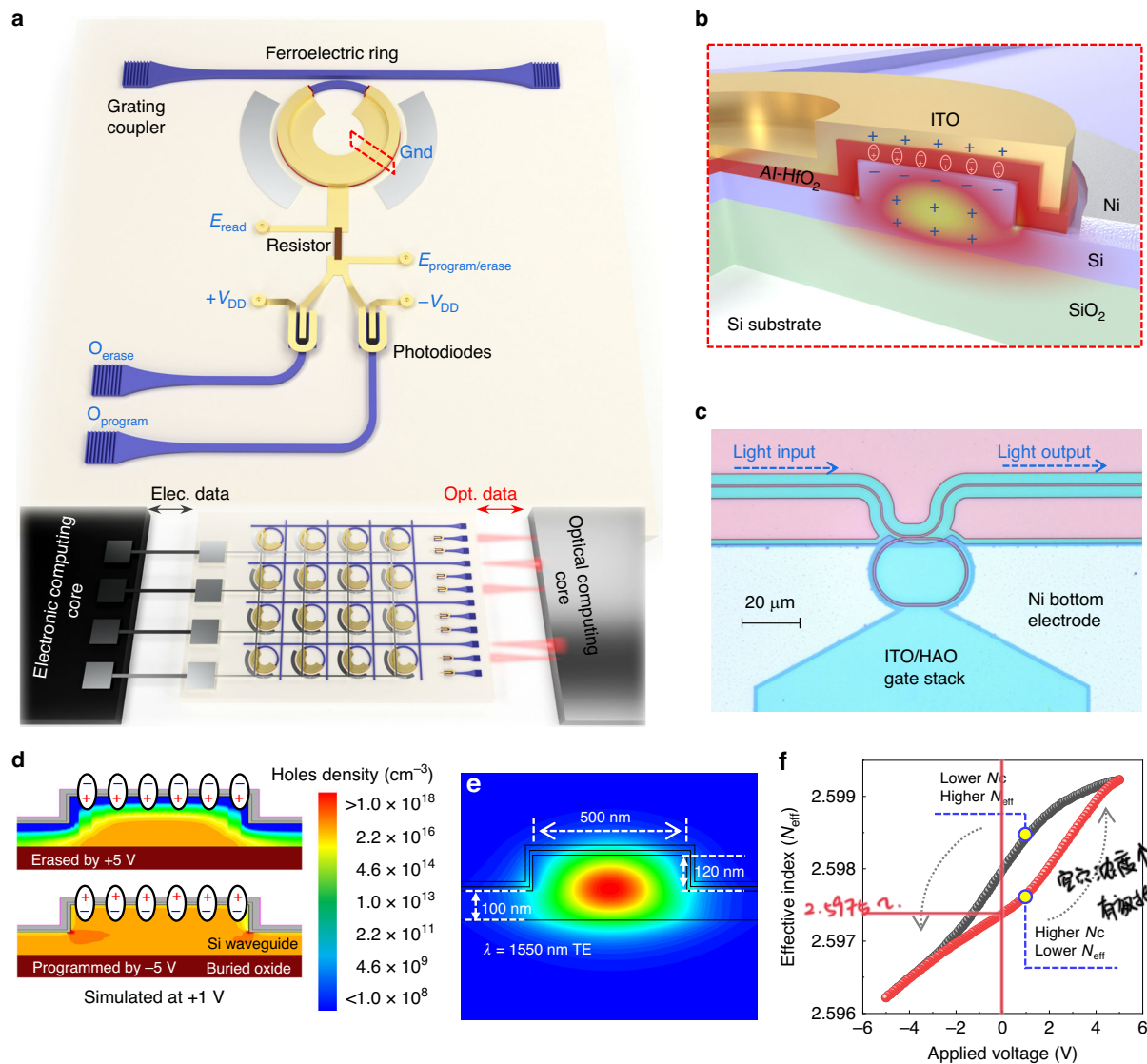
Fig. 1 Schematic and simulation results of the non-volatile photonic memory. a The 3D schematic of the non-volatile photonic memory cell with both electrical programming/erasing and optical programming/erasing functionalities. Ferroelectric material Al-doped HfO_2 (HAO) is deposited on top of the silicon waveguide to modulate the carrier concentration in the waveguide, such that the information can be stored in a non-volatile way. Peripheral circuits are designed for mixed-mode operations, for which two photodiodes are used for optical programming/erasing. The optical signal can be read out from the grating coupler of the bus waveguide. Electrical programming/erasing is enabled by the direct electrical bias, then delivered by the metal line to the HAO. Electrical reading relies on the E_{read} port by small signal sensing. This memory can serve as the interface for future hybrid electronic-photonic system to simplify the peripheral circuit design. **b** Cross-sectional zoom-in view on the ring. The Si waveguide is P-type doped to ensure the carrier concentration required by the ferroelectric switching. Light will transmit in the Si waveguide core under the non-volatile modulation of the ferroelectric material HAO. By switching the HAO, carrier concentration inside the waveguide is changed, resulting in a different propagation constant of the light. Therefore, the resonance wavelength of the optical ring resonator will be non-volatilely modified and can be viewed as a stored state. ITO serves as the top electrode to ensure low optical absorption as well as good ferroelectricity. **c** The microscope image of the non-volatile photonic switch. **d** Simulated carrier concentrations at 1 V biasing voltage after being initiated by voltages with opposite polarity. A distinct difference in carrier concentration under these two states is shown. **e** Optical mode profile simulation of the waveguide. Single transverse-electric mode is confirmed. **f** The effective index of the optical mode versus the applied voltages was simulated based on the carrier concentration simulation results. The direction of the hysteresis loop (counter-clockwise) proves the FE memory principle theoretically

cross-sectional view in Fig. 1b and N_h simulation results in Fig. 1d, when negative (positive) voltage is applied on the top electrode, the dipoles will be switched to a direction that can attract (repel) the holes, then the N_h in the Si will be higher (lower). Due to the permanent dipole moment after switching, the change in N_h is non-volatile

and directly related to the P_r. The accumulated (depleted) holes decrease (increase) the RIs and the propagation constant, leading to the blue (red) shift of the resonance peaks. Considering the waveguide dispersion in the sub-micron silicon waveguide and the resonant phenomenon in the micro-ring, this effect can be quantified by[53]

$$\Delta\lambda_{res} = \frac{\Delta n_{eff}\lambda_{res}}{n_g}$$

where Δn_{eff} is the effective index change induced by the difference in carrier concentration; n_g is the group index; λ_{res} is the center wavelength of one resonance peak; $\Delta\lambda_{res}$ denotes the wavelength shift. This shifted resonance peak position can then be optically read out by either measuring the optical spectrum when the input is a broadband light or the output power when the input is a tuneable laser aligned to a resonance peak. Non-destructive electrical reading is achieved by sensing the capacitance change using a small electric signal before and after the FE switching[54]. Noted that the readings are based on different mechanisms, thus the optical reading and electrical reading can operate independently without any conflict in future electronic-photonic systems as shown in Fig. 1a.

We aim to design a photonic-electronic memory that is capable of mixed-mode operations, where optical/electrical programming/erasing are all feasible. As shown in Fig. 1a, electrical programming/erasing biases can be directly applied from the $E_{program/erase}$ port to control the FE switching. Optical programming/erasing will rely on two photodiodes (PDs) to convert the optical power to electrical bias. These two PDs are constantly reverse-biased. When optical power is presented on the PDs, PDs serve as current sources, which can deliver the applied reverse-bias voltages to the FE capacitor assisted by a pull-up resistor. In this way, optical power can be used for programming/erasing. Upon programming/erasing, the results will be read out from the grating coupler optically, or from the E_{read} port electrically.

Based on the device design, the simulations have been conducted on the ring region accordingly to confirm the working principle, as shown in Fig. 1d–f for N_h distribution, optical mode profile, and n_{eff} simulation, respectively. The FE capacitor on the Si waveguide is erased/programmed using voltages with different polarities and read at 1 V. Note that the 1 V reading voltage provides a larger memory window but not necessary. The device shows decent memory window at 0 V. The non-volatility does not depends on the reading voltage. Pronounced differences in N_h (> 8 orders difference at +1 V reading voltage) are found in the Sentaurus TCAD simulation in Fig. 1d, which is expected due to the large and opposite P_r after programming and erasing. The waveguide is

designed to have an etching depth of 120 nm and a width of 500 nm. Single-mode operation is confirmed by the Lumerical MODE simulation, shown in Fig. 1e. Due to the large N_h difference, the simulated optical effective index response in Fig. 1f shows a counter-clockwise hysteresis loop representing the effect of ferroelectric-induced modulation of N_h on optical phase, which can be further converted to resonant peak shift.

Non-volatile photonic-electronic memory cell performance

The devices were fabricated after the device design and the simulation confirmation. Detailed fabrication processes, SEM/TEM characterizations, and the electrical characterizations of the FE film can be found in the Method section as well as the supplementary material Fig. S1 and S2. When measuring the devices, the operational speed is limited by the carrier generation/recombination time of Si for the FE switching process[46]. Therefore, all the measurements were carried out with a visible laser irradiating on the ring region to boost the electron generation/recombination speed. The power spectra (Fig. 2a) of the optical ring resonator were measured under a reading voltage of 1 V after programming and erasing using −5 V and 5 V, respectively. An excellent ER of 6.6 dB is shown, which is one of the highest ER among the reported works considering the low voltage used. For practical applications, photodetectors will be used to read the stored state. In this case, a high ER is preferred as it can lower the bit-error-rate (BER) of the stored information. A maximum peak difference of 0.14 nm is also featured in this test. Quality factors of the resonance peaks are different in these two states, indicating that the carrier concentrations are varying in different states. Detailed studies of the quality factor are shown in supplementary material Fig. S3. In addition to the spectra, we extracted the resonance peak positions and plotted them in Fig. 2b, in which clear counter-clockwise hysteresis loops can be observed for both 4 V and 5 V sweeping voltages. The hysteresis direction is critical here because it can validate the working principle. When the biasing voltage is sweeping from −5 V to 5 V, the FE layer HAO is first programmed by −5 V, resulting in hole accumulation in the waveguide. The effect of hole accumulation is retained by the P_r of the HAO layer, so the resonance peaks in the forward (−5 V to 5 V) sweeping is blue shifted compared with the resonance peaks in the backward (5 V to −5 V) sweeping. The reading voltage is selected as 1 V to maximize the output difference at different states. The transmission hysteresis loop is also calculated and provided in supplementary material S4. The electrical memory properties are also confirmed from the polarization-voltage relationship measured using the positive-up-negative-down (PUND) method, as shown in Fig. 2c. The experimentally measured hysteresis loop is
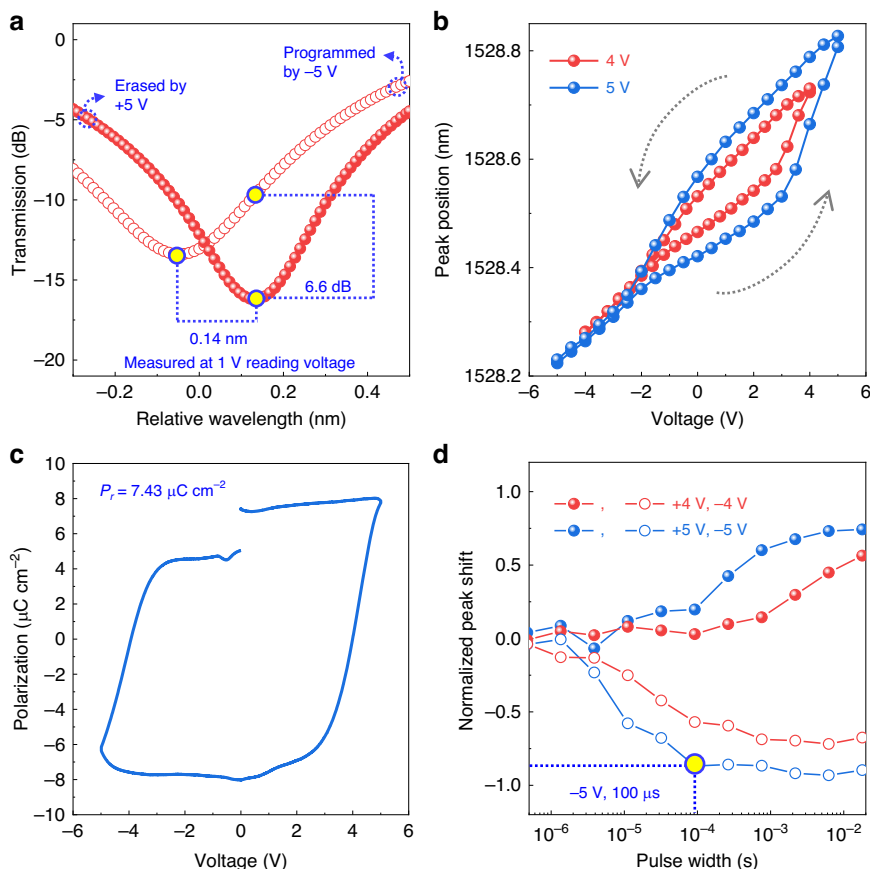
Fig. 2 <u>**Measurement results**</u> of the non-volatile photonic memory. **a** Measured transmission spectra of the ring resonator at different voltages. The device was erased by a 5 V pulse first and then programmed by a −5 V pulse. A high extinction ratio of 6.6 dB and a peak difference of 0.14 nm were obtained at 1 V reading voltage. **b** Measured resonance peak position versus the applied voltages. The counter-clockwise hysteresis loops are caused by ferroelectricity. **c** *P-V* loops measured by PUND method of the device with 10 nm HAO, featuring a remnant polarization of 7.43 μC cm^{-2}. **d** Measured resonance peak shift versus the input pulse width with pulse amplitude of 4 or 5 V. 90% of the maximum peak shift can be achieved by a −5 V, 100 μs pulse, featuring a 10 kHz writing speed of the memory cell

direct evidence for the proper functioning of our non-volatile photonic-electronic memory.

As an integral part of all memory applications, the speed performance of programming, reading, and erasing operations is important. Here, to determine the high-speed performance of the memory cell, <u>we examined the operation speed by using electrical pulses with the same amplitude (4 V or 5 V) but varying pulse width (ranging from 2 ns to 2 ms).</u> The amount of resonance peak shift is used to assess the switching performance under each applied electrical pulse, as depicted in Fig. 2d. The result shows that 90% of the maximum resonance peak shift can be achieved by a −5 V, 100 μs electrical pulse. Higher voltage generally offers a higher operating speed due to a larger electric field across the FE layer. Taking the p-type substrate into account, the switching of the HAO FE layer is easier when applying negative voltages than positive voltages because more holes in the Si waveguide are available to respond to the FE switching (see electrical

characterizations of FE switching speed in the supplementary material Fig. S2). For our memory cell, negative voltages are used for the programming process since the speed for information storage is more important.

Demonstration of multi-mode and multi-level storage functions

Taking advantage of the FE material, where the external voltage bias can control the induced P_r with partial switching capability, our non-volatile photonic-electronic memory is able to realize multi-level storage in a simple manner. <mark>By applying different programming voltages, the maximum achievable peak wavelength differences and ERs can be controlled by the induced P_r.</mark> Multi-level storage, as well as the mixed-mode operation, are proved to be feasible here, with details shown in Fig. 3. The measurement circuit design is shown in Fig. 3a, where optical/electrical programming/erasing/reading functions are equipped. To induce the FE switching and

Fig. 3 (See legend on next page.)
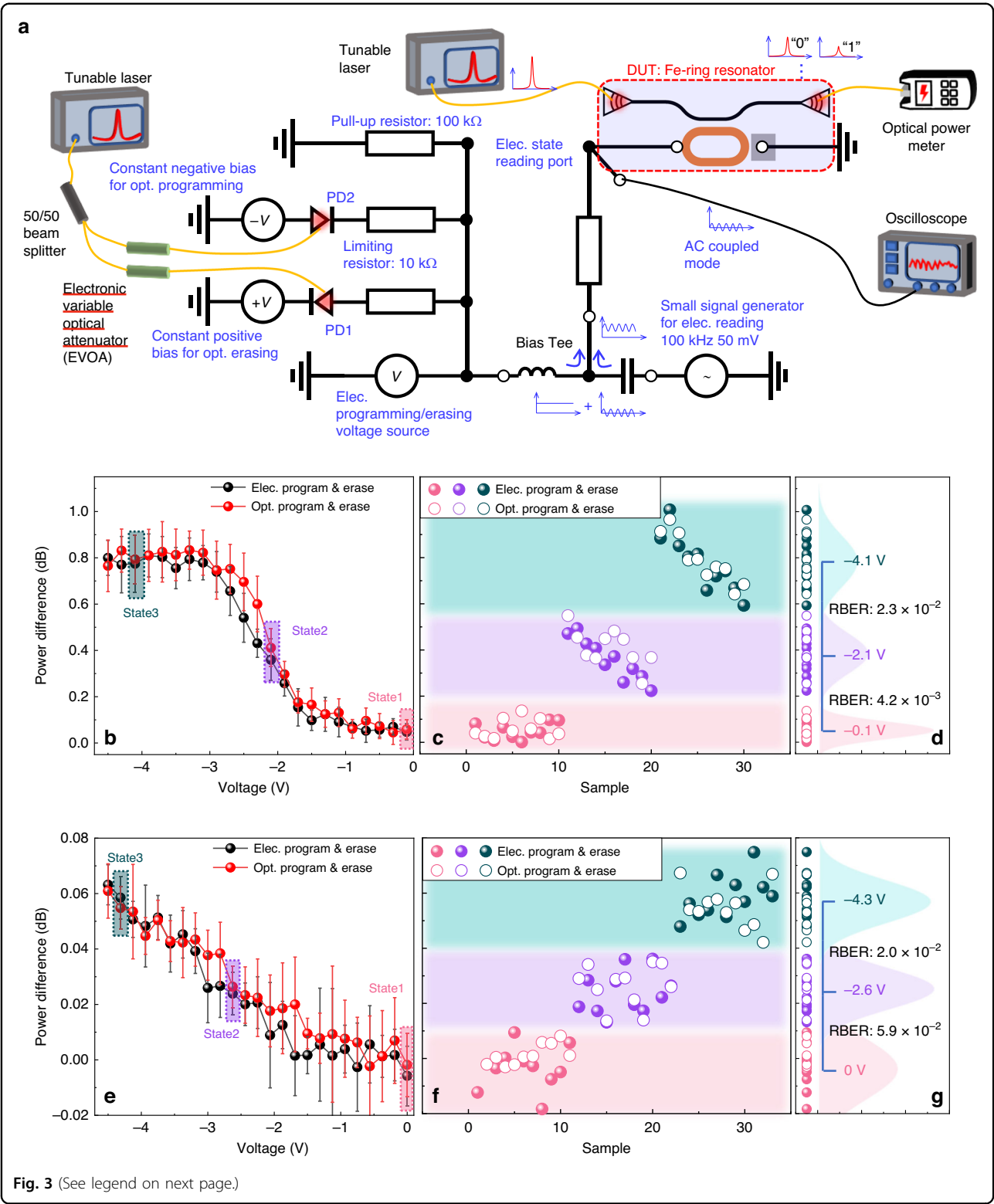
(see figure on previous page)

Fig. 3 Measurement setups and results for mixed-mode erasing/programming operation. a The measurement setups for mixed-mode operation. Optical erasing/programming is realized by two constantly reverse-biased PD1/PD2, respectively. Two EVOAs are used to adjust the optical power on the PDs and the photocurrent from the PDs, and finally, it controls the DC bias being delivered to the bias tee. Electrical erasing/programming was carried out by a single voltage source. Optical reading was then enabled by an optical power meter, while an oscilloscope provided the electrical reading function. **b** The optical power differences are read out at 1 V reading voltage after each erasing (4.5 V)/programming (-0.1 V ~ -4.5 V) operation in both optical/electrical ways. Due to the losses and noises in both the electrical circuit and the optical circuit, small deviations are shown between these two curves. Taking the losses and noises in both electrical/optical ways into consideration, three states can be clearly distinguished, which are state1 (-0.1 V), state2 (-2.1 V), and state3 (-4.1 V), corresponding to non-switched, partially-switched, and fully-switched FE state, respectively. The error bars are defined by the standard deviation of 10 data points. **c** Data points are shown in this figure for electrical operation (solid circles) and optical operation (hollow circles). **d** To verify the practicality of the multi-level operation, RBERs are calculated between each consecutive state. Here, the highest RBER is 2.3×10^{-2} between state1 and state2, which can be lowered to less than 10^{-12} by LDPC coding. **e** The electrical reading function of this readout circuit. Power differences are read out from an oscilloscope by sensing the magnitude of the small signal at 100 kHz. Considering the small deviations between electrical operation and optical operation, similar three states can be used for data storage, corresponding to non-switched and fully-switched state, respectively. The error bars are defined by the standard deviation of 10 data points. **f** Data points for these two states are shown for electrical operation (solid circles) and optical operation (hollow circles). **g** A maximum RBER of 5.9×10^{-2} is calculated between these two states, showing great reliability of the electrical readout function of the designed circuits

programming/erasing the memory cell, it is crucial to create enough DC bias on the FE capacitor. Here in the circuit, a bias tee is used to deliver the DC voltage from the voltage input (DC port of bias tee) to the device (RF + DC port of bias tee). The DC voltage for programming/erasing can be generated either optically or electrically: (a) Optical programming/erasing is realized by two constant reverse-biased PDs, while two electrically controlled EVOAs are used to tune the optical power intensity on these two PDs. Noted that fiber-coupled PDs on separated chips are used in the proof of principle experiment. The output photocurrents from the PDs flow through a pull-up resistor, which can create DC voltages at the DC port of the bias tee. The constant positive/negative DC bias being delivered to the input of the bias tee is therefore related to the optical power on the PDs. (b) Electrical programming/erasing is realized by a voltage source that directly produces the DC voltage into the bias tee, while in the meantime, both PDs are kept in the off state by turning off the optical power using EVOA. After optical/electrical erasing/programming, our memory can be read out both optically and electrically at the same time: (a) Optical readout is conducted by having a tunable laser input aligned with a resonant peak and measuring the output power using an optical power meter, where different storage states result in different optical power outputs. (b) Electrical readout relies on sensing the capacitance using a small signal input at the RF port of the bias tee, which is a non-destructive measurement different from the PUND method. The small signal is generated by a signal generator with a frequency of 100 kHz and a magnitude of 50 mV. The impedance of the ITO/FE/Si capacitor is changed along with the FE switching and can then be read out by the magnitude of the small signal. These working principles of optical/electrical programming/erasing/reading guide the following testing. Note

that a small AC signal introduces a negligible difference in the optical reading considering an averaged power reading time of more than 10 μs. Thus, the optical reading and electrical reading can be simultaneously realized.

Multi-level storage was first demonstrated by optical reading after electrically/optically programming/erasing, as shown in Fig. 3b. Starting at 0 V, the memory cell was erased by a $+4.5$ V pulse before being programmed by negative voltages ranging from -0.1 V to -4.5 V, and read under a reading voltage of 1 V. The length of the pulse is long enough to ensure the switching of the FE layer between each state. These voltage pulses for programming/erasing are generated either electrically or optically, without the requirement of prior knowledge for the driving source. Considering the noise and drift of the system, three states are available for this device using different programming voltages of -0.1 V, -2.1 V, and -4.1 V, which correspond to non-switched, partially switched, and fully switched FE states, respectively. Raw data points repeating 10 times for these three states are shown in Fig. 3c. The raw bit-error-rate (RBER)[55] between each consecutive state, which is not larger than 2.3×10^{-2}, as shown in Fig. 3d.

The memory cell was erased by $+4.5$ V and then programmed by negative voltages ranging from -0.1 V to -4.5 V. The readout is measured from frequency domain output at 100 kHz in Fig. 3e, showing three clearly distinguishable states with a maximum RBER of 5.9×10^{-2} between the states, as illustrated in Fig. 3f and g. Apart from this simple circuit for electrical reading, other methods have been reported on the FE capacitor reading in either a destructive way[56] or a non-destructive way[54] with better accuracy.

These RBERs all meet the requirements for utilizing low-density parity check (LDPC) error correction coding and can be smoothly lowered to less than 10^{-12} by LDPC
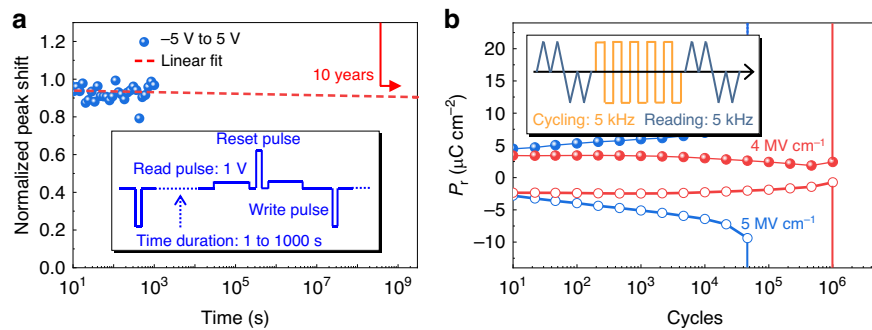
Fig. 4 Reliability testing results of the non-volatile photonic memory. a Measured peak shift at 1 V biasing voltage versus retention time at room temperature. Write and reset voltages are −5 V and 5 V, respectively. Retention time ranges from 1 s to 1000 s. No obvious degradation was observed. **b** The endurance measurements of the HAO thin film give a minimum endurance of 4×10^4 cycles at 5 V working voltage and 1×10^6 cycles at 4 V. A low cycling frequency of 5 kHz was used to ensure an effective stressing to the HAO thin film. Solid and hollow circles are for positive voltages and negative voltages, respectively

coding[57,58]. Besides the multi-level storage and mixed-mode operation, the simplicity of our multi-level storage realization, in which no pulse engineering is required, is another significant improvement over other implementations of non-volatile photonic-electronic memory. The memory driving system design can therefore benefit from the simplicity of the driving strategy of our memory cell.

To verify the non-volatile property as well as the reliability of our memory cell, retention, and endurance tests are conducted, as depicted in Fig. 4. In the inset of Fig. 4a, the memory cell was erased and programmed by ±5 V pulses and read under a biasing voltage of 1 V after a time duration ranging from 1 s to 1000 s at room temperature. No obvious degradation was observed within the 1000 s measurement time, and the fitting shows more than 10 years of estimated retention. The retention tests here show the non-volatility of our memory cells. The endurance tests were conducted on a dummy FE capacitor which excludes all the parasitic capacitance in our device. As shown in Fig. 4b, a square pulse train with a cycling frequency of 5 kHz was used to ensure effective electrical stressing and switching of the FE capacitor. The electrical field amplitudes were set to be 4 and 5 MV cm^{-1}, corresponding to the operating voltages of our memory cell. The endurance of our HAO thin film increases with a decreasing E-field. A minimum endurance of 4×10^4 cycles at 5 V operation voltage and 1×10^6 cycles at 4 V is obtained. This can be improved by interface engineering between Si and HAO layers[59–61].

Discussion

In our memory cell, the BER for electrical reading can be improved by implement a capacitance readout circuit[54,56]. The BER for optical reading is mainly limited by the ERs and Q-factors of the optical ring resonator. The
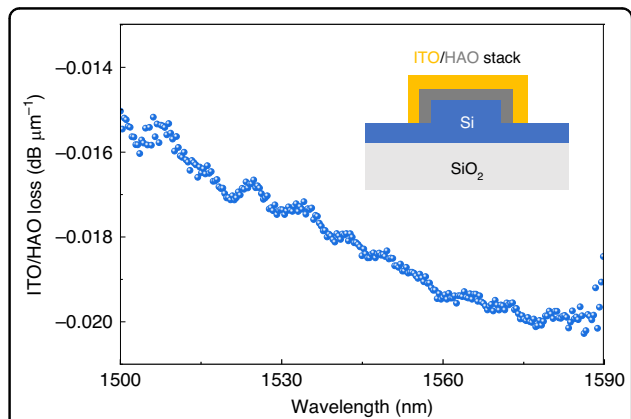

Fig. 5 Loss test of the ITO/HAO gate stack on Si waveguide.
13 nm ITO and 10 nm HAO were deposited on the Si waveguide, which is the same gate stack as the memory cell. The loss from the Si waveguide itself was excluded. In this work, ITO/HAO covers about 70 μm waveguide in the ring resonator region, resulting in an acceptable optical loss of about 1.26 dB

extinction ratio can be improved by adding a tunable coupler in the ring to match the critical coupling condition, while the Q-factors are related to the loss of the waveguide. Waveguide loss is strongly related to the lithography and plasma etching step, which have not been fully optimized in this work. Much better results can be expected if the process in commercialized foundries is utilized with waveguide loss of less than 1 dB cm^{-1}. Understanding the additional loss caused by the ITO/HAO gate stack is more important here. Measurements were conducted on the Si rib waveguide with ITO/HAO stack on it, as depicted in the inset of Fig. 5. The additional loss of ITO/HAO stack per transmission length was tested and calculated by subtracting the loss of the bare Si rib waveguide. In Fig. 5, additional loss for ITO/HAO is measured to be 0.018 dB μm^{-1}, which shows the

transparency of our ITO thin film at telecommunication wavelength. In our device, the ITO/HAO covers about 70 μm length on the ring region, corresponding to an acceptable optical loss of around 1.26 dB for this application. A trade-off has to be made here between the conductivity and the transparency of the ITO thin film. A better conductivity results in a more severe photon absorption in the ITO film, degrading the Q-factors of the optical ring resonator and ERs of the memory cell. By lowering the carrier concentration of the ITO thin film in the deposition process, the transparency enhances, but higher parasitic resistance of the ITO/HAO/Si MIS capacitor would degrade its high-speed performance. A possible solution is to reduce the thickness of ITO thin film while keeping its conductivity using the post-annealing process after ITO deposition[62]. Other transparent electrodes can also be used, such as ZnO[63] and CdO[64].

In the current proof of principle stage, the full single-chip integration of resistors, PDs, and bias tee, is not achieved. The discrete components might bring in noise and loss in the measurement process. On-chip components are necessary to improve overall performance. Actually, on-chip waveguide-coupled PDs[65], on-chip resistors, and on-chip bias tee[66], have already been reported. The integration with other photonic and electronic components for the future hybrid electronic-photonic system is straightforward as the structure is designed to be fully compatible with photonic foundry processes. The maximum temperature during the FE layer fabrication, approaching 650 degrees Celsius, is unlikely to affect the doping profile, the material properties and device performance. One of the potential issues for the full integration is the heat crosstalk. The FE photonic memory cell has negligible heat generation due to its capacitor-like nature. The supporting electronic components can be placed at a distance to isolate the heat transmission. To further improve the thermal stability, active wavelength locking techniques can be introduced as an alternative to the Peltier cooler.

The performance is also not superior to mature technologies, but mainly due to the material contamination and lack of process optimization. The switching speed is mainly limited by the insufficient carrier concentration of the silicon waveguide layer, which can be improved by optimizing the doping profile in the waveguide[54]. Besides, reducing the parasitic capacitance and increasing ITO conductivity will also help increase the speed by lowering the RC delay. The main limitation for the endurance is the defect density of the Si-HAO interface, which can be improved by interface engineering and optimizing the fabrication process[59–61]. Despite not demonstrating an array, our monolithic integration process provides high scalability. The fabrication complexity remains constant irrespective of the device number. Using photonic foundry processes, the unit cell size can also scale down to 5 μm, allowing a 1000×1000 array within a typical chip size of 20×20 mm.

In conclusion, we have reported here a non-volatile programmable photonic-electronic memory cell with multi-level storage and mixed-mode operation functionalities, enabled by the employment of an Al-doped HfO_2 ferroelectric layer with low operating voltage and a transparent ITO electrode with low optical absorption on top of the silicon waveguide. In our demonstration, the information is stored optically/electrically induced by the remnant polarization of HAO and can be read out optically by the optical power meter. We achieve one of the highest ERs of 6.6 dB at a 5 V operation voltage, with an endurance of 4×10^4 cycles and an estimated retention of more than 10 years. A comparison with state-of-the-art nonvolatile photonic memories is shown in Table 1. This work shows the considerable potential of ferroelectric photonic devices for future hybrid electronic-photonic platforms, such as photonic interconnect, optical neuromorphic computing, data center, and optical communication applications, where non-volatile photonics are indispensable.

Methods
Device fabrication process flow

The ring resonator and the grating coupler were patterned using the Raith EBPG-5200 electron beam lithography system and etched by Oxford PlasmaPro 100 Cobra ICP RIE etching system using $CHF_3/O_2/Ar$ on an SOI wafer. 250 nm SiO_2 was then deposited by Oxford PlasmaPro 100 PECVD as the cladding layer, followed by the opening of an operational window directly on the ring resonator region using dry etching. After that, 10 nm HAO was deposited using Picosun ALD at 300 °C. The doping concentration of aluminum is 1:30 controlled by the cycle ratio of Al and Hf. Tungsten was deposited by Sputtering System - AJA UHV as the top electrode. Rapid thermal annealing was performed by the RTP system from Annealsys. After that, Tungsten top electrode was replaced by ITO top electrode deposited using RF-sputtering by Sputtering System - AJA UHV. Finally, the bottom electrode Ni was deposited by the ebeam evaporation system E-Beam Evaporator - AJA UHV. Detail flow charts and TEM figures can be found in supplementary materials Fig. S1.

Measurement setup for the mixed mode operations

For the optical programming/erasing function, the output from a C-band EDFA (Fiberprime) is split into two paths and followed by 2 EVOAs (Thorlabs) to control the optical power. InGaAs fiber pigtailed PDs (Beijing Lightsensing) are used to convert the optical power to DC

Table 1 Performance comparison among state-of-the-art nonvolatile photonic memory technologies

Ref.	Method/ material	Mixed mode	Multi-level	Endurance (cycles)	Retention	Extinction ratio (dB)	Writing speed	Writing voltage	Writing power
Li [23]	PCM: GST	OR OW	✓	\	\	1.55	250 ns	\	680 pJ
Zhou [24]	PCM: GST	OR EW	✓	100	\	4.13	50 ns	7 V	7 nJ
Farmakidis [25]	Plasmonic PCM: GST	✓	✓	\	\	0.0305	20 ns	0.35 V	16 pJ
Delaney [26]	PCM: Sb_2Se_3	OR OW	×	\	\	7	400 ns	\	14 nJ
Zhang [28]	PCM: GSST	OR OW EW	×	\	\	42	1 μs	24 V	5.5 μJ
Chen [29]	PCM: SST	OR ER EW	✓	>100	1 h	0.088	2 ns	2.45 V	\
Meng [30]	PCM: GSSe	OR EW	✓	$>5 \times 10^5$	\	12	500 ms	10 V	400 nJ
Song [35]	Floating Gate: Poly-Si	OR EW	✓	\	\	12.7	600 ms	20 V	20 pJ
Grajower [36]	Floating Gate: SiN	OR EW	×	\	\	0.4	\	110 V	\
Tossoun [39]	Memristor: InP	OR ER EW	✓	$>1 \times 10^3$	12 h	12.7	300 ps	5 V	0.36 pJ
Emboras [40]	Plasmonic Memristor: Ag	OR EW	×	\	\	0.04	10 ms	9 V	750 pJ
This work	Ferroelectric-SOI: HAO	✓	✓	$>1 \times 10^6$ @ 4 V	1000 s (measure) 10 yrs. (fit)	6.6	100 μs	5 V	5.05 nJ

OR optical read, *OW* optical write, *ER* electrical read, *EW* electrical write

voltages and then applied to the FE memory cell through a bias tee (Marki Microwave). For electrical programming/ erasing function, the DC voltages are generated by a source measurement unit (Keysight U2722A). For the optical reading function, the input is a tunable laser (Agilent 81949 A), while the output power is measured by an optical power meter (Thorlabs PM100D). For electrical reading, the small signal is generated by an arbitrary waveform generator (Keysight 33500B) and read by using an oscilloscope (LeCroy WavePro). A visible laser (Thorlabs) with 520 nm wavelength and about 5 mW power is used to help the FE switching and a thermo-electric cooler (TEC) is used to reduce the frequency drift. All the optical spectra and peak shifts are measured by an optical spectrum analyser (Yokogawa AQ6370B).

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Data availability
All of the data that support the findings of this study are available in the main text. Source data are available from the corresponding author on request.

Conflict of interest
The authors declare no competing interests.

References
1. Wetzstein, G. et al. Inference in artificial intelligence with deep optics and photonics. *Nature* **588**, 39–47 (2020).
2. Zangeneh-Nejad, F. et al. Analogue computing with metamaterials. *Nat. Rev. Mater.* **6**, 207–225 (2021).
3. Marković, D. et al. Physics for neuromorphic computing. *Nat. Rev. Phys.* **2**, 499–510 (2020).

4. Chen, Z. G. & Segev, M. Highlighting photonics: looking into the next decade. *eLight* **1**, 2 (2021).

5. Alexoudi, T., Kanellos, G. T. & Pleros, N. Optical RAM and integrated optical memories: a survey. *Light Sci. Appl.* **9**, 91 (2020).

6. Goi, E. et al. Perspective on photonic memristive neuromorphic computing. *PhotoniX* **1**, 3 (2020).

7. Li, L. L. et al. Intelligent metasurfaces: control, communication and computing. *eLight* **2**, 7 (2022).

8. Atabaki, A. H. et al. Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip. *Nature* **556**, 349–354 (2018).

9. Sun, C. et al. Single-chip microprocessor that communicates directly using light. *Nature* **528**, 534–538 (2015).

10. Shastri, B. J. et al. Photonics for artificial intelligence and neuromorphic computing. *Nat. Photonics* **15**, 102–114 (2021).

11. De Lima, T. F. et al. Machine learning with neuromorphic photonics. *J. Lightwave Technol.* **37**, 1515–1534 (2019).

12. Tait, A. N. et al. Demonstration of multivariate photonics: blind dimensionality reduction with integrated photonics. *J. Lightwave Technol.* **37**, 5996–6006 (2019).

13. Huang, C. R. et al. A silicon photonic–electronic neural network for fibre nonlinearity compensation. *Nat. Electron.* **4**, 837–844 (2021).

14. Zhang, S. L. et al. Field and lab experimental demonstration of nonlinear impairment compensation using neural networks. *Nat. Commun.* **10**, 3033 (2019).

15. Xu, X. Y. et al. 11 TOPS photonic convolutional accelerator for optical neural networks. *Nature* **589**, 44–51 (2021).

16. Zhang, H. et al. An optical neural chip for implementing complex-valued neural network. *Nat. Commun.* **12**, 457 (2021).

17. Shao, R., Zhang, G. & Gong, X. Generalized robust training scheme using genetic algorithm for optical neural networks with imprecise components. *Photonics Res.* **10**, 1868–1876 (2022).

18. O'Brien, J. L. Optical quantum computing. *Science* **318**, 1567–1570 (2007).

19. Takeda, S. & Furusawa, A. Toward large-scale fault-tolerant universal photonic quantum computing. *APL Photonics* **4**, 060902 (2019).

20. Youngblood, N. et al. Integrated optical memristors. *Nat. Photonics* **17**, 561–572 (2023).

21. Fang, Z. R. et al. Non-volatile materials for programmable photonics. *APL Mater.* **11**, 100603 (2023).

22. Wuttig, M., Bhaskaran, H. & Taubner, T. Phase-change materials for non-volatile photonic applications. *Nat. Photonics* **11**, 465–476 (2017).

23. Li, X. et al. Fast and reliable storage using a 5 bit, nonvolatile photonic memory cell. *Optica* **6**, 1–6 (2019).

24. Zhou, W. et al. In-memory photonic dot-product engine with electrically programmable weight banks. *Nat. Commun.* **14**, 2887 (2023).

25. Farmakidis, N. et al. Plasmonic nanogap enhanced phase-change devices with dual electrical-optical functionality. *Sci. Adv.* **5**, eaaw2687 (2019).

26. Delaney, M. et al. Nonvolatile programmable silicon photonics using an ultralow-loss Sb_2Se_3 phase change material. *Sci. Adv.* **7**, eabg3500 (2021).

27. Ríos, C. et al. Integrated all-photonic non-volatile multi-level memory. *Nat. Photonics* **9**, 725–732 (2015).

28. Zhang, Y. F. et al. Broadband transparent optical phase change materials for high-performance nonvolatile photonics. *Nat. Commun.* **10**, 4279 (2019).

29. Chen, X. Z. et al. Neuromorphic photonic memory devices using ultrafast, non-volatile phase-change materials. *Adv. Mater.* **35**, 2203909 (2023).

30. Meng, J. W. et al. Electrical programmable multilevel nonvolatile photonic random-access memory. *Light Sci. Appl.* **12**, 189 (2023).

31. Ielmini, D. et al. Physical interpretation, modeling and impact on phase change memory (PCM) reliability of resistance drift due to chalcogenide structural relaxation. 2007 IEEE International Electron Devices Meeting. Washington, DC, USA: IEEE, 2007, 939-942.

32. Zhang, W. & Ma, E. Unveiling the structural origin to control resistance drift in phase-change memory materials. *Mater. Today* **41**, 156–176 (2020).

33. Pirovano, A. et al. Scaling analysis of phase-change memory technology. IEEE International Electron Devices Meeting 2003. Washington, DC, USA: IEEE, 2003, 29.6.1-29.6.4.

34. Cai, K. Vertical constrained coding for phase-change memory with thermal crosstalk. 2014 International Conference on Computing, Networking and Communications (ICNC). Honolulu, HI, USA: IEEE, 2014, 312-316.

35. Song, J. F. et al. Integrated photonics with programmable non-volatile memory. *Sci. Rep.* **6**, 22616 (2016).

36. Grajower, M. et al. Non-volatile silicon photonics using nanoscale flash memory technology. *Laser Photonics Rev.* **12**, 1700190 (2018).

37. Aritome, S. et al. Reliability issues of flash memory cells. *Proc. IEEE* **81**, 776–788 (1993).

38. Lee, J. D. et al. Effects of interface trap generation and annihilation on the data retention characteristics of flash memory cells. *IEEE Trans. Device Mater. Reliab.* **4**, 110–117 (2004).

39. Tossoun, B. et al. High-speed and energy-efficient non-volatile silicon photonic memory based on heterogeneously integrated memresonator. *Nat. Commun.* **15**, 551 (2024).

40. Emboras, A. et al. Nanoscale plasmonic memristor with optical readout functionality. *Nano Lett.* **13**, 6151–6155 (2013).

41. Fang, Z. R. et al. Fast and energy-efficient non-volatile III-V-on-silicon photonic phase shifter based on memristors. *Adv. Optical Mater.* **11**, 2301178 (2023).

42. Abbas, H., Li, J. Y. & Ang, D. S. Conductive bridge random access memory (CBRAM): challenges and opportunities for memory and neuromorphic computing applications. *Micromachines* **13**, 725 (2022).

43. Tan, A. J. et al. Experimental demonstration of a ferroelectric HfO_2-based content addressable memory cell. *IEEE Electron Device Lett.* **41**, 240–243 (2020).

44. Müller, J. et al. Ferroelectric hafnium oxide: A CMOS-compatible and highly scalable approach to future ferroelectric memories. 2013 IEEE International Electron Devices Meeting. Washington, DC, USA: IEEE, 2013, 10.8.1-10.8.4.

45. Müller, J. et al. Ferroelectric $Zr_{0.5}Hf_{0.5}O_2$ thin films for nonvolatile memory applications. *Appl. Phys. Lett.* **99**, 112901 (2011).

46. Zhou, Z. P. et al. A metal-insulator-semiconductor non-volatile programmable capacitor based on a $HfAlO_x$ ferroelectric film. *IEEE Electron Device Lett.* **41**, 1837–1840 (2020).

47. Kim, K. & Lee, S. Y. Memory technology in the future. *Microelectron. Eng.* **84**, 1976–1981 (2007).

48. Udayakumar, K. et al. Manufacturable high-density 8 Mbit one transistor–one capacitor embedded ferroelectric random access memory. *Jpn. J. Appl. Phys.* **47**, 2710 (2008).

49. Geler-Kremer, J. et al. A ferroelectric multilevel non-volatile photonic phase shifter. *Nat. Photonics* **16**, 491–497 (2022).

50. Okuno, J. et al. SoC compatible 1T1C FeRAM memory array based on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$. 2020 IEEE Symposium on VLSI Technology. Honolulu, HI, USA: IEEE, 2020, 1-2.

51. Francois, T. et al. Demonstration of BEOL-compatible ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ scaled FeRAM co-integrated with 130nm CMOS for embedded NVM applications. 2019 IEEE International Electron Devices Meeting (IEDM). San Francisco, CA, USA: IEEE, 2019, 15.7.1-15.7.4.

52. Zheng, S. Y. et al. Proposal of ferroelectric based electrostatic doping for nanoscale devices. *IEEE Electron Device Lett.* **42**, 605–608 (2021).

53. Bogaerts, W. et al. Silicon microring resonators. *Laser Photonics Rev.* **6**, 47–73 (2012).

54. Zhou, Z. P. et al. Experimental demonstration of an inversion-type ferroelectric capacitive memory and its 1 kbit crossbar array featuring high CHCS/CLCS, fast speed, and long retention. 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits). Honolulu, HI, USA: IEEE, 2022, 357-358.

55. Freude, W. et al. Quality metrics for optical signals: eye diagram, Q-factor, OSNR, EVM and BER. 2012 14th International Conference on Transparent Optical Networks (ICTON). Coventry, UK: IEEE, 2012, 1-4.

56. Wu, J. X. et al. Monolithic integration of oxide semiconductor FET and ferroelectric capacitor enabled by Sn-doped InGaZnO for 3-D embedded RAM application. *IEEE Trans. Electron Devices* **68**, 6617–6622 (2021).

57. Richardson, T. J., Shokrollahi, M. A. & Urbanke, R. L. Design of capacity-approaching irregular low-density parity-check codes. *IEEE Trans. Inf. Theory* **47**, 619–637 (2001).

58. Djordjevic, I. B. et al. Using LDPC-coded modulation and coherent detection for ultra highspeed optical transmission. *J. Lightwave Technol.* **25**, 3619–3625 (2007).

59. Zhou, J. R. et al. Demonstration of ferroelectricity in Al-doped HfO_2 with a low thermal budget of 500 °C. *IEEE Electron Device Lett.* **41**, 1130–1133 (2020).

60. Cao, R. R. et al. Improvement of endurance in HZO-based ferroelectric capacitor using Ru electrode. *IEEE Electron Device Lett.* **40**, 1744–1747 (2019).

61. Chernikova, A. G. et al. Improved ferroelectric switching endurance of La-doped $Hf_{0.5}Zr_{0.5}O_2$ thin films. *ACS Appl. Mater. Interfaces* **10**, 2701–2708 (2018).

62. Li, E. W. et al. Transparent conductive oxide-gated silicon microring with extreme resonance wavelength tunability. *Photonics Res.* **7**, 473–477 (2019).

63. Li, X. D. et al. A study on the evolution of dielectric function of ZnO thin films with decreasing film thickness. *J. Appl. Phys.* **115**, 103512 (2014).

64. Campione, S. et al. Submicrometer epsilon-near-zero electroabsorption modulators enabled by high-mobility cadmium oxide. *IEEE Photonics J.* **9**, 6601307 (2017).

65. Wang, H. B. et al. High-speed and high-responsivity pin waveguide photodetector at a 2 μm wavelength with a $Ge_{0.92}Sn_{0.08}$/Ge multiple-quantum-well active layer. *Opt. Lett.* **46**, 2099–2102 (2021).

66. Hettrich, H. & Möller, M. Linear low-power 13GHz SiGe-bipolar modulator driver with 7 Vpp differential output voltage swing and on-chip bias tee. 2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM). Coronado, CA, USA: IEEE, 2014, 80-83.