```
`timescale 1ns / 1ps
/**********************************************************************
*
* Module: FullAdd
*
* Author: Noah Hanks
* Class: ECEN 220, Section 3, Fall 2020 - ECEN 220, Section 1, Winter 2020
* Date: 30 Sep 2020
*
* Description: This is a hierarchical design that creates a full adder module then 9
instances of the 1-bit adders to make the circuit
*
*
**********************************************************************/
`default_nettype none

module FullAdd(
    input wire logic a, b, cin,
    output logic s, co
    );

    logic aAndb, bAndcin, aAndcin;
    xor(s, a, b, cin);
    and(aAndb, a, b);
    and(aAndcin, a, cin);
    and(bAndcin, b, cin);
    or(co, aAndb, bAndcin, aAndcin);

endmodule
```