```
`timescale 1ns / 1ps
/**********************************************************************
*
* Module: Add9
*
* Author: Noah Hanks
* Class: ECEN 220, Section 3, Fall 2020 - ECEN 220, Section 1, Winter 2020
* Date: 30 Sep 2020
*
* Description: This module wires the inputs and outputs together to add them and
calls FullAdd
*
*
**********************************************************************/
`default_nettype none

module Add9(
    input wire logic [8:0] a,
    input wire logic [8:0] b,
    input wire logic cin,
    output wire logic [8:0] s,
    output wire logic co
    );

    logic c1, c2, c3, c4, c5, c6, c7, c8;
    FullAdd FA0(.s(s[0]), .co(c1), .a(a[0]), .b(b[0]), .cin(cin));
    FullAdd FA1(.s(s[1]), .co(c2), .a(a[1]), .b(b[1]), .cin(c1));
    FullAdd FA2(.s(s[2]), .co(c3), .a(a[2]), .b(b[2]), .cin(c2));
    FullAdd FA3(.s(s[3]), .co(c4), .a(a[3]), .b(b[3]), .cin(c3));
    FullAdd FA4(.s(s[4]), .co(c5), .a(a[4]), .b(b[4]), .cin(c4));
    FullAdd FA5(.s(s[5]), .co(c6), .a(a[5]), .b(b[5]), .cin(c5));
    FullAdd FA6(.s(s[6]), .co(c7), .a(a[6]), .b(b[6]), .cin(c6));
    FullAdd FA7(.s(s[7]), .co(c8), .a(a[7]), .b(b[7]), .cin(c7));
    FullAdd FA8(.s(s[8]), .co(co), .a(a[8]), .b(b[8]), .cin(c8));




endmodule
```