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`timescale 1ns / 1ps
/**********************************************************************
*
* Module: seven_segment
*
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* Class: ECEN 220, Section 3, Fall 2020 - ECEN 220, Section 1, Winter 2020
* Date: 9 Oct 2020
*
* Description: Sets functions to trll the board which leds on the seven segments to
turn on to display all hexidecimal values.
*
*
**********************************************************************/
`default_nettype none

module seven_segment(
    output logic[6:0] segment,
    input wire logic[3:0] data

    );
    logic [3:0] not_data;

    not(not_data[0], data[0]);
    not(not_data[1], data[1]);
    not(not_data[2], data[2]);
    not(not_data[3], data[3]);

    logic a1, a2, a3, a4;
    and(a1, data[0], not_data[1], not_data[2], not_data[3]);
    and(a2, not_data[0], not_data[1], data[2], not_data[3]);
    and(a3, data[0], data[1], not_data[2], data[3]);
    and(a4, data[0], not_data[1], data[2], data[3]);
    or(segment[0], a1, a2, a3, a4);

    logic b1, b2, b3;
    logic data_0_or_data_1;
    xor(data_0_or_data_1, data[0], data[1]);
    and(b1, data_0_or_data_1, data[2], not_data[3]);
    and(b2, data[0], data[1], data[3]);
    and(b3, not_data[0], data[2], data[3]);
    or(segment[1], b1, b2, b3);

    assign segment[2] =
        (data==4'b0010)?1:
        (data==4'b1100)?1:
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        (data==4'b1110)?1:
        (data==4'b1111)?1:
        0;

    assign segment[3] = (data==4'b0001) || (data==4'b0100) || (data==4'b0111) ||
(data==4'b1010) || (data==4'b1111);
    assign segment[4] = (data==4'b0001) || (data==4'b0011) || (data==4'b0100) ||
(data==4'b0101) || (data==4'b0111) || (data==4'b1001);
    assign segment[5] = (data==4'b0001) || (data==4'b0010) || (data==4'b0011) ||
(data==4'b0111) || (data==4'b1101);
    assign segment[6] = (data==4'b0000) || (data==4'b0001) || (data==4'b0111) ||
(data==4'b1100);




endmodule
```