```
`timescale 1ns / 1ps
/**********************************************************************
*
* Module: FunRegister
*
* Author: Noah Hanks
* Class: ECEN 220, Section 3, Fall 2020 - ECEN 220, Section 1, Winter 2020
* Date: 24 Oct 2020
*
* Description: A loadable flip-flop design to create n-bit loadable registers.
*
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**********************************************************************/
`default_nettype none

module FunRegister(
    input wire logic CLK,
    input wire logic CLR,
    input wire logic INC,
    output wire logic[3:0] Q,
    output wire logic[3:0] NXT
    );

    FDCE my_ff1 (.Q(Q[3]), .C(CLK), .CE(1'b1), .CLR(1'b0), .D(NXT[3]));
    FDCE my_ff2 (.Q(Q[2]), .C(CLK), .CE(1'b1), .CLR(1'b0), .D(NXT[2]));
    FDCE my_ff3 (.Q(Q[1]), .C(CLK), .CE(1'b1), .CLR(1'b0), .D(NXT[1]));
    FDCE my_ff4 (.Q(Q[0]), .C(CLK), .CE(1'b1), .CLR(1'b0), .D(NXT[0]));
    assign NXT =
        (CLR & ~INC)?4'b0000:
        (~CLR & INC)?Q+1:
        Q;

    endmodule
```