```
#-----------------------------------------------------------
# Vivado v2020.1 (64-bit)
# SW Build 2902540 on Wed May 27 19:54:49 MDT 2020
# IP Build 2902112 on Wed May 27 22:43:36 MDT 2020
# Start of session at: Wed Nov 11 18:00:07 2020
# Process ID: 14012
# Current directory: C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab
9/tx/tx.runs/synth_1
# Command line: vivado.exe -log tx_top.vds -product Vivado -mode batch -messageDb
vivado.pb -notrace -source tx_top.tcl
# Log file: C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab
9/tx/tx.runs/synth_1/tx_top.vds
# Journal file: C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab
9/tx/tx.runs/synth_1\vivado.jou
#-----------------------------------------------------------
source tx_top.tcl -notrace
Command: synth_design -top tx_top -part xc7a35ticpg236-1L
Starting synth_design
Attempting to get a license for feature 'Synthesis' and/or device 'xc7a35ti'
INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a35ti'
INFO: [Device 21-403] Loading part xc7a35ticpg236-1L
INFO: [Synth 8-7079] Multithreading enabled for synth_design using a maximum of 2
processes.
INFO: [Synth 8-7078] Launching helper process for spawning children vivado processes
INFO: [Synth 8-7075] Helper process launched with PID 11184
---------------------------------------------------------------------------------
Starting RTL Elaboration : Time (s): cpu = 00:00:07 ; elapsed = 00:00:08 . Memory
(MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
INFO: [Synth 8-6157] synthesizing module 'tx_top'
[C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab
9/tx/tx.srcs/sources_1/new/tx_top.sv:12]
INFO: [Synth 8-6157] synthesizing module 'debounce'
[C:/Users/noahh/Desktop/debounce.sv:15]
INFO: [Synth 8-6157] synthesizing module 'mod_counter'
[C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab7/Stopwatch/Stopwatch.srcs/sources_1/new/mod_counter.sv:16]
    Parameter MOD_VALUE bound to: 500000 - type: integer
    Parameter BIT_NUMBER bound to: 19 - type: integer
INFO: [Synth 8-6155] done synthesizing module 'mod_counter' (1#1)
[C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab7/Stopwatch/Stopwatch.srcs/sources_1/new/mod_counter.sv:16]
INFO: [Synth 8-6155] done synthesizing module 'debounce' (2#1)
[C:/Users/noahh/Desktop/debounce.sv:15]
INFO: [Synth 8-6157] synthesizing module 'tx' [C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab 9/tx/tx.srcs/sources_1/new/tx.sv:16]
```

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INFO: [Synth 8-6157] synthesizing module 'mod_counter__parameterized0'
[C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab7/Stopwatch/Stopwatch.srcs/sources_1/new/mod_counter.sv:16]
    Parameter MOD_VALUE bound to: 5208 - type: integer
    Parameter BIT_NUMBER bound to: 13 - type: integer
INFO: [Synth 8-6155] done synthesizing module 'mod_counter__parameterized0' (2#1)
[C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab7/Stopwatch/Stopwatch.srcs/sources_1/new/mod_counter.sv:16]
INFO: [Synth 8-6157] synthesizing module 'mod_counter__parameterized1'
[C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab7/Stopwatch/Stopwatch.srcs/sources_1/new/mod_counter.sv:16]
    Parameter MOD_VALUE bound to: 8 - type: integer
    Parameter BIT_NUMBER bound to: 3 - type: integer
INFO: [Synth 8-6155] done synthesizing module 'mod_counter__parameterized1' (2#1)
[C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab7/Stopwatch/Stopwatch.srcs/sources_1/new/mod_counter.sv:16]
INFO: [Synth 8-155] case statement is not full and has no default
[C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab 9/tx/tx.srcs/sources_1/new/tx.sv:5
INFO: [Synth 8-6155] done synthesizing module 'tx' (3#1)
[C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab 9/tx/tx.srcs/sources_1/new/tx.sv:1
INFO: [Synth 8-6157] synthesizing module 'SevenSegmentControl'
[C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab7/Stopwatch/Stopwatch.srcs/sources_1/new/SevenSegmentControl.sv:12]
    Parameter COUNT_BITS bound to: 17 - type: integer
INFO: [Synth 8-6155] done synthesizing module 'SevenSegmentControl' (4#1)
[C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab7/Stopwatch/Stopwatch.srcs/sources_1/new/SevenSegmentControl.sv:12]
INFO: [Synth 8-6155] done synthesizing module 'tx_top' (5#1)
[C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab
9/tx/tx.srcs/sources_1/new/tx_top.sv:12]
---------------------------------------------------------------------------------
Finished RTL Elaboration : Time (s): cpu = 00:00:09 ; elapsed = 00:00:10 . Memory
(MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Handling Custom Attributes
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:10 ; elapsed = 00:00:11
. Memory (MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:10 ; elapsed = 00:00:11 .
Memory (MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.007 . Memory
```

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(MB): peak = 1021.457 ; gain = 0.000
INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints
Initializing timing engine
Parsing XDC File [C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab
9/tx/tx.srcs/constrs_1/new/constraints.xdc]
Finished Parsing XDC File [C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab
9/tx/tx.srcs/constrs_1/new/constraints.xdc]
INFO: [Project 1-236] Implementation specific constraints were found while reading
constraint file [C:/Users/noahh/Documents/Vivado/Ecen 220/Labs/Lab
9/tx/tx.srcs/constrs_1/new/constraints.xdc]. These constraints will be ignored for
synthesis but will be used in implementation. Impacted constraints are listed in the
file [.Xil/tx_top_propImpl.xdc].
Resolution: To avoid this warning, move constraints listed in
[.Xil/tx_top_propImpl.xdc] to another XDC file and exclude this new file from
synthesis with the used_in_synthesis property (File Properties dialog in GUI) and
re-run elaboration/synthesis.
Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 1021.457 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.028 .
Memory (MB): peak = 1021.457 ; gain = 0.000
-----------------------------------------------------------------------------
Finished Constraint Validation : Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 .
Memory (MB): peak = 1021.457 ; gain = 0.000
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Start Loading Part and Timing Information
-----------------------------------------------------------------------------
Loading part: xc7a35ticpg236-1L
-----------------------------------------------------------------------------
Finished Loading Part and Timing Information : Time (s): cpu = 00:00:17 ; elapsed =
00:00:20 . Memory (MB): peak = 1021.457 ; gain = 0.000
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Start Applying 'set_property' XDC Constraints
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:18 ;
elapsed = 00:00:20 . Memory (MB): peak = 1021.457 ; gain = 0.000
-----------------------------------------------------------------------------
```

```
INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'debounce'
INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'tx'
---------------------------------------------------------------------------------
---------------
                   State |                     New Encoding |
Previous Encoding
---------------------------------------------------------------------------------
---------------
                      s0 |                               00 |
       00
                      s1 |                               01 |
       01
                      s2 |                               10 |
       10
                      s3 |                               11 |
       11
---------------------------------------------------------------------------------
---------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding
'sequential' in module 'debounce'
---------------------------------------------------------------------------------
---------------
                   State |                     New Encoding |
Previous Encoding
---------------------------------------------------------------------------------
---------------
                    IDLE |                           000001 |
      000
                   START |                           000010 |
      001
                    BITS |                           000100 |
      010
                     PAR |                           001000 |
      011
                    STOP |                           010000 |
      100
                     ACK |                           100000 |
      101
---------------------------------------------------------------------------------
---------------
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding
'one-hot' in module 'tx'
---------------------------------------------------------------------------
Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:18 ; elapsed = 00:00:20 .
Memory (MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------
```

```
---------------------------------------------------------------------------------
Start RTL Component Statistics
---------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
       2 Input    3 Bit       Adders := 1
+---XORs :
                  8 Bit    Wide XORs := 1
+---Registers :
                  3 Bit    Registers := 1
                  1 Bit    Registers := 3
+---Muxes :
       6 Input    6 Bit        Muxes := 1
       2 Input    6 Bit        Muxes := 7
       4 Input    4 Bit        Muxes := 2
       2 Input    4 Bit        Muxes := 1
       4 Input    2 Bit        Muxes := 1
       2 Input    2 Bit        Muxes := 6
       4 Input    1 Bit        Muxes := 2
       2 Input    1 Bit        Muxes := 3
       6 Input    1 Bit        Muxes := 2
---------------------------------------------------------------------------------
Finished RTL Component Statistics
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Part Resource Summary
---------------------------------------------------------------------------------
Part Resources:
DSPs: 90 (col length:60)
BRAMs: 100 (col length: RAMB18 60 RAMB36 30)
---------------------------------------------------------------------------------
Finished Part Resource Summary
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Cross Boundary and Area Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:21 ; elapsed =
00:00:24 . Memory (MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Applying XDC Timing Constraints
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:32 ; elapsed =
00:00:34 . Memory (MB): peak = 1021.457 ; gain = 0.000
```

```
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Timing Optimization
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Timing Optimization : Time (s): cpu = 00:00:32 ; elapsed = 00:00:35 .
Memory (MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Technology Mapping
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Technology Mapping : Time (s): cpu = 00:00:32 ; elapsed = 00:00:35 . Memory
(MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Flattening Before IO Insertion
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Final Netlist Cleanup
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished IO Insertion : Time (s): cpu = 00:00:37 ; elapsed = 00:00:40 . Memory (MB):
peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Renaming Generated Instances
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Renaming Generated Instances : Time (s): cpu = 00:00:37 ; elapsed =
00:00:40 . Memory (MB): peak = 1021.457 ; gain = 0.000
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Start Rebuilding User Hierarchy
---------------------------------------------------------------------------------
---------------------------------------------------------------------------------
Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:37 ; elapsed = 00:00:40 .
```

```
Memory (MB): peak = 1021.457 ; gain = 0.000
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Start Renaming Generated Ports
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Finished Renaming Generated Ports : Time (s): cpu = 00:00:37 ; elapsed = 00:00:40 .
Memory (MB): peak = 1021.457 ; gain = 0.000
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Start Handling Custom Attributes
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Finished Handling Custom Attributes : Time (s): cpu = 00:00:37 ; elapsed = 00:00:40
. Memory (MB): peak = 1021.457 ; gain = 0.000
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Start Renaming Generated Nets
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Finished Renaming Generated Nets : Time (s): cpu = 00:00:37 ; elapsed = 00:00:40 .
Memory (MB): peak = 1021.457 ; gain = 0.000
-----------------------------------------------------------------------------
-----------------------------------------------------------------------------
Start Writing Synthesis Report
-----------------------------------------------------------------------------

Report BlackBoxes:
+-+--------------+----------+
| |BlackBox name |Instances |
+-+--------------+----------+
+-+--------------+----------+

Report Cell Usage:
+------+-------+------+
|      |Cell   |Count |
+------+-------+------+
|1     |BUFG   |     1|
|2     |CARRY4 |    14|
|3     |LUT1   |     3|
|4     |LUT2   |     4|
|5     |LUT3   |     6|
|6     |LUT4   |    20|
|7     |LUT5   |     4|
|8     |LUT6   |    13|
|9     |MUXF7  |     1|
```

```
|10    |FDRE   |    62|
|11    |FDSE   |     1|
|12    |IBUF   |    11|
|13    |OBUF   |    14|
+------+-------+------+
```

Finished Writing Synthesis Report : Time (s): cpu = 00:00:37 ; elapsed = 00:00:40 .
Memory (MB): peak = 1021.457 ; gain = 0.000

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.
Synthesis Optimization Runtime : Time (s): cpu = 00:00:26 ; elapsed = 00:00:38 .
Memory (MB): peak = 1021.457 ; gain = 0.000
Synthesis Optimization Complete : Time (s): cpu = 00:00:38 ; elapsed = 00:00:41 .
Memory (MB): peak = 1021.457 ; gain = 0.000
INFO: [Project 1-571] Translating synthesized netlist
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory
(MB): peak = 1021.457 ; gain = 0.000
INFO: [Netlist 29-17] Analyzing 15 Unisim elements for replacement
INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
INFO: [Project 1-570] Preparing netlist for logic optimization
INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory
(MB): peak = 1021.457 ; gain = 0.000
INFO: [Project 1-111] Unisim Transformation Summary:
No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis
34 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
synth_design completed successfully
synth_design: Time (s): cpu = 00:00:46 ; elapsed = 00:01:06 . Memory (MB): peak =
1021.457 ; gain = 0.000
INFO: [Common 17-1381] The checkpoint 'C:/Users/noahh/Documents/Vivado/Ecen
220/Labs/Lab 9/tx/tx.runs/synth_1/tx_top.dcp' has been generated.
INFO: [runtcl-4] Executing : report_utilization -file tx_top_utilization_synth.rpt
-pb tx_top_utilization_synth.pb
INFO: [Common 17-206] Exiting Vivado at Wed Nov 11 18:01:19 2020...