```
`timescale 1ns / 1ps
/**********************************************************************
*
* Module: seven_segment
*
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* Class: ECEN 220, Section 3, Fall 2020 - ECEN 220, Section 1, Winter 2020
* Date: 14 Oct 2020
*
* Description: Uses two nor games to determine the outputs of q and qbar.
The gates are crossed and wired together
*
*
**********************************************************************/
`default_nettype none

module Figure15_17(input wire logic d,
             input wire logic clk,
             output wire logic q,     // This output must have the 'wire' specifier
             output wire logic qbar   // This output must have the 'wire' specifier
          );
          logic notD, notCLK, notDAndnotCLK, dAndnotCLK, notNotCLK;
          logic norTop, norBot, norTopAndNNCLK, norBotAndNNCLK;
         assign #1ns notD = ~d;
         assign #1ns notCLK = ~clk;
         assign #3ns notDAndnotCLK = notD & notCLK;
         assign #3ns dAndnotCLK = d & notCLK;
         assign #1ns notNotCLK = ~notCLK;
         assign #2ns norTop = ~(dAndnotCLK | norBot);
         assign #2ns norBot = ~(notDAndnotCLK | norTop);
         assign #3ns norTopAndNNCLK = norTop & notNotCLK;
         assign #3ns norBotAndNNCLK = norBot & notNotCLK;
         assign #2ns q = ~(norTopAndNNCLK | qbar);
         assign #2ns qbar = ~(norBotAndNNCLK | q);
endmodule
```