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timescale 1ns / 1ps
/*****
*
* Module: seven_segment
*
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*
* Description: Uses two nor gates to determine the outputs of q and qbar.
The gates are crossed and wired together
*
*
*****/
`default_nettype none

module latch(input wire logic r,
             input wire logic s,
             output wire logic q,      // This output must have the 'wire' specifier
             output wire logic qbar    // This output must have the 'wire' specifier
             );

    // nor(q, r, qbar);
    // nor(qbar, s, q);
    assign #3ns q = ~(r | qbar);
    assign #3ns qbar = (s | q);

endmodule

```