```verilog
`timescale 1ns / 1ps
/***********************************************************************
*
* Module: stopwatch_top
*
* Author: Noah Hanks
* Class: ECEN 220, Section 3, Fall 2020 - ECEN 220, Section 1, Winter 2020
* Date: 28 Oct 2020
*
* Description: Sets switches, buttons and the display to the data in stopwatch
module usable on the fpga board.
*
*
***********************************************************************/
`default_nettype none

module stopwatch_top(
input wire logic sw, clk, btnc,
output logic[7:0] segment,
output logic[3:0] anode
    );

   logic[3:0] digit0, digit1, digit2, digit3;
   Stopwatch SW0(.clk(clk), .reset(btnc), .run(sw), .digit0(digit0),
.digit1(digit1), .digit2(digit2), .digit3(digit3));
   SevenSegmentControl SSC0 (.segment(segment), .anode(anode), .reset(btnc),
.clk(clk), .dataIn({digit3, digit2, digit1, digit0}), .digitPoint(4'b0100),
.digitDisplay(4'b1111));

endmodule
```