EEE381 Tech Memo

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Subject: Lab #02

1 Abstract

The purpose of this lab exercise was to observe the DC and small AC signal charactaristics of MOSFET devices. This includes extracting various parameters that determine specific characteristics of MOSFETs. Theses parameters were extracted from both NMOS and PMOS devices.

2 Theory

DC behavior of MOSFETs can be modeled like a simple transconductance amplifier, where the current through the device is a function of the properties of the transistor, the voltage across the gate and source, and the voltage across the drain and source. This relationship changes based on what operating mode the transistor is in, either linear or saturation. Both of these relationships can be seen in Equations 1 and 2.

$$I_d = k_n\prime \frac{W}{L}[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2](1 + \lambda V_{DS}), \qquad V_{DS} \geq V_{GS} - V_t \quad (Linear) \tag{1}$$

$$I_d = k_n\prime \frac{W}{L}(V_{GS} - V_t)^2(1 + \lambda V_{DS}), \qquad V_{DS} < V_{GS} - V_t \quad (Saturation) \tag{2}$$

Where $k_n\prime = \mu_n C_{ox}$, μ_n is the electron mobility, C_{ox} is oxide capacitance per unit area, W is channel width, L is channel length, λ is the channel length modulation parameter, and V_t is the threshold voltage. V_t can be calculated when there is a voltage between the source and body with Equation 3.

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right] \tag{3}$$

Where V_{t0} is the threshold voltage when $V_{SB} = 0$, ϕ_f is a physical parameter of the device and γ is the body-effect parameter, which can be expressed as seen in Equation 4.

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_{sub}}}{C_{ox}} \tag{4}$$

The body-effect parameter γ can be found by ploting $\sqrt{I_D}$ vs. V_{GS} and finding the slope, which is γ. Using this same graph, the threshold voltages can be found by looking at the x-intercept for each of the different V_{SB} values.

These equations apply both to NMOS and PMOS but when calculating values for PMOS, the absolute value of the voltages need to be used, due to the opposite polarity of the device.

The channel length modulation effect causes an increase in current by a factor of $1 + \lambda V_{DS}$ due to the shortening of the channel length. For small signal AC modeling, this can effectvly be modeled by a resistance between the drain and source, r_0. The value can be found using Equation 5.

$$r_0 = \frac{1}{|\lambda| I_D} = \frac{|V_A|}{I_D} \tag{5}$$

Where V_A is the early voltage, which can be found by extrapolating the line created by the I_d vs. V_{DS} curve when the MOSFET is in saturation, to the x-intercept and taking the absolute value.

3 Results and Discussion

For the first part of the experiment, five different V_{DS} values were applied and I_D was measured for three V_{SB} values, with $V_{GS} = V_{DS}$for a total of 24 data points. This data was then used to create the $sqrt I_D$ vs. V_{DS} graphs (Figures 1 and 2 and Tables 1 and 2).

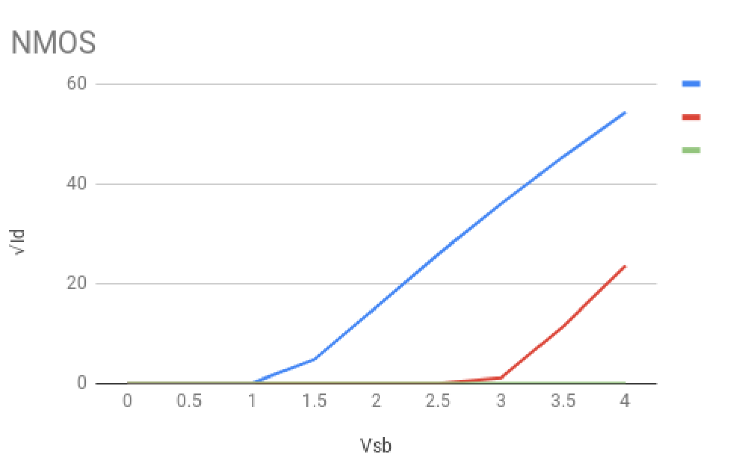

Figure 1: NMOS $\sqrt{I_D}$ vs. V_{DS}

Table 1: NMOS I_D vs. V_{DS} data

$\mathbf{V_{DS}}$ (V)	$\mathbf{I_D}$ (µA)		
V_{SB}	0V	2V	5V
0	0	0	0
0.5	0	0	0
1	0	0	0
1.5	22.2	0	0
2	234.1	0	0
2.5	673.2	0	0
3	1294.4	1.2	0
3.5	2062.8	131.3	0
4	2950.5	555.9	0

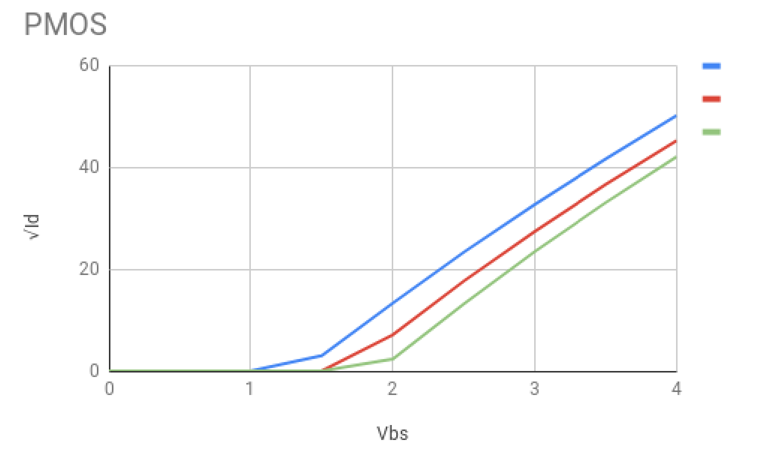

Figure 2: PMOS $\sqrt{I_D}$ vs. V_{DS}

Table 2: PMOS I_D vs. V_{SD} data

$\mathbf{V_{SD}}$ (V)	$\mathbf{I_D}$ (µA)		
V_{BS}	0V	2V	5V
0	0	0	0
0.5	0	0	0
1	0	0	0
1.5	9.1	0	0
2	177.9	50.6	5.5
2.5	546.8	313.4	174.7
3	1076	756	553.6
3.5	1741.4	1346	1097.2
4	2525	2053	1780.1

It's important to note, during the experiment, none of the given values of V_{SD} for $V_{SB} = 5$V were enough to cause the NMOS transitor to turn on. In order to get some meaningful data out of that dataset, the minimum voltage that was required to turn on the MOSFET was recorded as 4.8 V.

A linear regression was used to find a line of best fit for the extraction of the transconductance parameter (k) and the threshold voltage (V_t). The experimental values for V_t that were found can be seen in Table 3 and the experimental value for k can be seen in Table 4.

Table 3: MOSFET V_t parameter extraction

$\|\mathbf{V_{SB}}\|$ (V)	$\mathbf{V_t}$ (V)	
	NMOS	PMOS
0	1.23	1.30
2	2.96	1.59
5	4.8	1.85

Table 4: MOSFET k parameter extraction

MOSFET	**k**	μ
NMOS	21.1959	2.1196×10^7
PMOS	19.2986	1.9297×10^7

A graph of V_t vs. $\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}$ was created in order to extract the body-effect parameter (γ) for both the NMOS and PMOS transistors. This graph and the value for γ can be seen in Figure 3 and Table 5.

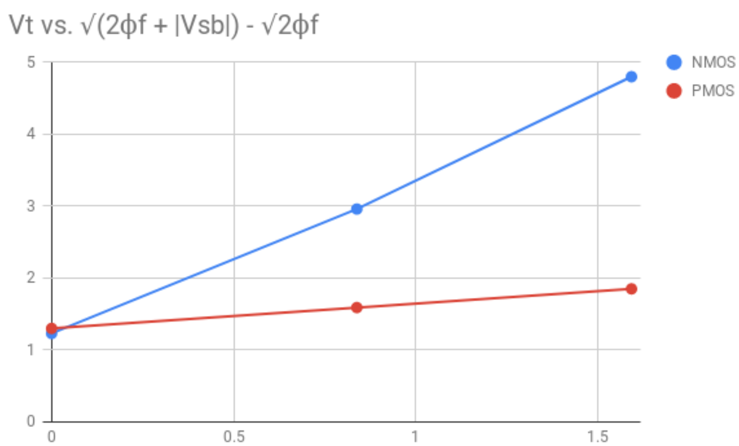

Figure 3: V_t vs. $\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}$

Table 5: Body-effect Parameter (γ)

MOSFET Type	γ
NMOS	2.24
PMOS	0.346

The next step in the experiment was to find the substrate doping parameter N_{sub} using two different methods. The first uses Equation 4 and the second uses Equation 6.

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (\frac{N_{sub}}{N_{ref}})} \tag{6}$$

Rearranging Equation 4 for N_{sub}, a simple equation is derrived (7).

$$N_{sub} = \frac{(\gamma C_{ox})^2}{2q\varepsilon_s} \tag{7}$$

Using the extracted value of γ and the assumed values for C_{ox} , q, and ε_s, the value for γ can be calculated. This value can be found in Table 6.

Rearranging Equation 6 for N_{sub}, a slightly more complex equation is derrived (8).

$$N_{sub} = N_{ref}\left(\frac{\mu_{max} - \mu_{min}}{\mu - \mu_{min}} - 1\right) \tag{8}$$

Using the given values for μ_{max}, μ_{min}, N_{ref} and the experimental values for μ, the N_{sub} parameter can be calculated. This value can also be found in Table 6.

Table 6: Calculated N_{sub} values

MOSFET Type	$\mathbf{N_{sub}}$ (Method 1)	$\mathbf{N_{sub}}$ (Method 2)
NMOS	134.017	9.2×10^{13}
PMOS	3.19754	2.23×10^{14}

These two methods for finding N_{sub} produced vastly different values. this is partly due to the fact that one method assumes uniform substrate doping, which is not the reality. Also, the large difference between the values could be due to calculation errors. This seems like the most likley reason due the the extremly large difference between the values.

The last part of the exercise was to extract the channel length modulation parameter ($\lambda_p and \lambda_n$). This was done by plotting I_D vs. $|V_{DS}|$ and using a linear regression to fit the curve created when the device is in saturation. The x-intercept of this line is the early voltage (V_A). The λ is then the inverse of the early voltage. Figure 4 and 5 shows the graph of I_D vs. $|V_{DS}|$ for both the NMOS and PMOS devices.

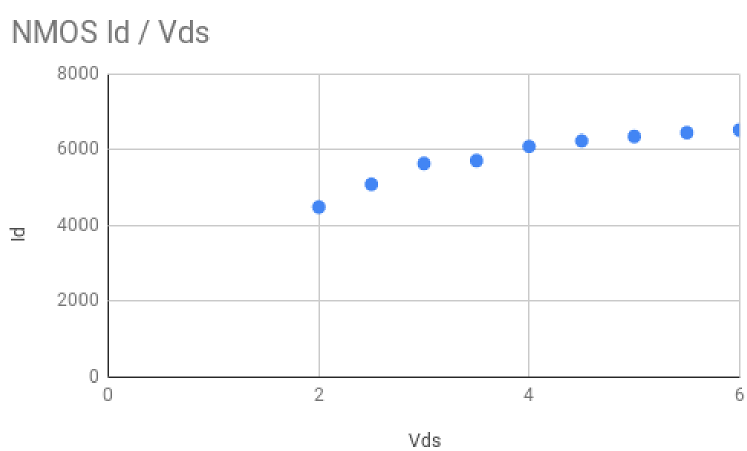

Figure 4: NMOS I_D vs. $|V_{DS}|$

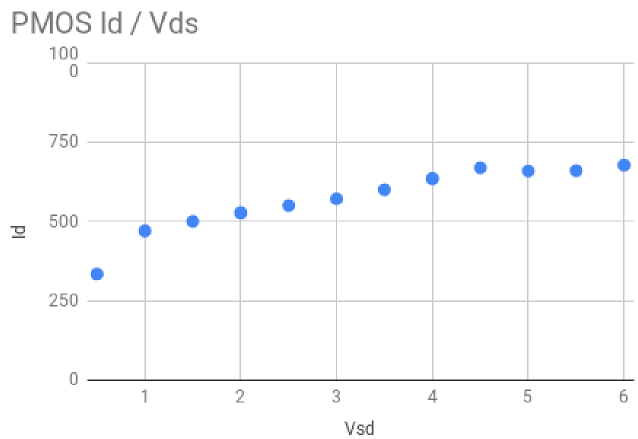

Figure 5: PMOS I_D vs. $|V_{DS}|$

The $|V_A|$ values that were found using the trendline when the device was in saturation can be found in Table 7.

Table 7: Extracted $|V_A|$ and λ

MOSFET Type	$\mathbf{|V_A|}$	λ
NMOS	56.6	0.01767
PMOS	19.7	0.05076

These values were relativley close for the values of V_A found on the datasheet for the NMOS and PMOS transistors.

4 Conclusion

The goal of this lab was to understand the different parameters in DC and AC biasing of MOSFET transistors. Parameters such as k, V_t, μ, γ, and λ were extracted using graphs and relationships between I_D and V_{DS}. Most of the experimentally found values agreed with the theorized values, except for the second method for finding N_{sub}.