EEE381 Tech Memo

From: Charles Noah Lutz
Partner: N/A
To: Colin Bussert
Date: Performed: 11/29/18; Due: 12/09/18
Subject: Lab #05-06

1 Abstract

The goal of lab exercises 5 and 6 was to build a functioning operational amplifier and observe several different characteristics of the op-amp. These characteristics included gain of each individual stage, the overall gain and the frequency response of the overall op-amp. The circuit was first designed using hand calculations, then tested in a PSPICE simulator to verify the operation. Then the op-amp was built in-lab and tested experimentally.

2 Theory

An ideal op-amp has an input resistance of infinity, an output resistance of zero and a gain of infinity. While this is not practically possible, the closer an op-amp can be built to the ideal case, the better the op-amp will perform in any given circuit. The two amplifiers that were used in this lab exercise was the NMOS differential amplifier (effectivly two common source amplifiers) with a PMOS current mirror load and a PMOS common source amplifier. Figure 1 shows the schematic for the op-amp.

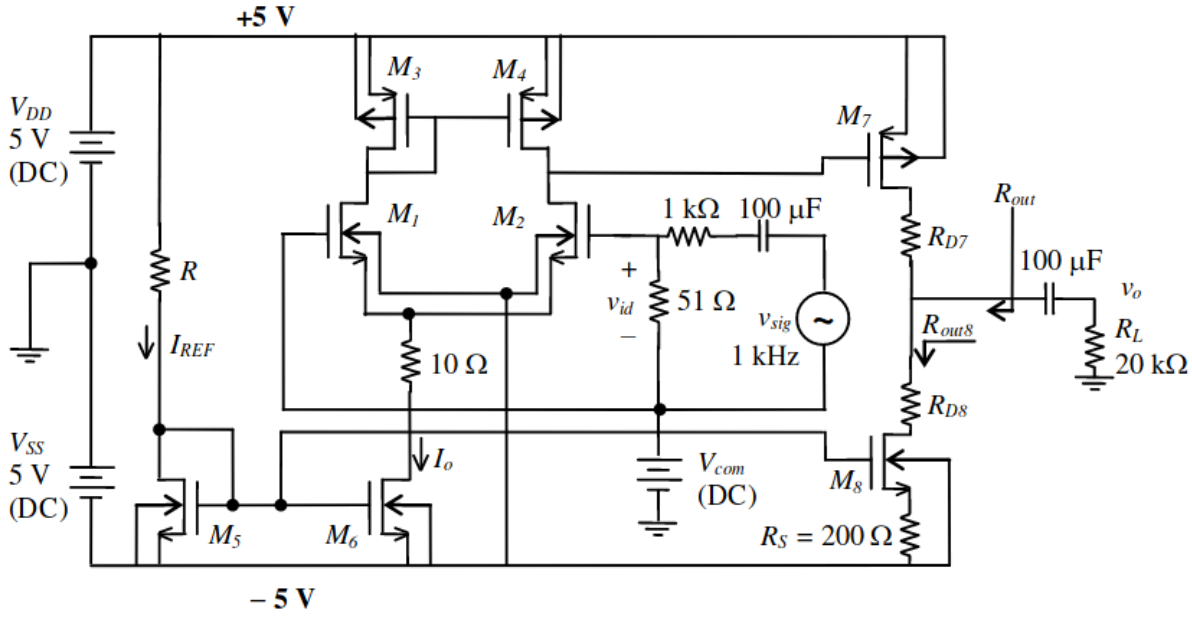


Figure 1: Operational amplifier used for this lab exercise

The first value that was calculated was the reference current that was required to ensure that the op-amp had a gain of $> 240 \frac{V}{V}$. Using the differential amplifier that was built in lab exercise

4 as a starting point, which had a reference current of 4mA, the only thing that needed to be calculated was the effective gain when the two stages are cascaded.

$$A_v = A_1 * A_2 = -33.665 * -25.668 = 864.1132 \frac{\text{V}}{\text{V}} \tag{1}$$

As the calculated gain is much more than $240 \frac{\text{V}}{\text{V}}$ it was decided to go with 4mA as the reference current.

The next values that needed to be calculated were the $R_{7/8}$ values to center the output around 0V DC. It was found that to center the output R_8 to 2.15kΩ. Since this value needed to be a standard resistor value, a resistor of 2.2kΩ was used.

Next, the circuit was built and simulated in PSPICE. Figure 2 shows the circuit in PSPICE.

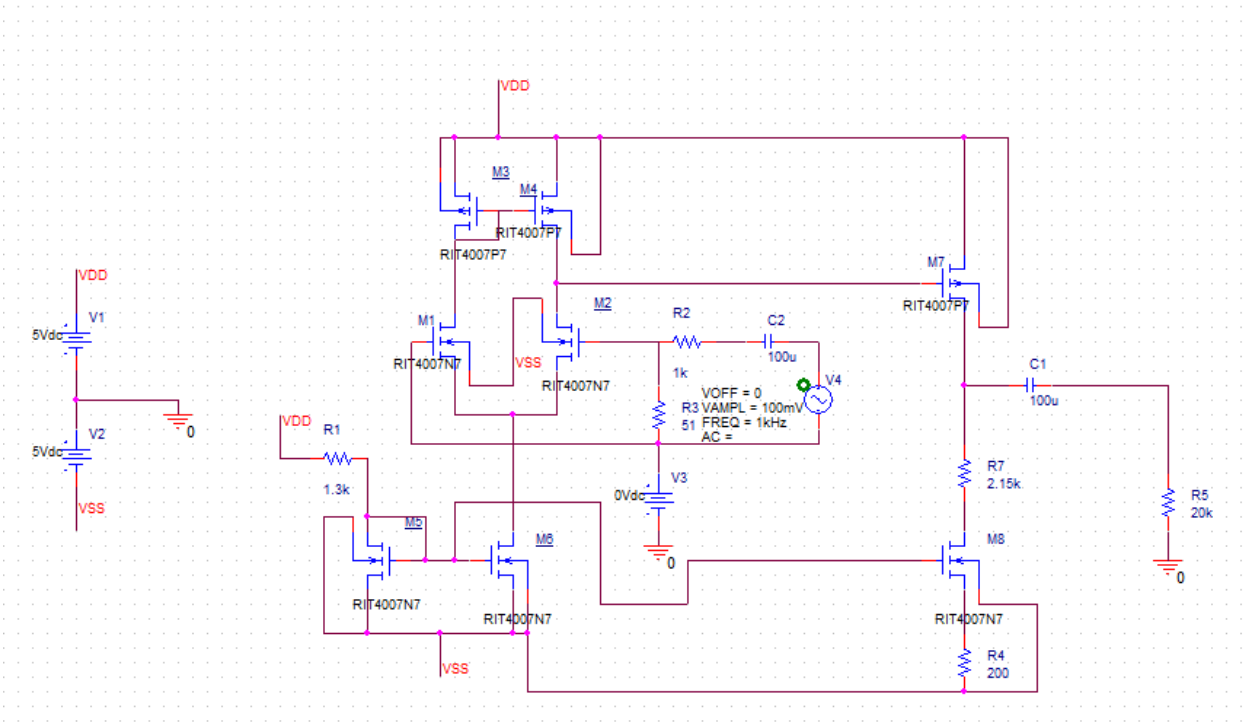
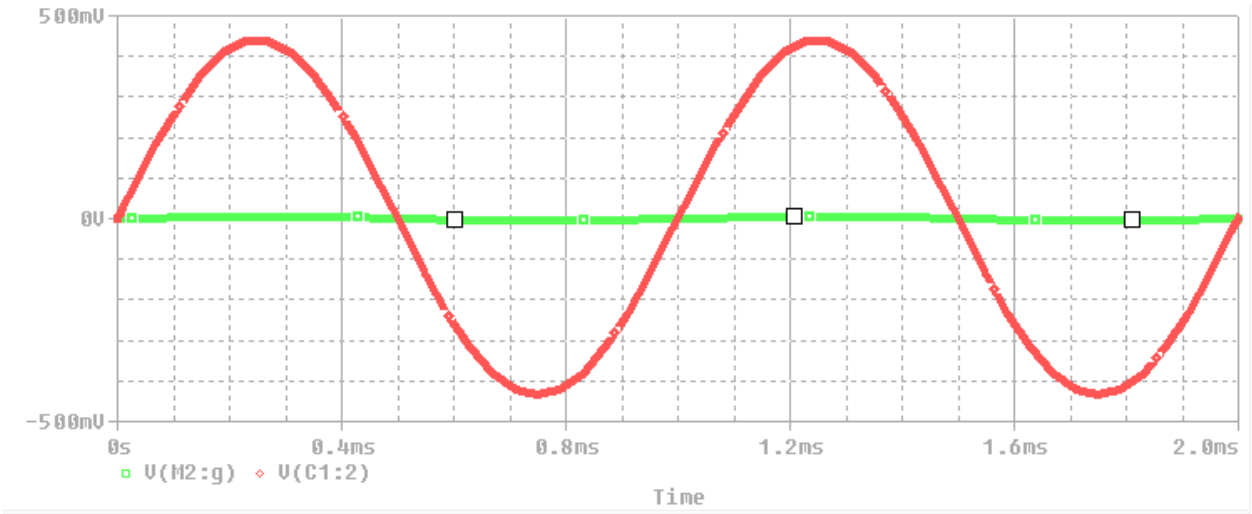


Figure 2: Operational amplifier in PSPICE simulator

The first simulation that was run was a simple transient simulation to find the overall gain of the amplifier. Figure 3 shows the input signal and the output signal.



Measurement Results

Evaluate	Measurement	Value
☑	MAX(V(M2:g)) - MIN(V(M2:g))	9.66881m
☑	MAX(V(C1:2)) - MIN(V(C1:2))	872.41528m

Figure 3: PSPICE simulated voltage gain of operational amplifier

$$A_v = \frac{V_{out}}{V_{in}} = \frac{872.415\text{mV}}{9.669\text{mV}} = 90.228\frac{\text{V}}{\text{V}} \tag{2}$$

The next simulation that was run was a frequency response. The frequency of the input was varied from 1Hz to 100MHz and gain measured and graphed against the frequency. Figure 4 shows the gain (in dB) versus the frequency of the input signal.

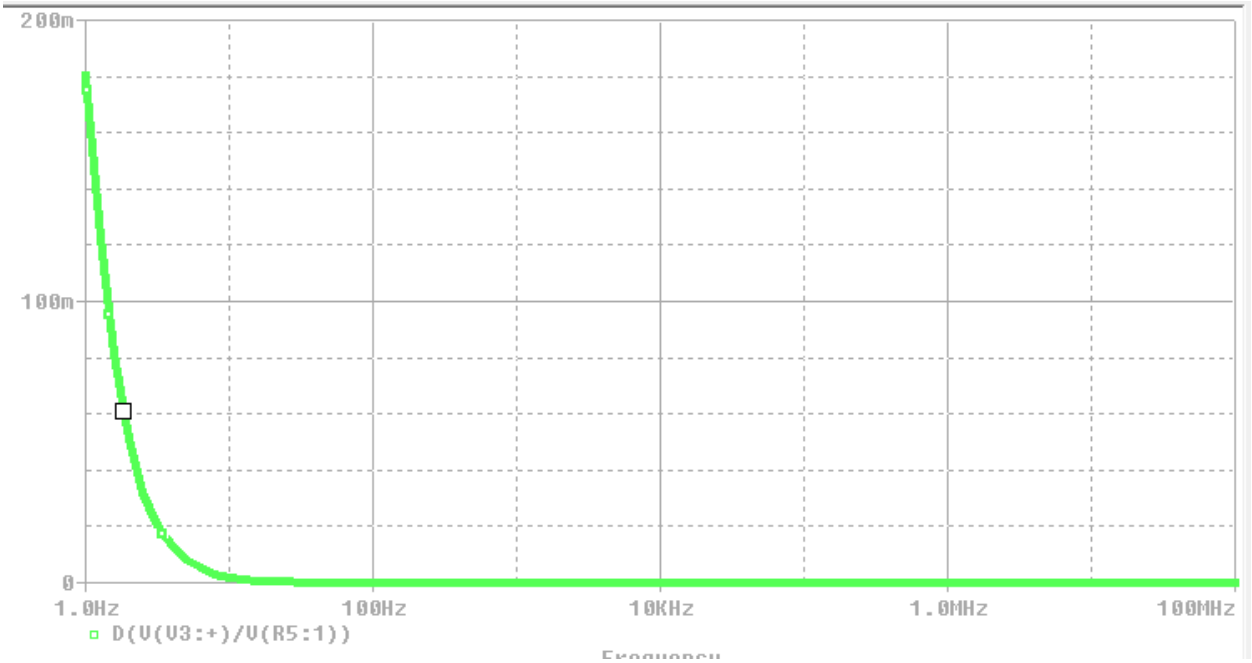


Figure 4: Simulated frequency response of op-amp

It should be noted that this frequency response graph is incorrect and could be due to the simulation profile being set up incorrectly or the transistor values being incorrect.

3 Results and Discussion

Next, the circuit in Figure 1 was built in-lab using CD4007 packages and a breadboard. The differential pair that was built in lab excercise 4 was used as a starting point and modified slightly to add the second common source amplifier.

First the overall gain of the circuit was measured. This was done using a waveform generator running at 1kHz and an oscilloscope to measure the output. Figure 5 shows the experimental gain where channel 1 shows input and channel 2 shows output.

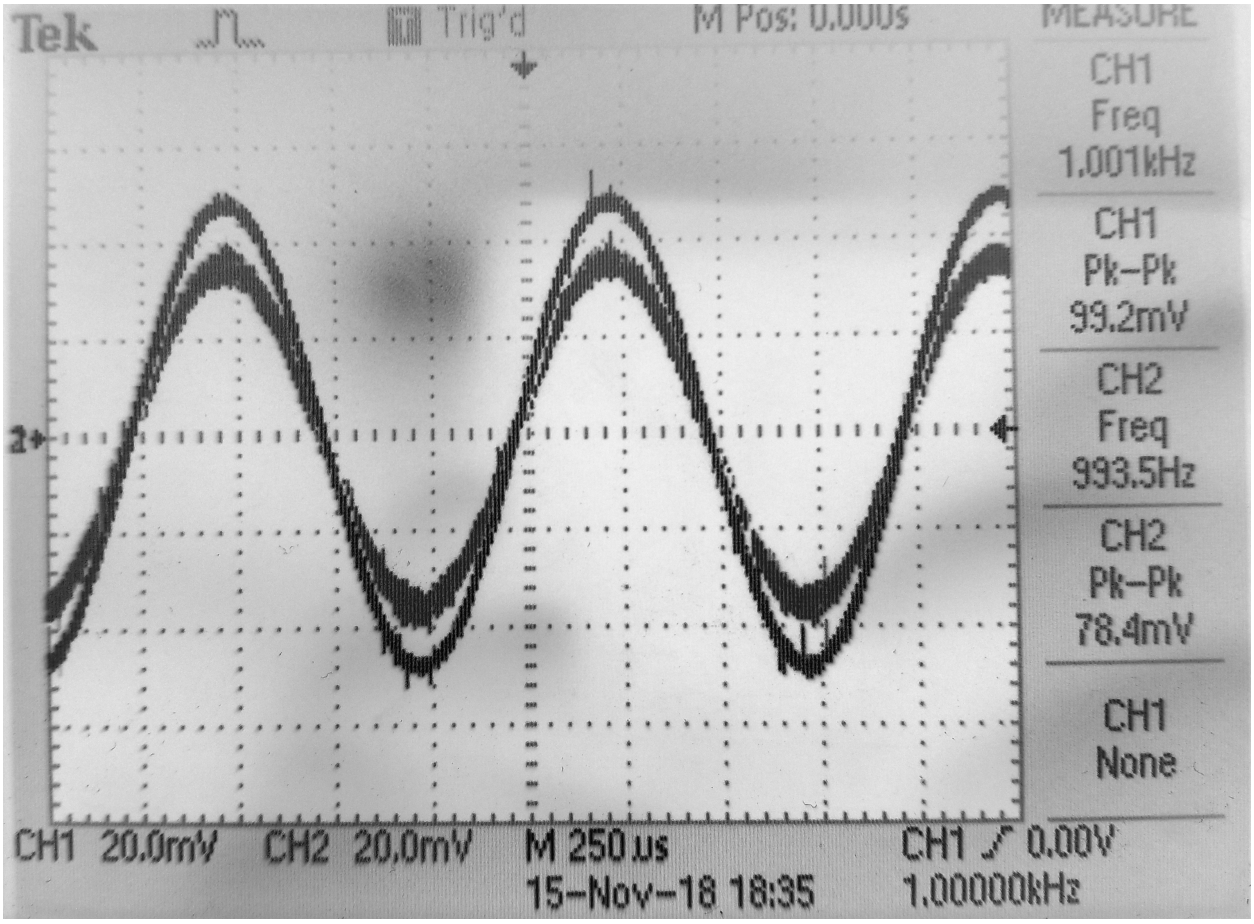


Figure 5: Experimental gain

It should be noted that we could not get our second stage (common source amplifier) working. Instead we used the first stage as our output. This results in a much lower gain, as it is only going through one amplifier.

Table 1: Experimental gain measurements

Voltage	Value
V_{sig}	99.2 mV
V_{id}	4.813 mV
V_o	78.4 mV

$$A_v = \frac{V_{out}}{V_{id}} = \frac{78.4\text{mV}}{4.813\text{mV}} = 16.29\frac{\text{V}}{\text{V}} \tag{3}$$

Next, the frequency response of the circuit was tested. Again, a waveform generator running at various frequencies was used for input and an oscilloscope was used to measure the input and output which was used to calculate the gain in dB. Table 2 shows the raw data and Figure 6 shows the logarithmic graph for frequency response.

Table 2: Experimental frequency response data

Frequency	Gain (dB)
100 Hz	25.105
1 kHz	25.105
10 kHz	25.015
100 kHz	20
1 MHz	7.61
10 MHz	2.11

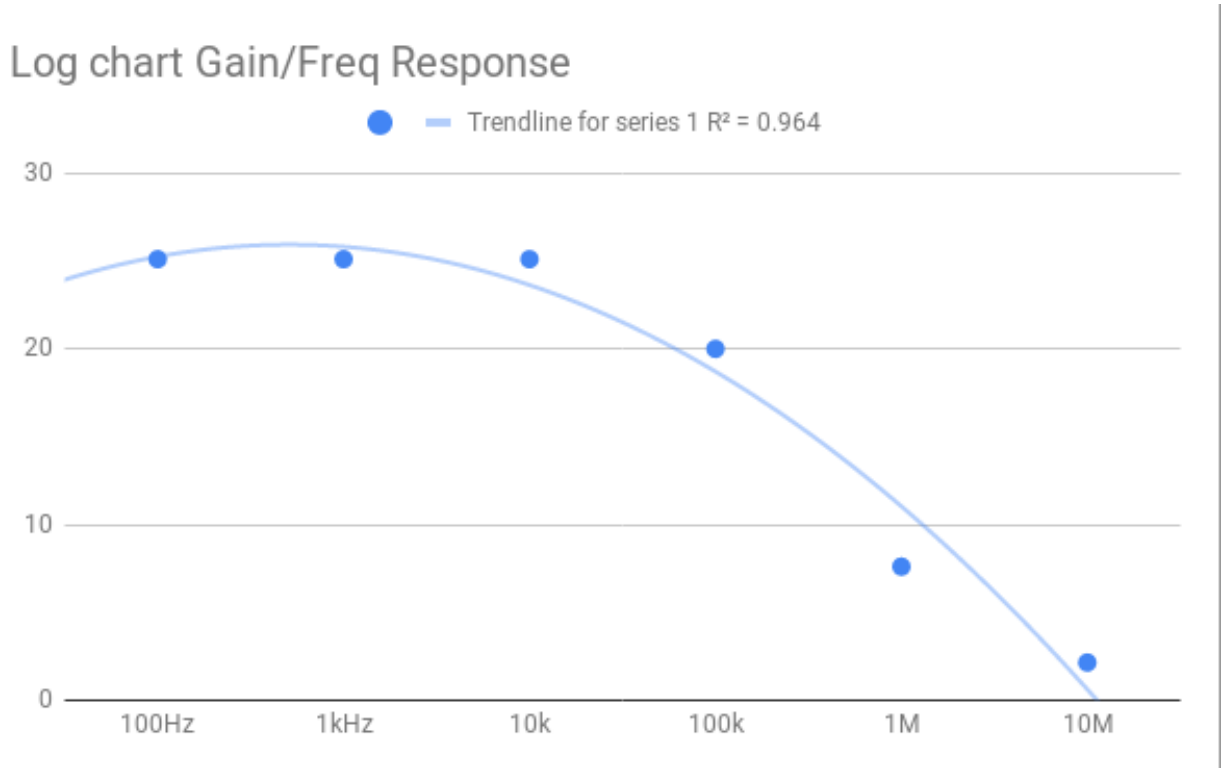


Figure 6: Experimental frequency response Bode plot

As the frequency gets above 10 kHz, the gain starts to drop off. This is not consistent with the frequency response graph that was obtained during PSPICE simulation. This could be due to the simulation profile being set up incorrectly, returning incorrect values. This theory is supported by the fact that the simulated frequency response graph was not the correct general shape.

4 Conclusion

The goal of lab exercise 5 and 6 was to build a functioning operational amplifier using a differential amplifier and a common source amplifier. The specific attributes of the amplifier that were being investigated were the overall gain of the amplifier and the frequency response.
During the in-lab portion of the exercise we were unable to get the second stage, common source amplifier to sucessfully work, due to this, we instead used the first stage, differential amplifier as our output. While this reduced our overall gain, it still allowed us to run a frequency analysis on the amplifier.
There was also an error during simulation that caused the simulated frequency response to be incorrect. This could have been due to the transistors being set up wrong or the simulation profile being incorrect.