A Decade of Nanoelectronics – Journey from classical bulk CMOS to metal-gate FinFETs

Prof. Jakub Kedzierski

Indian Institute of Technology Bombay

March 3, 2012

My Background

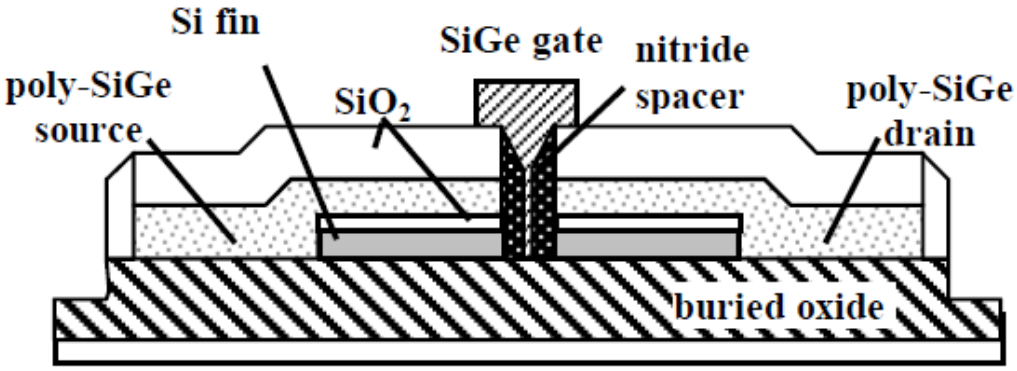
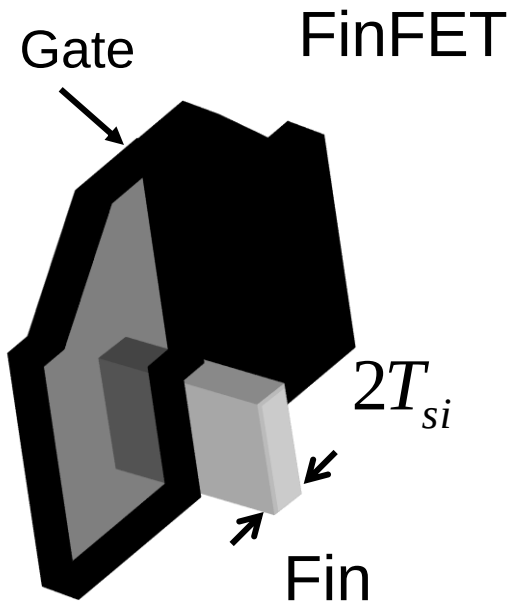


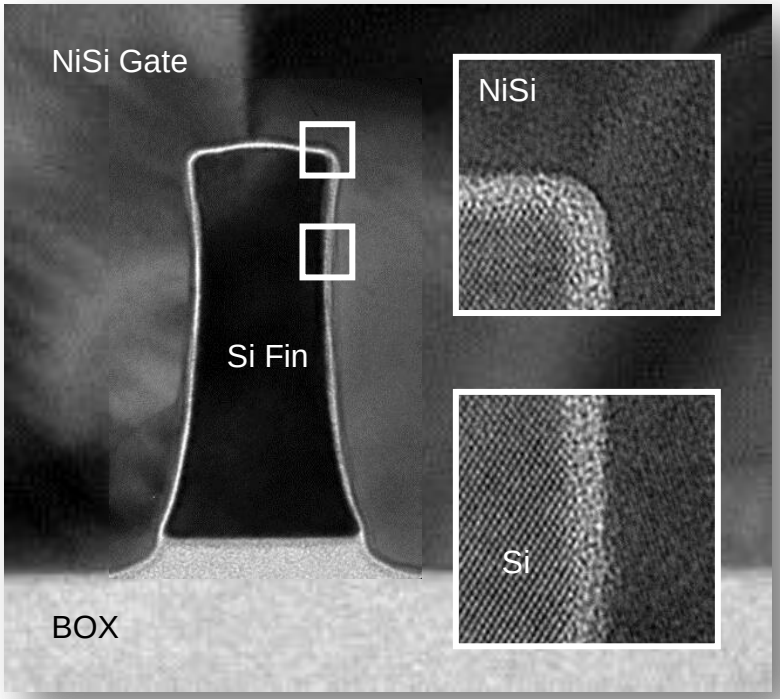
Figure 1: Schematic drawing of FinFET



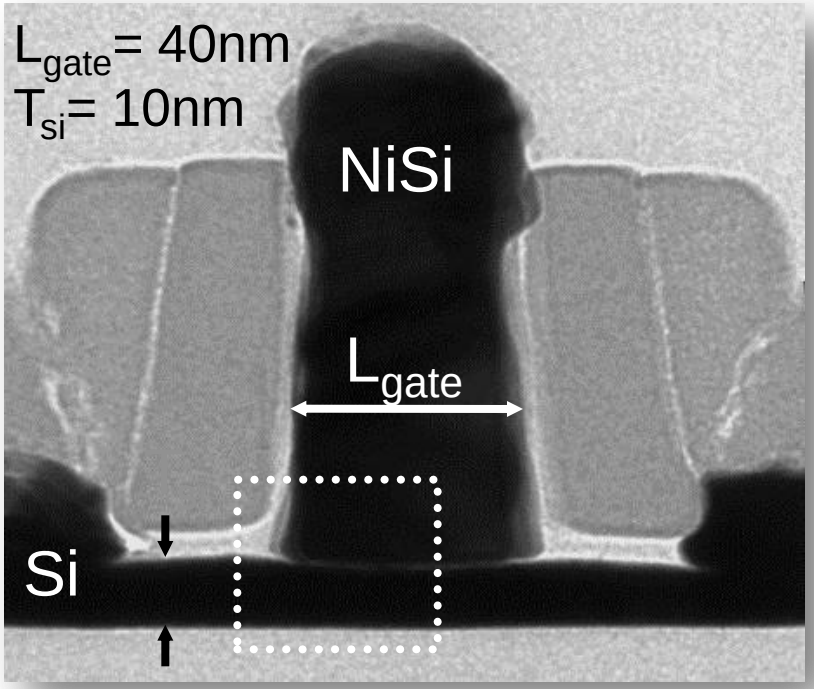
The first FinFET structure from UC Berkeley (IEDM 1999)

- **Born in Poland, if you don't understand my accent: STOP ME**
- **Co-invented the FinFET device while at UC Berkeley**

My Background



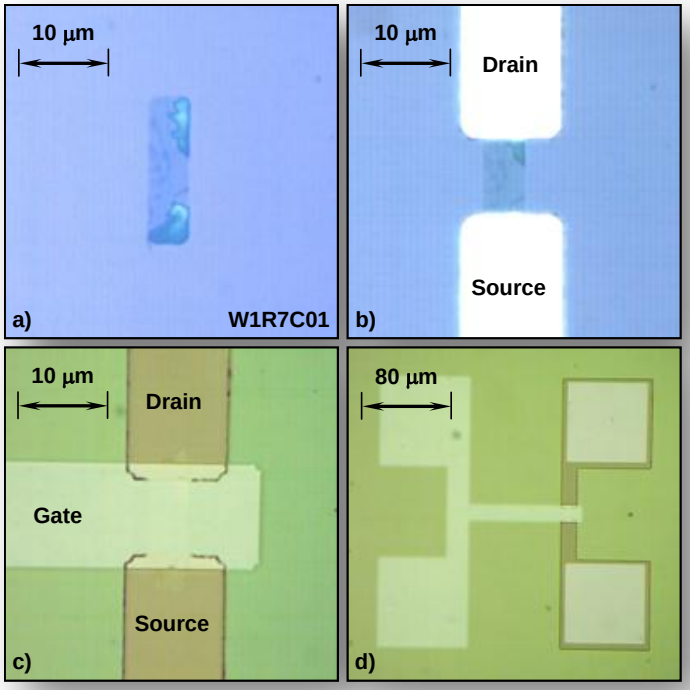
FinFET

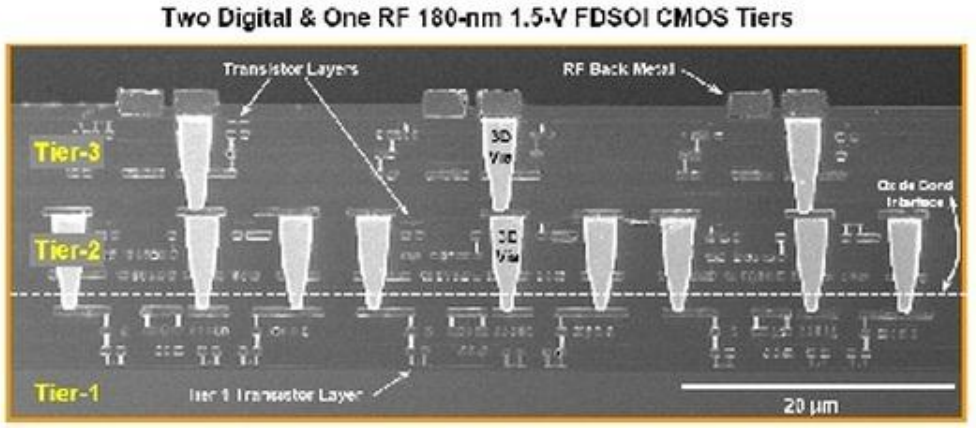


FDSOI

- **Graduated from UC Berkeley (2001)**
- **Worked at IBM's Watson Research Center on advanced CMOS devices (2001-2005)**

My Background



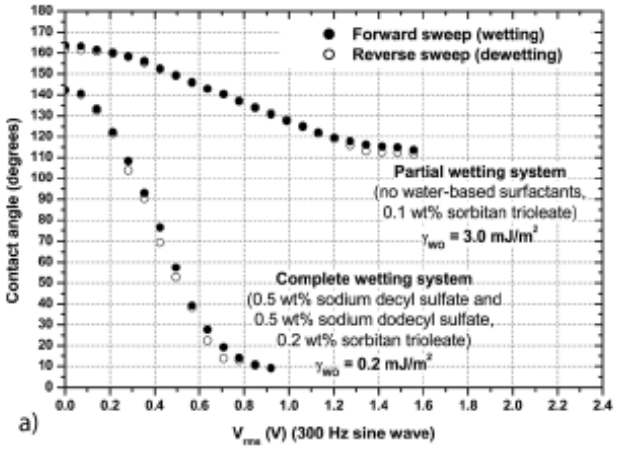


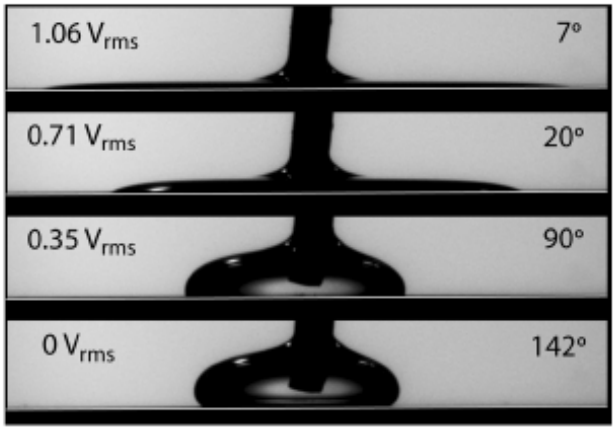
3D electronics

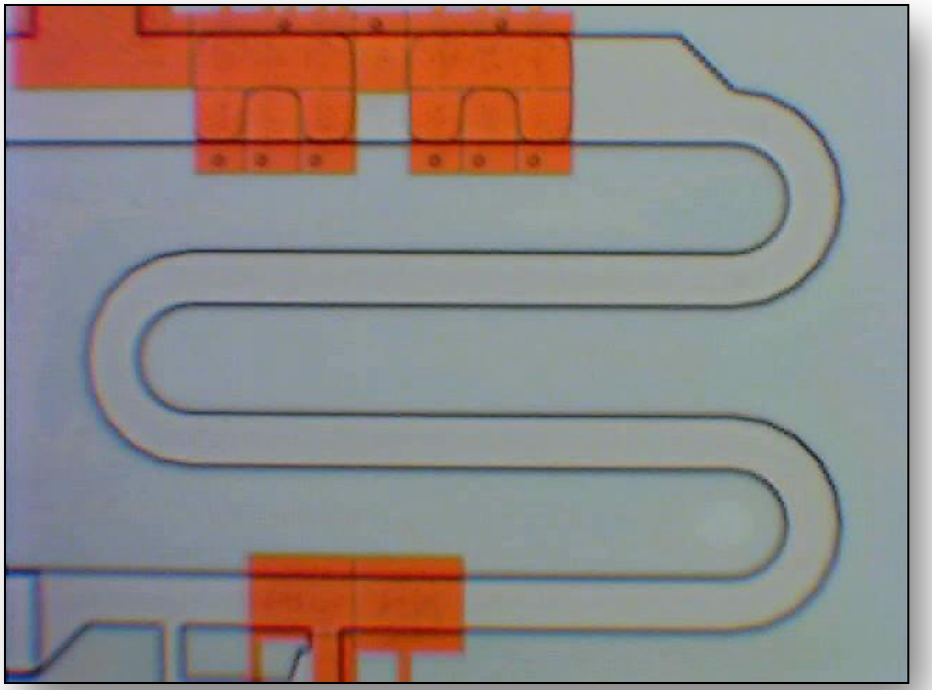
Graphene

- **Joined MIT Lincoln Laboratory (2005)**
  - **My group works in 3D electronics, graphene, low power electronics, and microfluidics**

My Background







Microfluidics

- **Currently on leave from MIT, working as a visiting professor at the Indian Institute of Technology Bombay**

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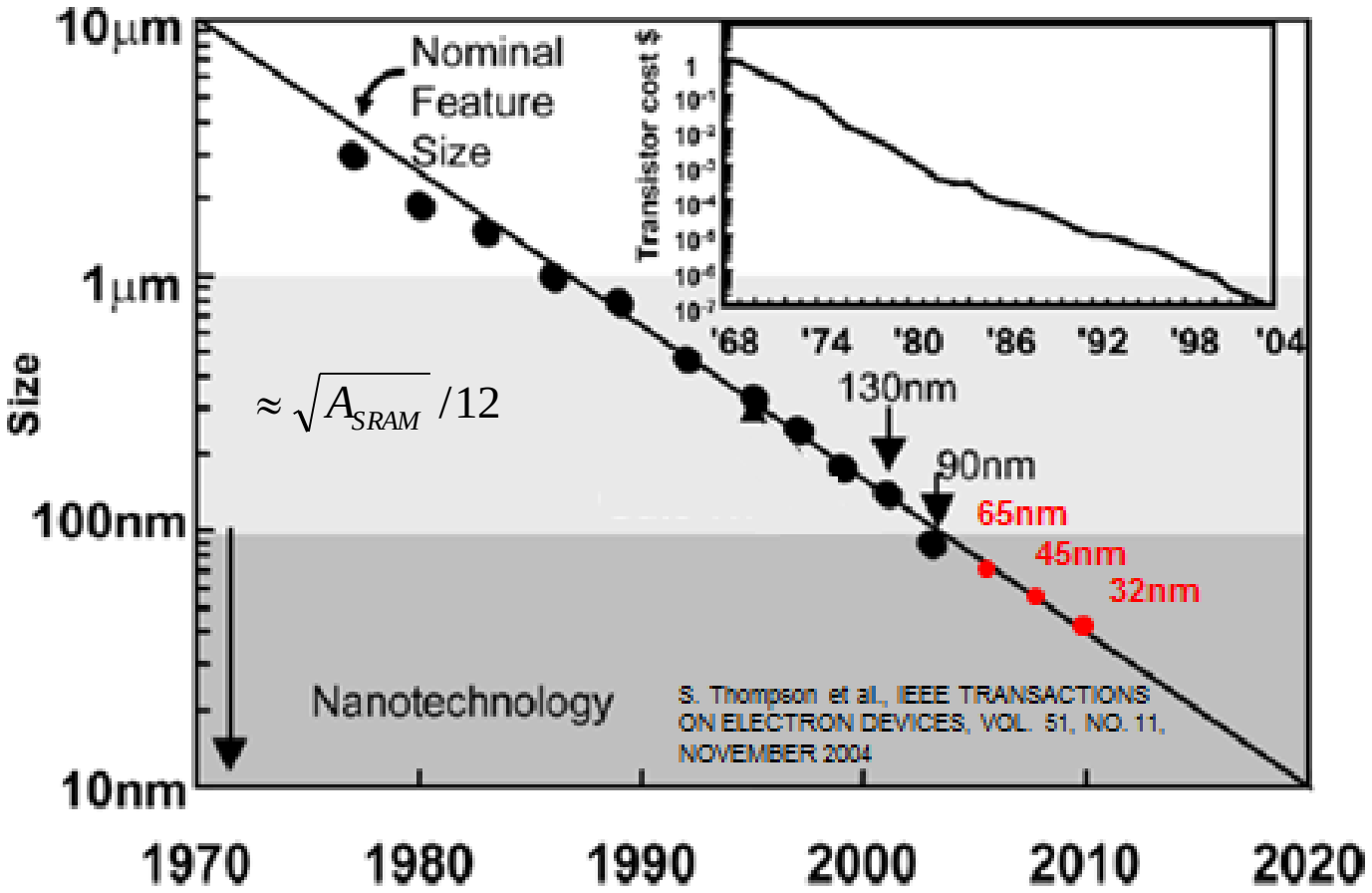
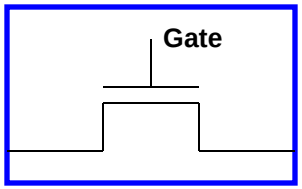
Silicon Past

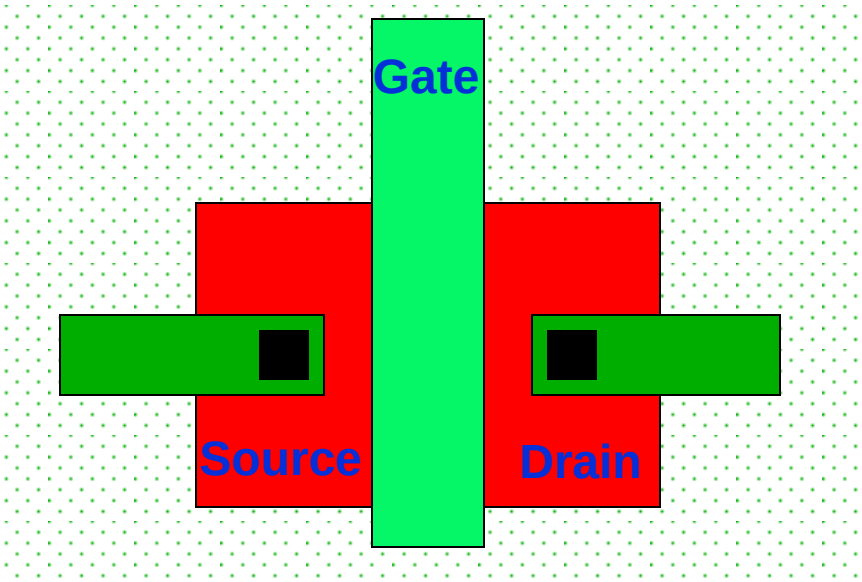


- **CMOS technology progress over last 30 years**
  - **This talk will cover scaling in the nanoelectronics era (last decade), but scaling has of course been going on since the late 60's**

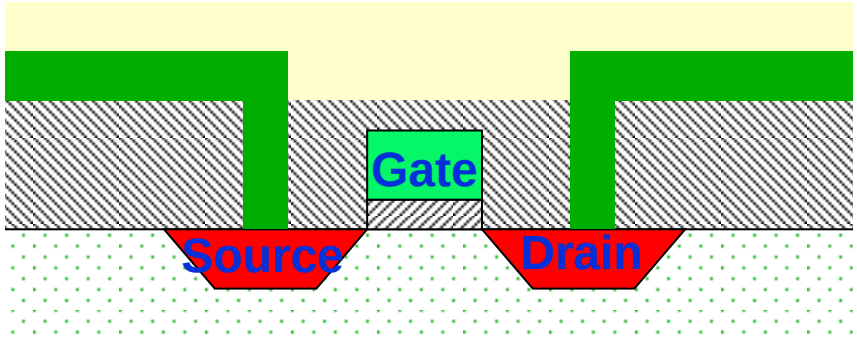
Anatomy of a Transistor

Top View

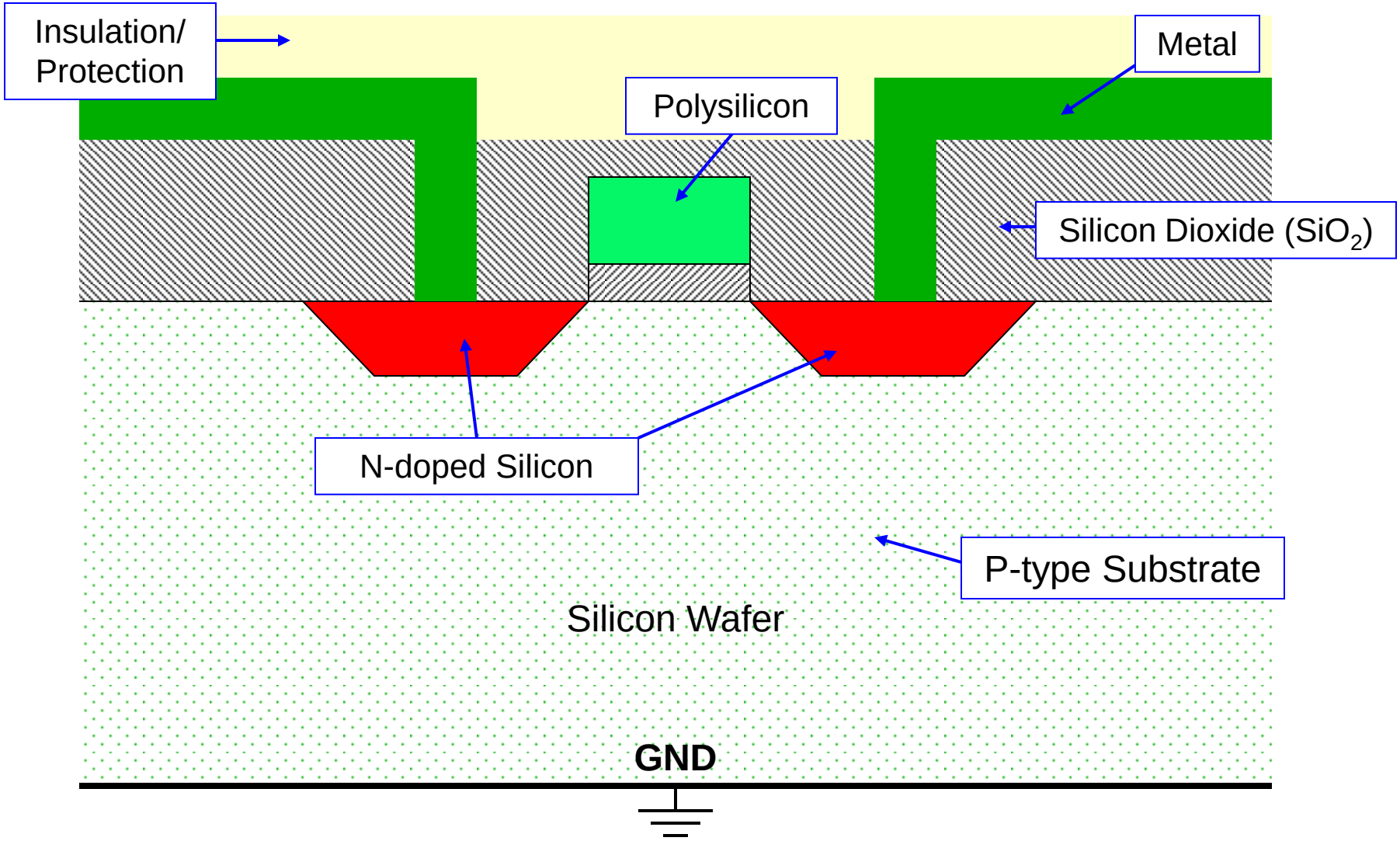




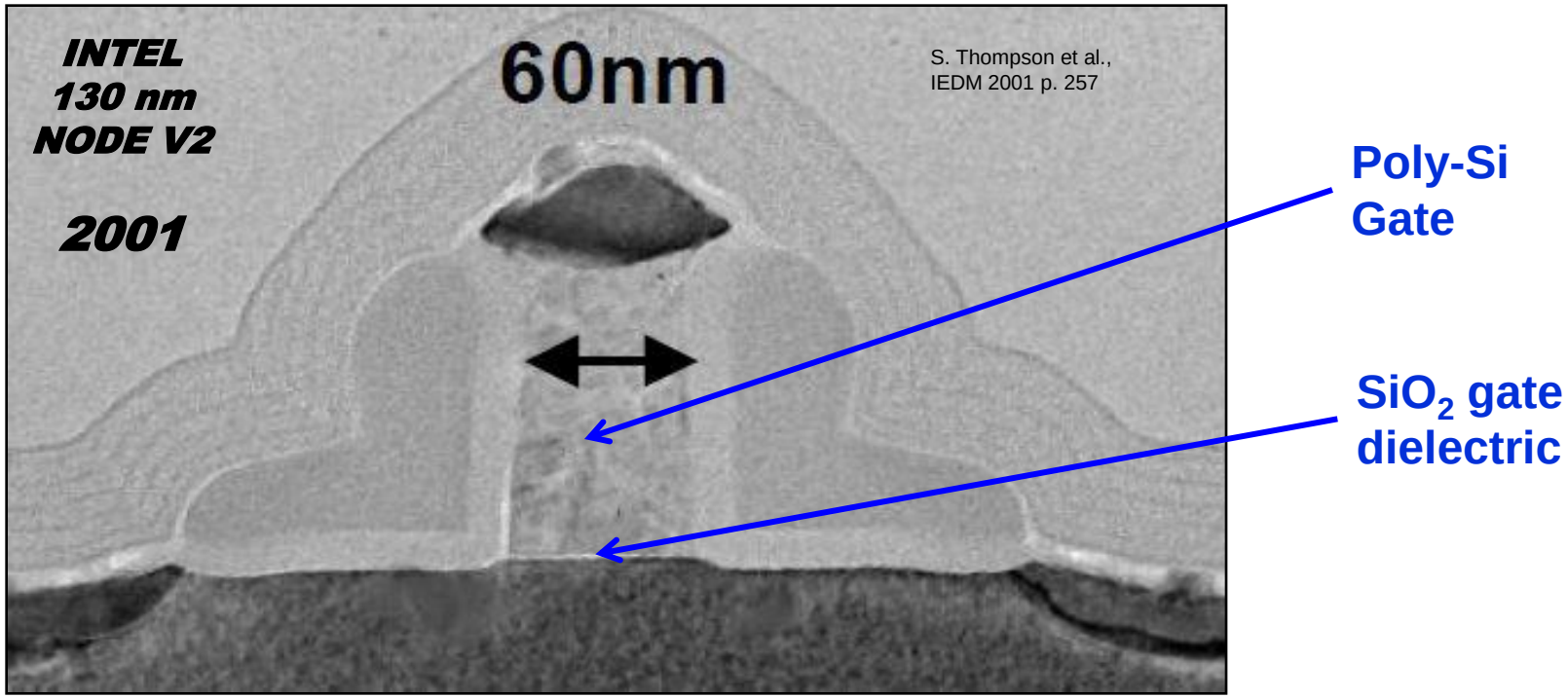
Side View



Anatomy of a Transistor

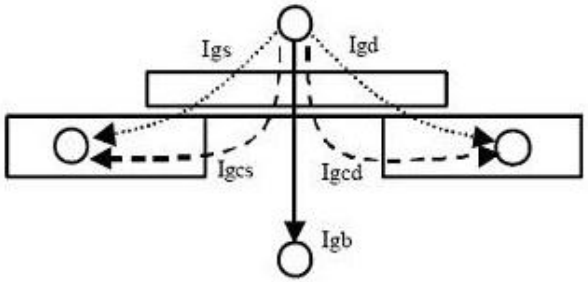


Flashback - 2001

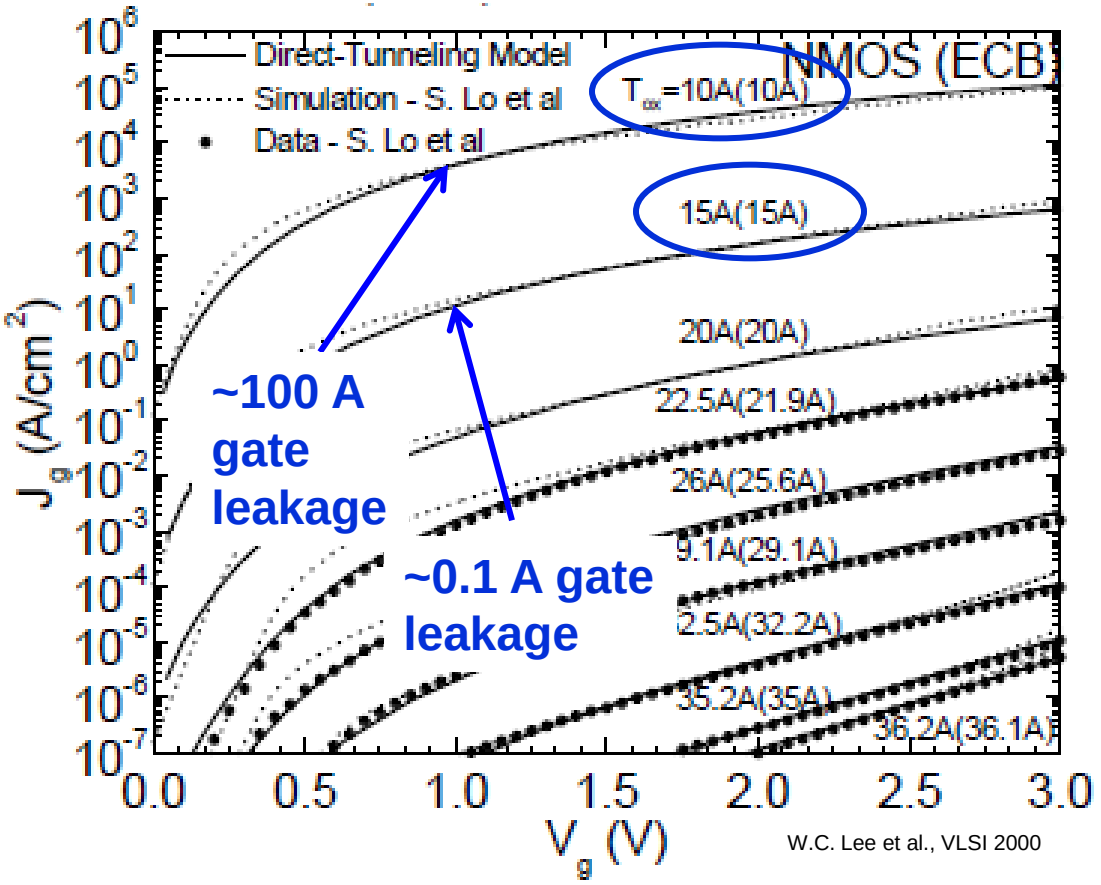


- **Enhanced 130 nm technology device from Intel**
  - **Scaled gate length (less than half of node value)**
  - **Poly-silicon gate**
  - **Thin SiO_2 gate dielectric – 1.5 nm**

Flashback - 2001



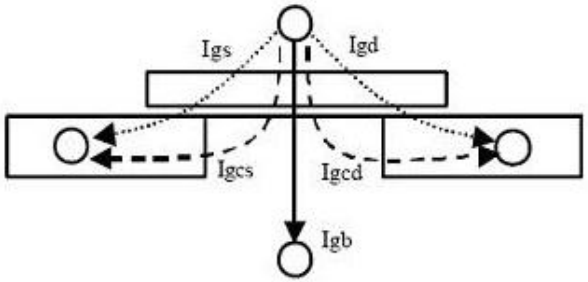
Road-block: Gate oxide tunneling current, the quantum nature of matter lets electrons penetrate the gate oxide



W.C. Lee et al., VLSI 2000

- **Scaling to gate oxide the next node by 30% proved impossible**
  - **Gate oxide leakage jumps from ~1 Amp to ~1000 Amps between 1.5 nm and 1.0 nm thick SiO_2 dielectrics**

Flashback - 2001



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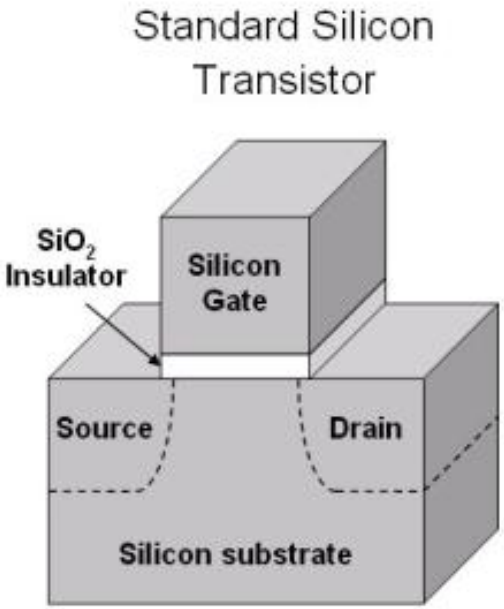
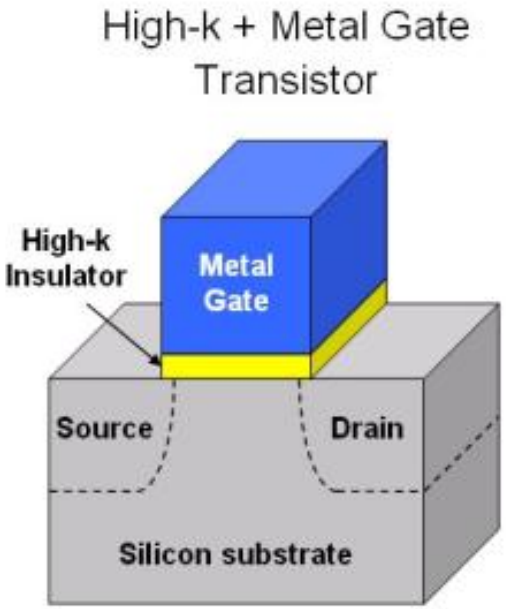
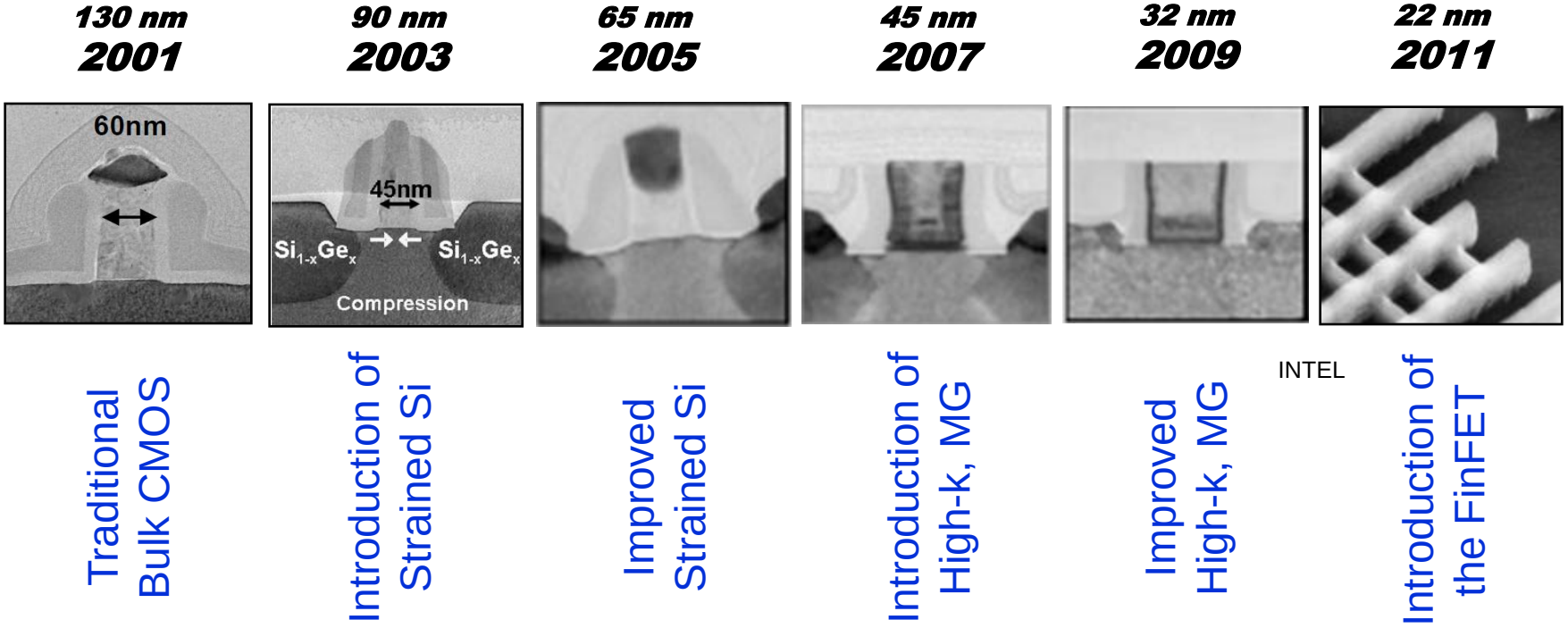




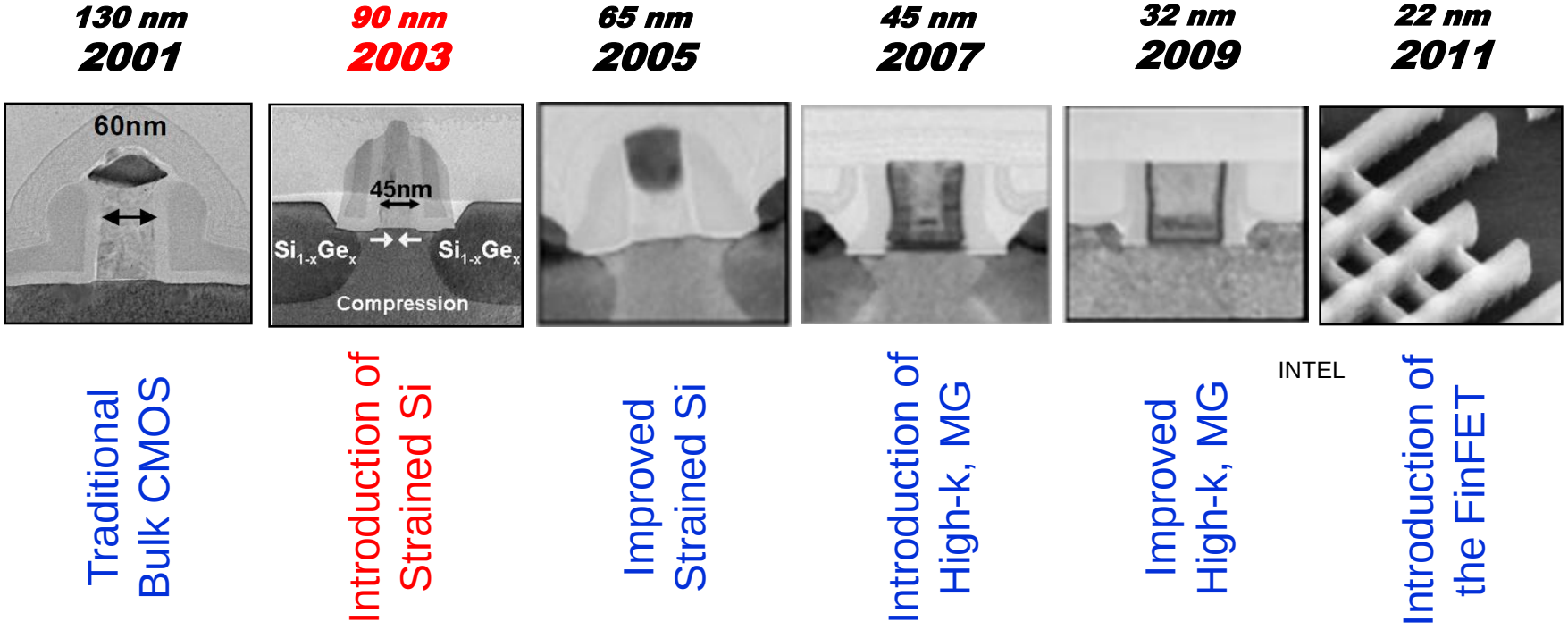
- **Ideal Solution – Replace the leaky silicon dioxide with a high-k dielectric and eliminate poly-Si depletion in the gate by using a metal gate**
- **Reality – Not so easy – Thousands of papers were published on high-k metal gate, and the solution is not ideal**

A Decade of Nanoelectronics



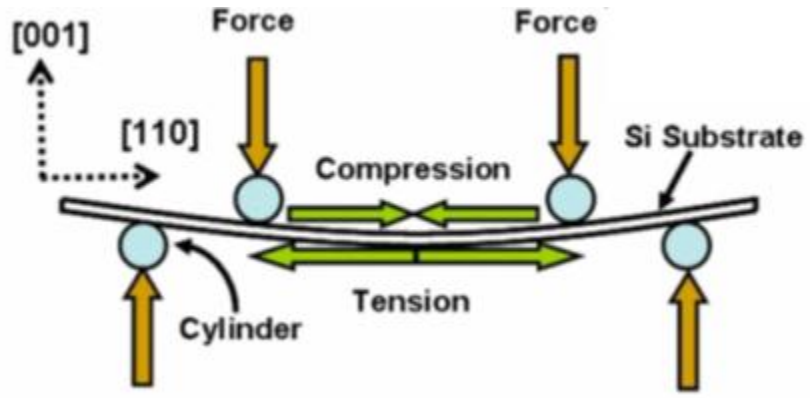
- **The challenge posed by the end of silicon dioxide scaling led to many innovations in the last decade**
  - **Strained silicon (2003), High-k/Metal Gate (2007), FinFET (2011)**

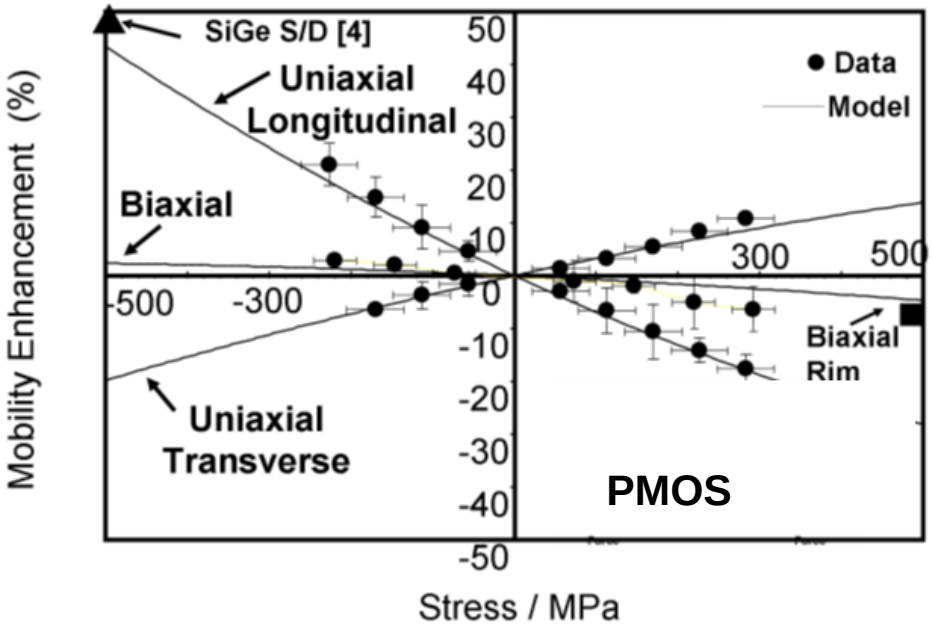
Introduction of Strained Si



- **High-k/Metal Gate proved so difficult that the industry had to look elsewhere to find a performance boost**
- **Strained Silicon was introduce by Intel in 2003 in the 90 nm node**

Strain Engineering (I)





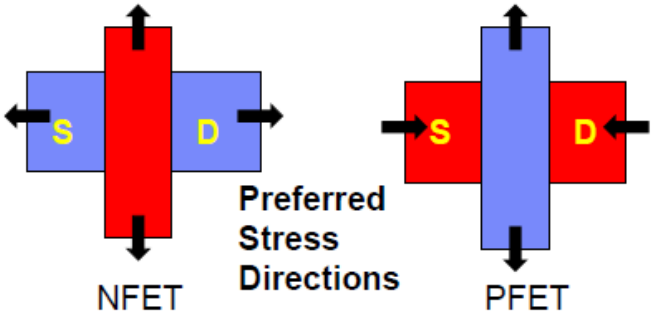
- **Straining silicon changes mobility and can improve device performance**
- **Uniaxial Longitudinal stress is very effective in enhancing performance**
  - **Compressive – PMOS**
  - **Tensile – NMOS**

LOW STRESS PIEZORESISTANCE COEFFICIENTS FOR 3 DIRECTIONS OF STRESS: LONGITUDINAL, TRANSVERSE, AND PERPENDICULAR TO PLANE OF THE MOSFET (z IS QUANTIZED DIRECTION).

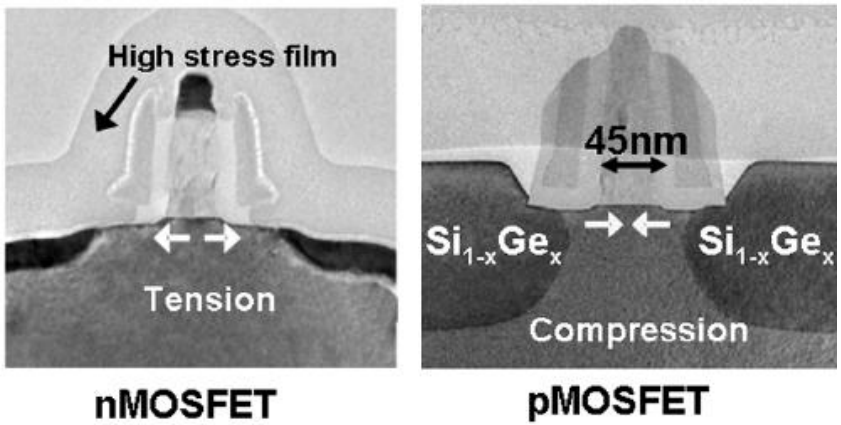
Wafer	(001)				(110)
Channel	⟨110⟩		⟨100⟩		⟨110⟩
Type	NMOS	PMOS	NMOS	PMOS	PMOS
$\pi_{\parallel}$	-35.5	71.7	-38.55	9.1	27.3
$\pi_{\perp}$ (in)	-14.5	-33.8	-18.7	-6.19	-5.1
$\pi_{\perp}$ (out)	27.0	-20.0	–	–	-25.8

S. Thompson et al. (various)

Strain Engineering (II)



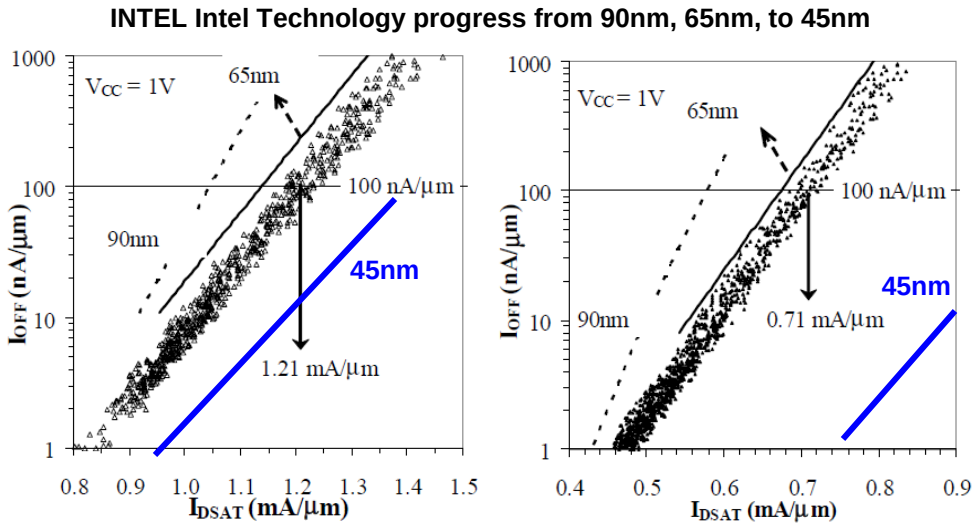
INTEL 90nm logic technology TEMs



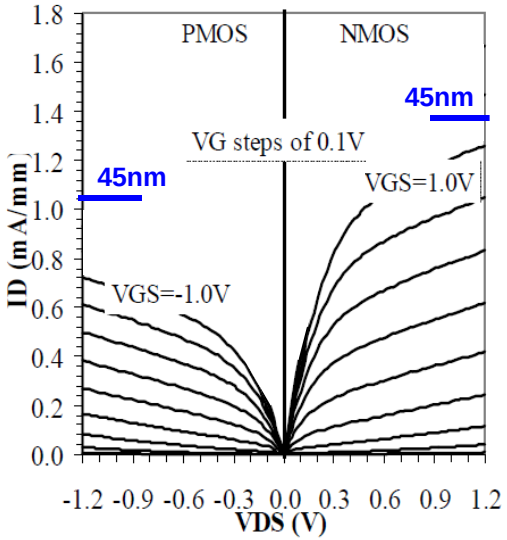
- Different strain configurations required for NMOS and PMOS
- NMOS strain strategy
  - Devices are strained with properly stressed liner films (strain perpendicular to gate) and spacers (strain parallel to gate)
- PMOS strain strategy
  - Devices are strained with an embedded SiGe epitaxial layer in the source/drain that compresses the channel (perpendicular to gate) and spacers (strain parallel to gate)

S. Thompson et al., IEEE TED, VOL. 51, NO. 11, NOVEMBER 2004

Strain Engineering (III)



NMOS V_{dd} = 1.0V PMOS

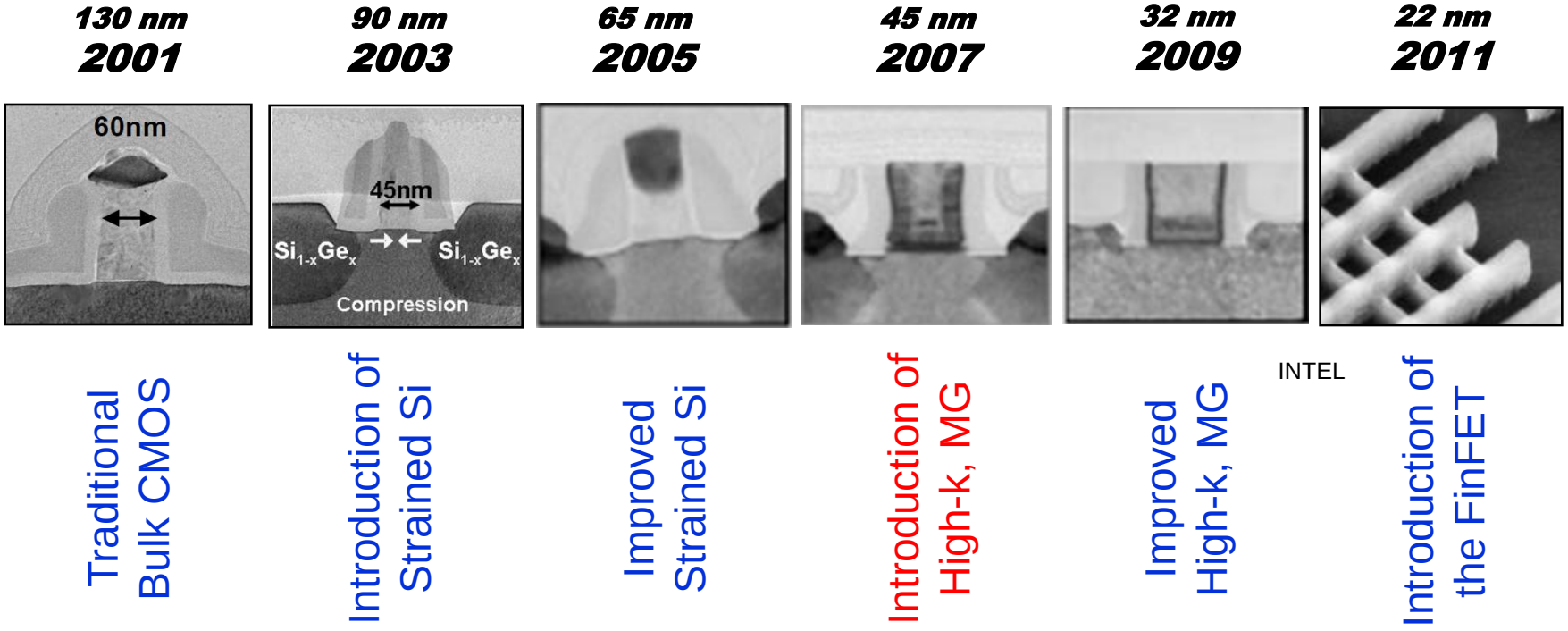


Advanced 65nm I_d - V_d

- **Technology Nodes from 90nm to 45nm have been optimizing the strain effect increasing device performance**
- **PMOS benefits more from strain than NMOS**
  - **65nm node – 1.4x NMOS, 2.1x PMOS (mobility gain vs unstrained)**
- **As a consequence PMOS currents are catching up to NMOS**

S. Tyagi – IEDM 2005 pg. 245

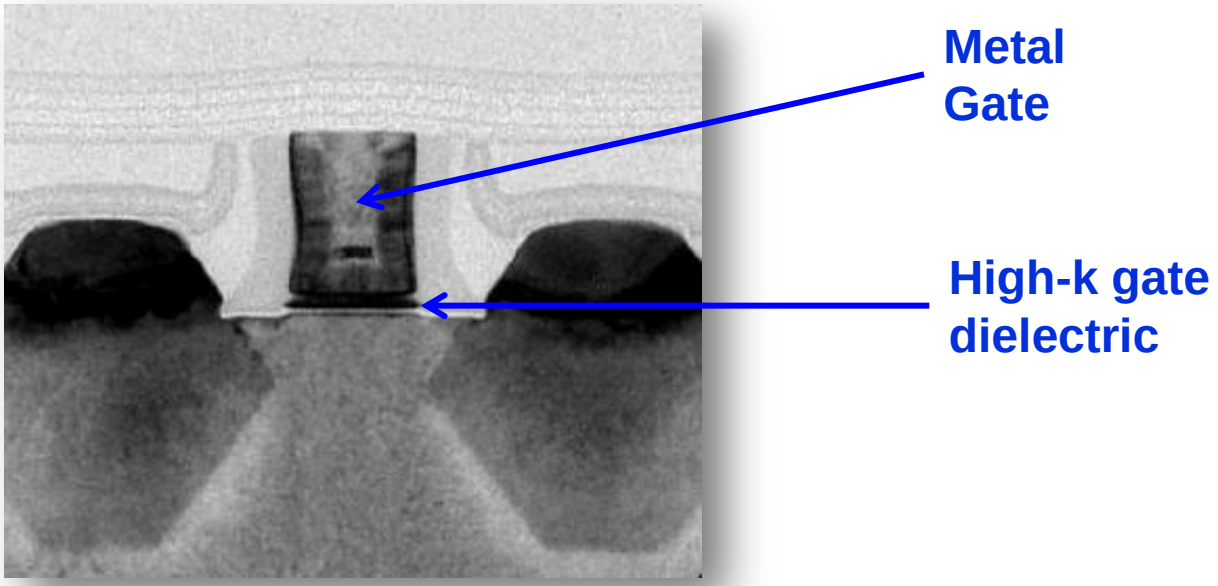
Introduction of High-k / Metal-Gate



- **Strain is great, but it doesn't do anything to solve the original problem of gate oxide leakage**
- **To solve gate oxide leakage issues high-k and metal gate were introduced in the 45 nm node by Intel**

Metal Gate (I)

INTEL 45nm logic technology TEMs

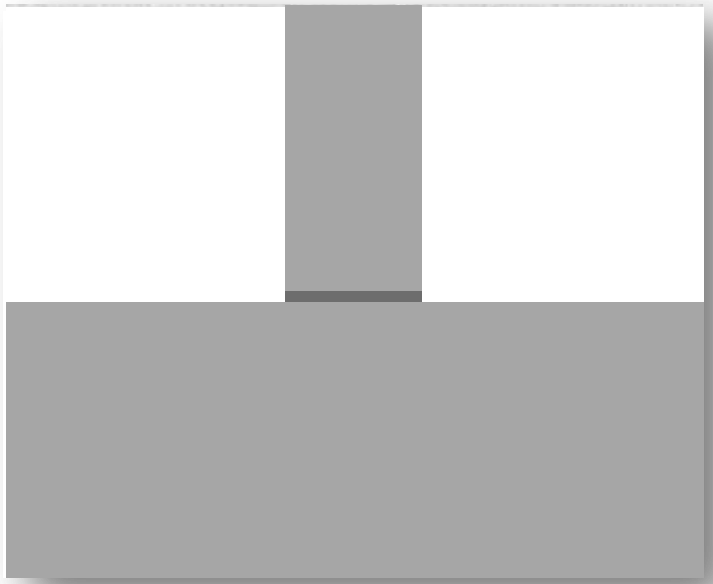


K. Mistry et al., 2007 IEDM p. 247

- The PMOS 45nm device with high-k, metal gate in cross section
- Gate-last process was used for fabrication, with two different metals (for NMOS and PMOS) over a $Hf_{(x)}Si_{(1-x)}O_2$ dielectric

Metal Gate (I)

- STI, Wells, and VT Implants
- **ALD deposition of high-k gate dielectric**
- Polysilicon deposition and gate patterning
- S/D extensions, spacer, Si Recess & SiGe deposition
- S/D Formation, Ni Salicidation, ILD0 Deposition
- **Poly Opening Polish, Poly Removal**
- **PMOS workfunction metal deposition**
- **Metal gate patterning, NMOS WF metal deposition**
- **Metal gate fill and polish, ESL deposition**



- **My interpretation of the high-k / metal gate process**
- **Transistor fabrication up to gate definition and etch**
  - **At this point gate is poly-Si on high-k $Hf_{(x)}Si_{(1-x)}O_2$ dielectric**
  - **Poly-Si gate is used because it can stand up to SD anneals**

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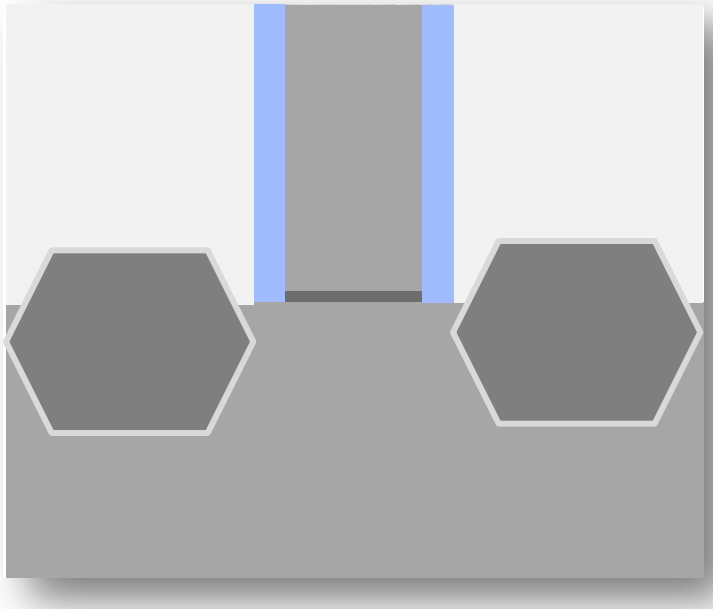

- **Spacer formation**
- **Source drain formation including strain SiGe (PMOS)**
- **Ni Silicidation and initial interlayer dielectric deposition**

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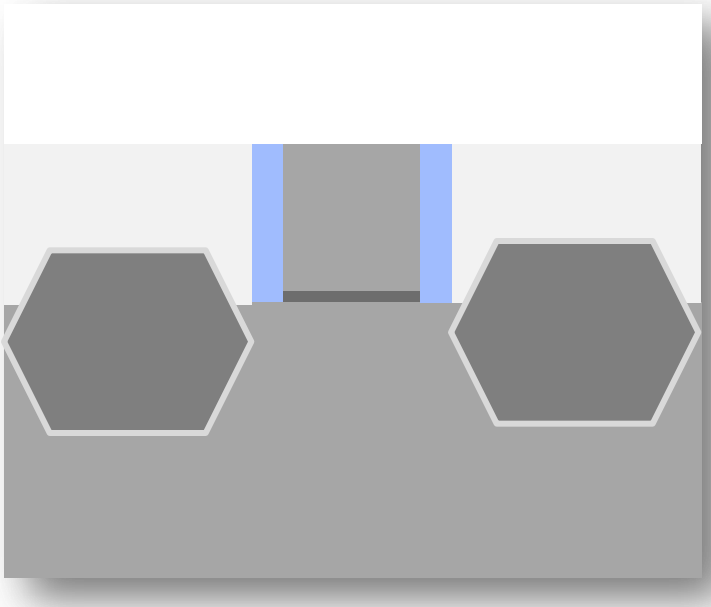

- **CMP for poly open**
  - **Exposes the top of poly to etch for removal**

Metal Gate (I)

- STI, Wells, and VT Implants
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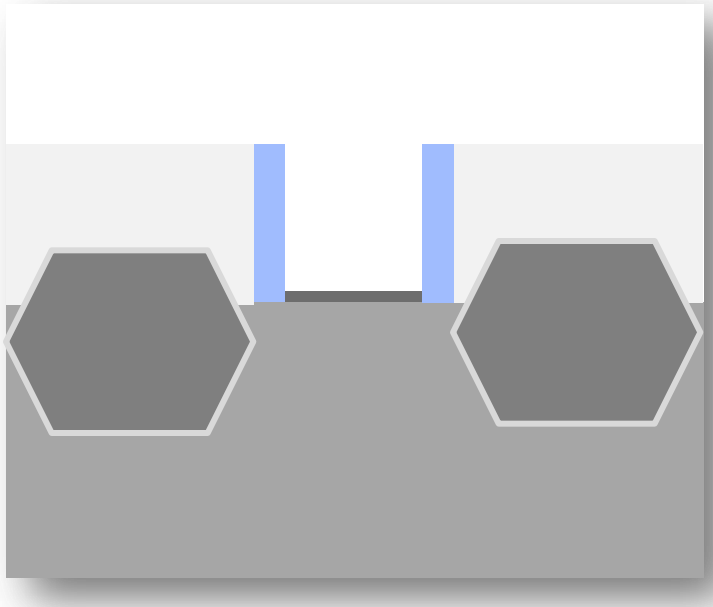

- **Poly removal**

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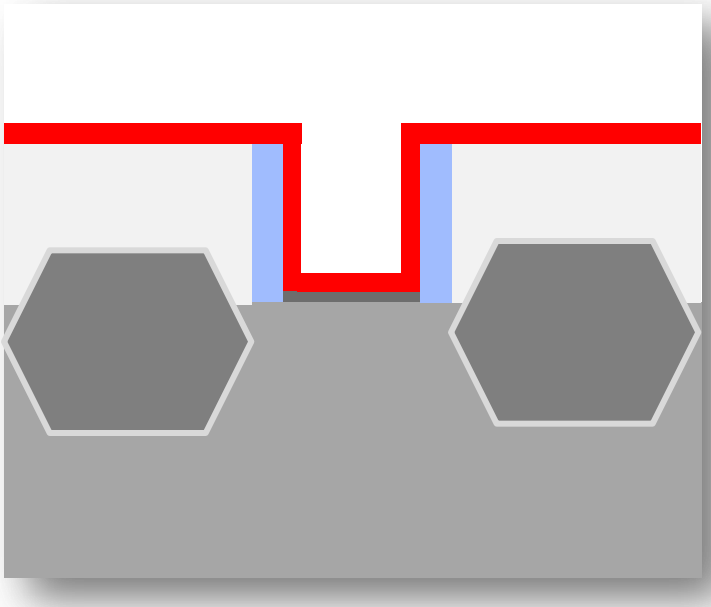

- **PMOS workfunction deposition**
  - **Undisclosed metal, likely a complex alloy, perhaps TaN with impurities to modify the workfunction**

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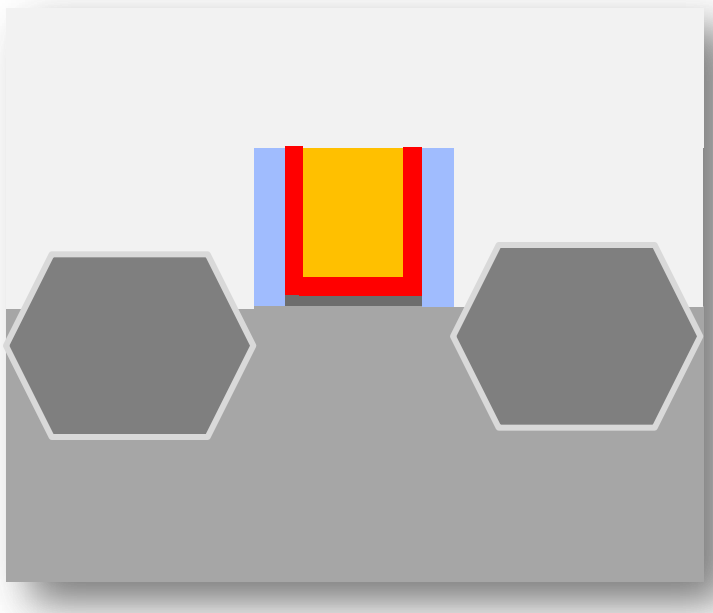

- **Similar process is used for NMOS**
- **Common metal fill is used to fill in the gate, potentially TiN or W**
- **Final CMP removes metal from undesired locations**
- **Secondary interlayer dielectric is deposited**

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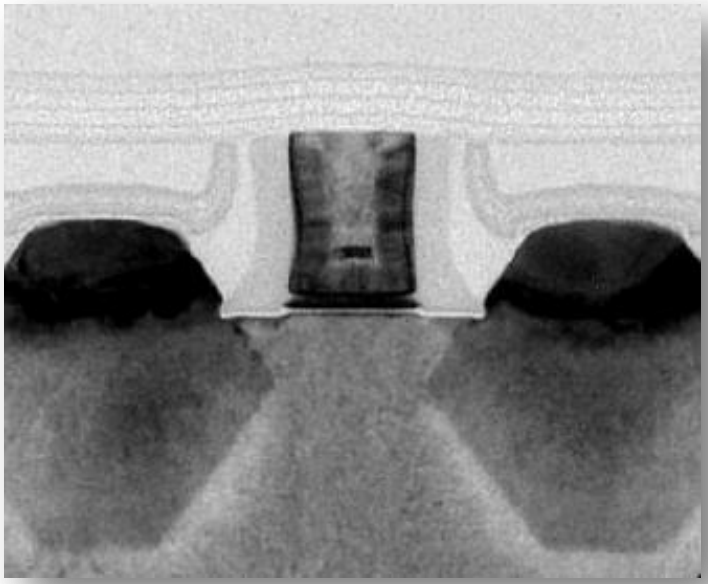
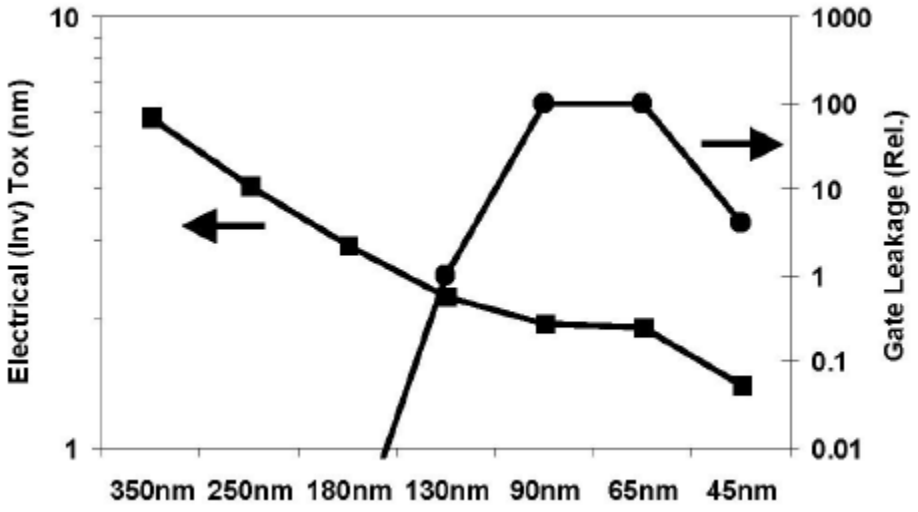
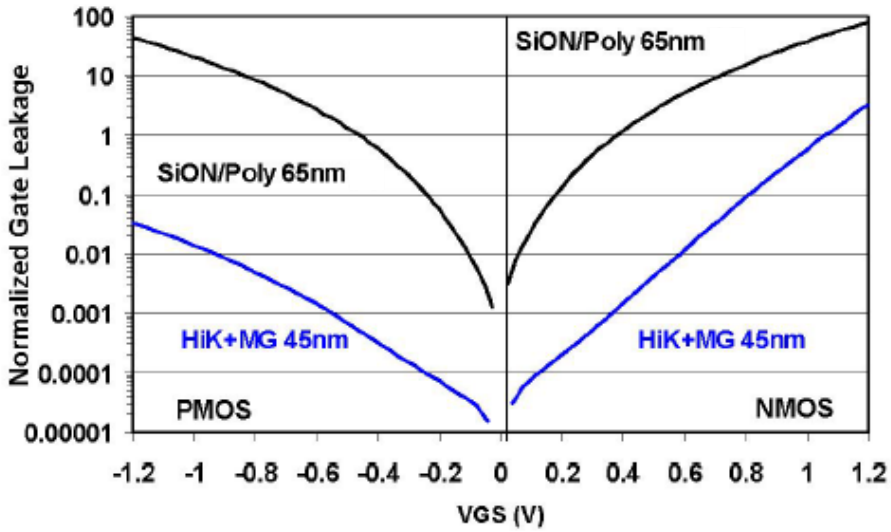


- **Finished 45 nm node high-k, metal gate PMOS device**

Metal Gate (II)

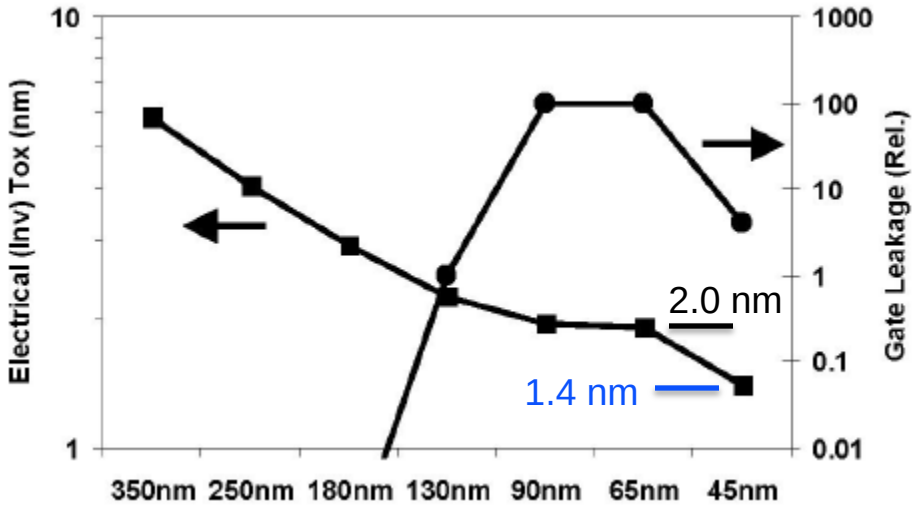




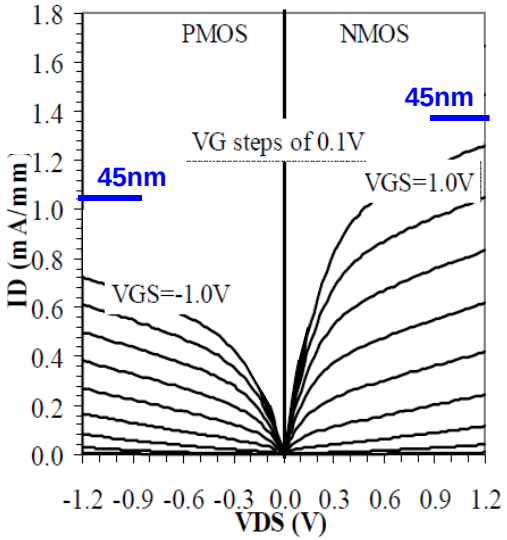
- Oxide scaling of SiO_2 has stopped at 90nm node due to the exponentially increasing gate leakage current
- Bulk transistor scaling is impossible without scaling the gate oxide thickness
- High-k, metal gate reduces effective oxide thickness and the gate leakage at the same time
  - 0.7x reduction in T_{ox}
  - 70x reduction in gate leakage (NMOS 1V)

K. Mistry et al., 2007 IEDM p. 247

Metal Gate (III)



40% Increase in C_{inv} in 45nm vs 65nm

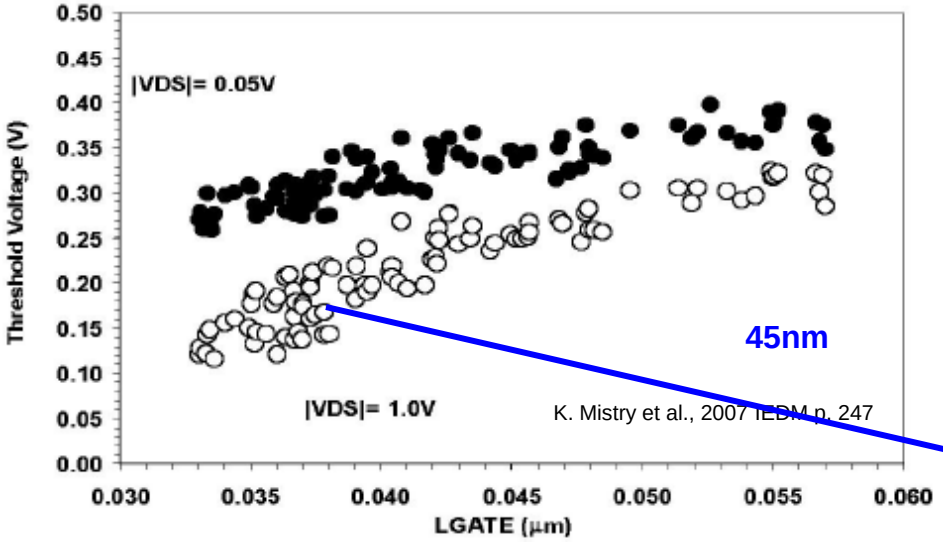


Comparison of 65nm vs 45nm

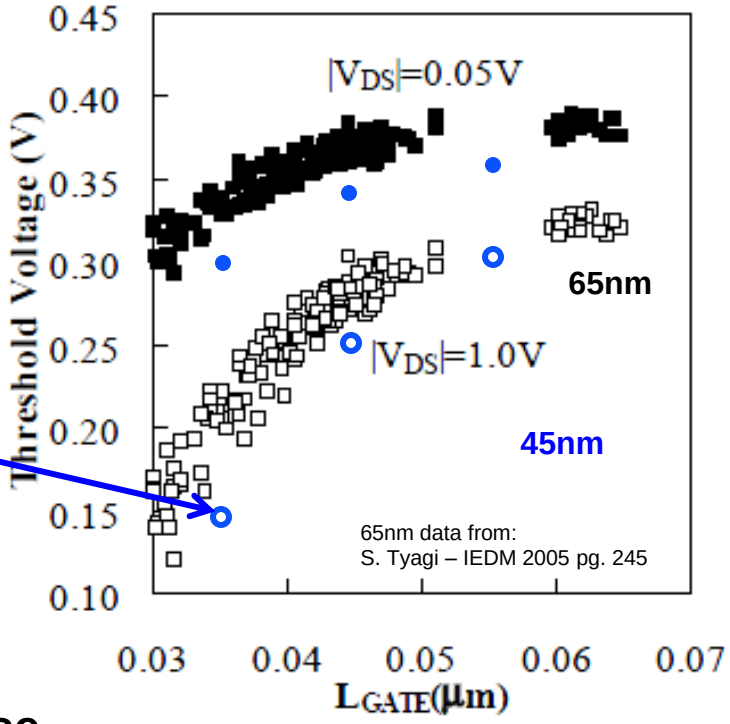
- **Metal gate high-k has reduced the electrical oxide thickness from 2.0 nm (65nm node) to 1.4 nm (45nm node)**
- **But NMOS currents have not increased in proportion**
  - **Mobility is reduced by the high-k**

K. Mistry et al., 2007 IEDM p. 247

Metal Gate (IV)



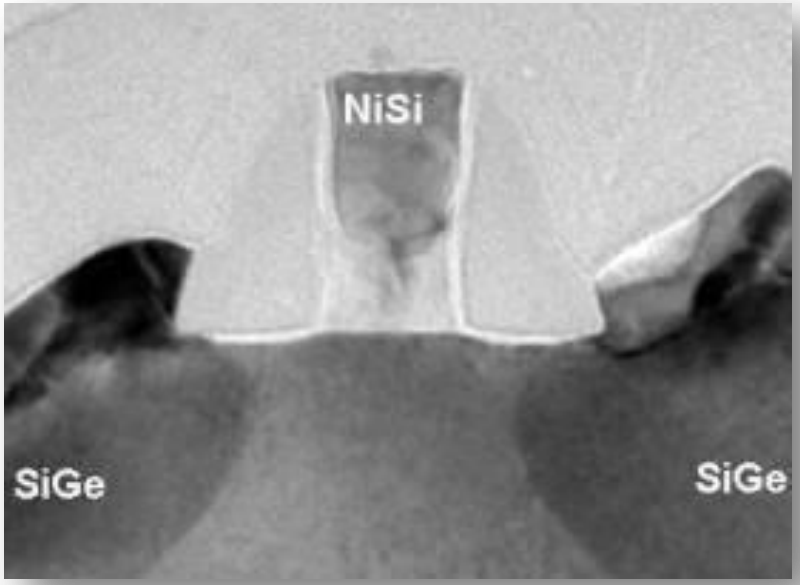
NMOS V_t roll-off 45nm



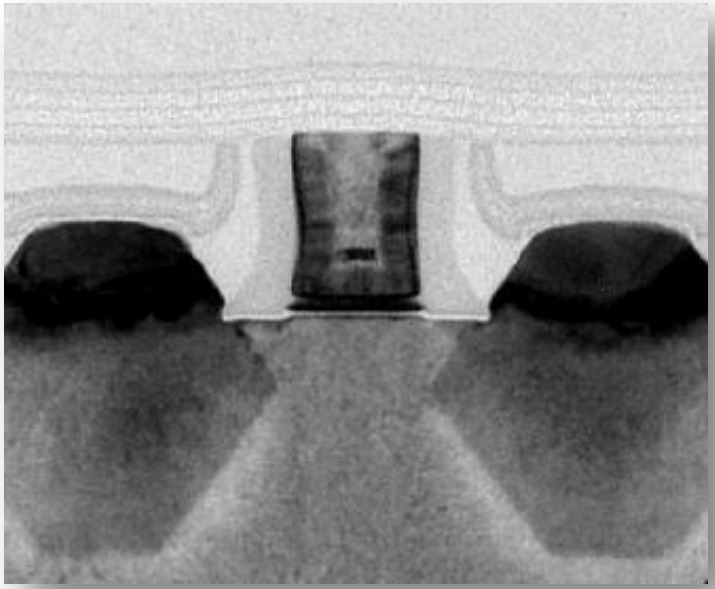
NMOS V_t roll-off 65nm vs 45nm

- **V_t roll-off characteristics for 45nm**
  - **45nm short channel effects are worse than 65nm**
- **45nm and 65nm technology gate length is almost identical**
  - **~45 nm in the SRAM cell**

What Happened to Gate Scaling?



65mn node – L_g = 45nm

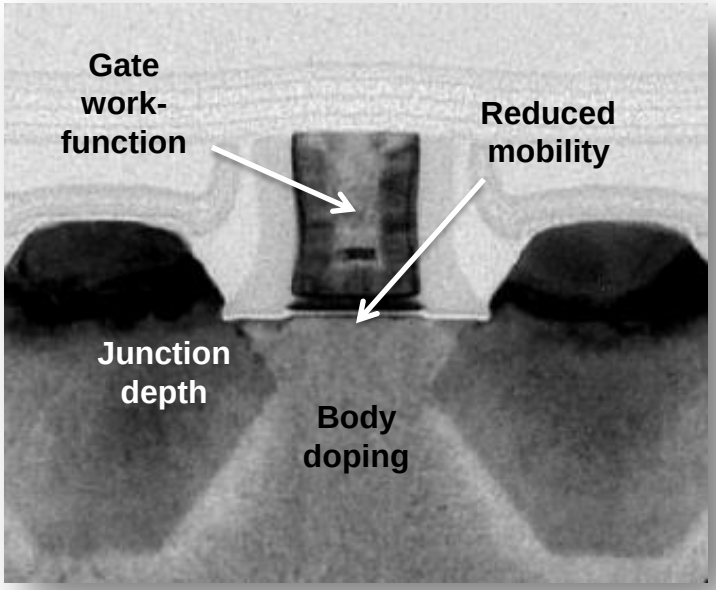


45mn node – L_g = 45nm

- **45nm node devices with high-k metal gate scale the same as 65nm node devices without high-k metal gate**
- **What happened to scaling!**
- **Wasn't the whole point of high-k metal gate to enable scaling?**

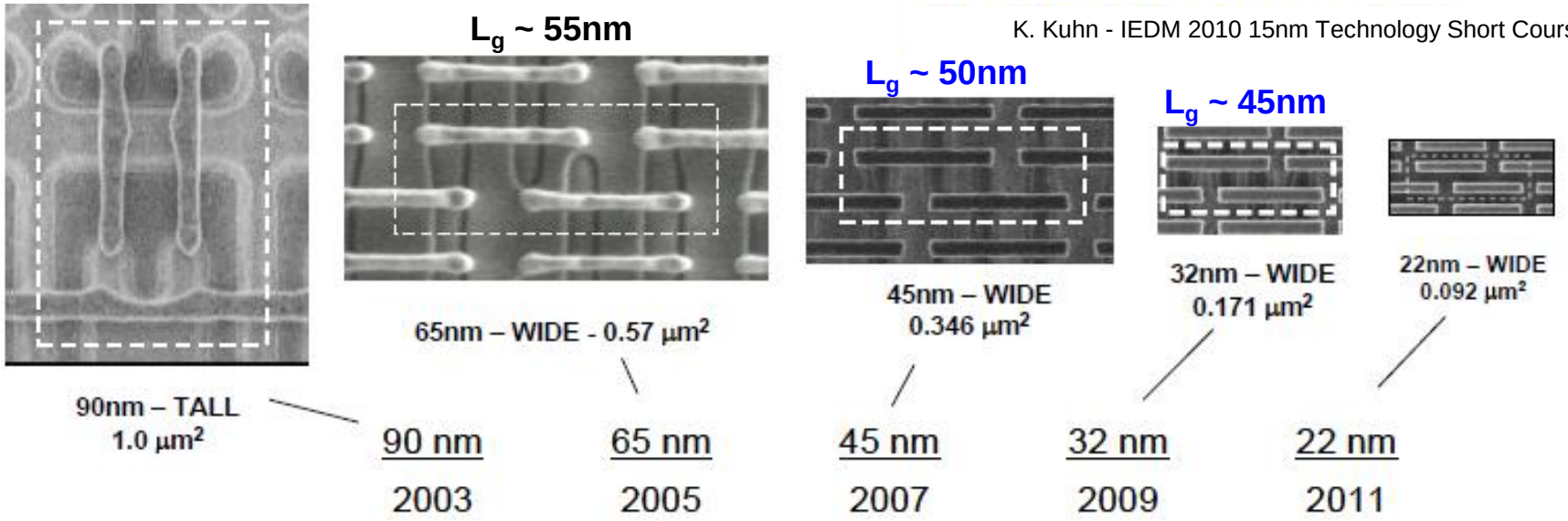
What Happened to Gate Scaling?

- **Why are high-k / metal gate bulk devices not as scalable as hoped?**
- **Body doping is hard to scale up**
  - **Vertical field reduces mobility this effect is often worse in High-K systems**
  - **Metal gate work-functions may not be all the way to band edge requiring lower body doping for same V_t**
- **Shallower junctions have high resistance and are difficult to integrate with all the stress engineering features**
- **High-k / metal gate is not really a scaling solution, it is a gate leakage solution**



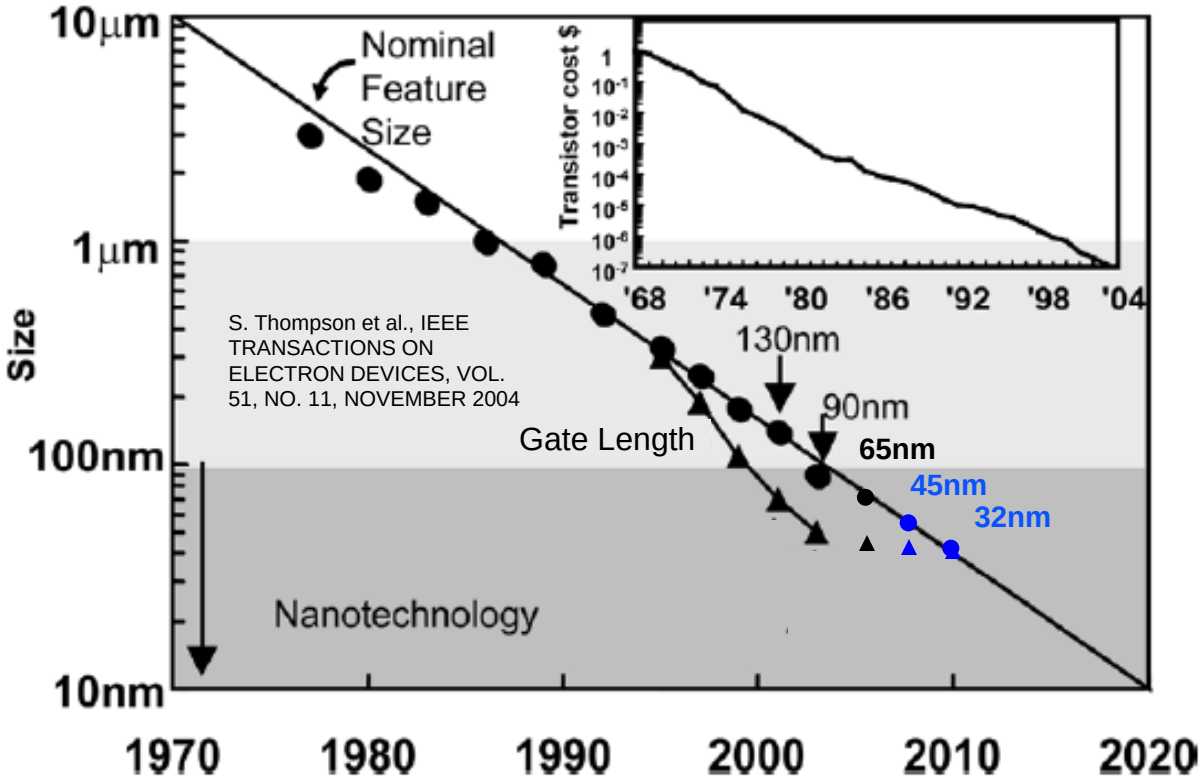
Factors contributing to the non-scaling of bulk transistors past the 65nm node

Gate Scaling Crisis (I)



- **SRAM gate scaling has been scaling slowly for the last 3 nodes**
- **SRAM gate pitch and active pitch have been scaled aggressively**
  - **Gate-to-gate spacing is 67nm at 32nm node down from 155nm at 65nm node**
- **Nominal size $\sqrt{A_{SRAM}}/12$ has scaled appropriately with technology node**

Gate Scaling Crisis (II)



- **Scaling has been on track, the nominal feature size** $\approx \sqrt{A_{SRAM}}/12$ **scaling with technology node**
- **But at the 32nm node the gate occupies ~50% of SRAM area, further area scaling without gate is running out of steam**

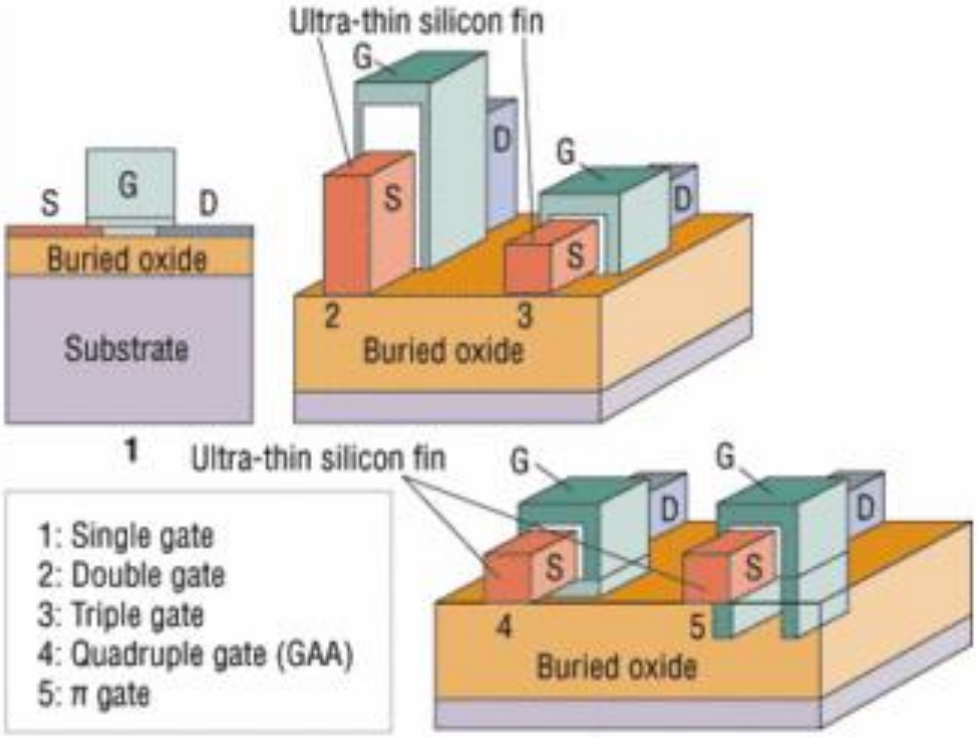
Gate Scaling Crisis (III) - Solutions

- **Evolutionary approach**
  - **Traditional bulk devices can always be optimized more**
  - **Short channel effects could be controlled with body dose but this will likely lead to lower drive**
  - **Keep scaling everything but gate length, particularly with very narrow width CMOS**
  - **Low risk, limited benefit**

- **Revolutionary approach**
  - **Abandon the bulk device and adopt a more scalable device architecture**

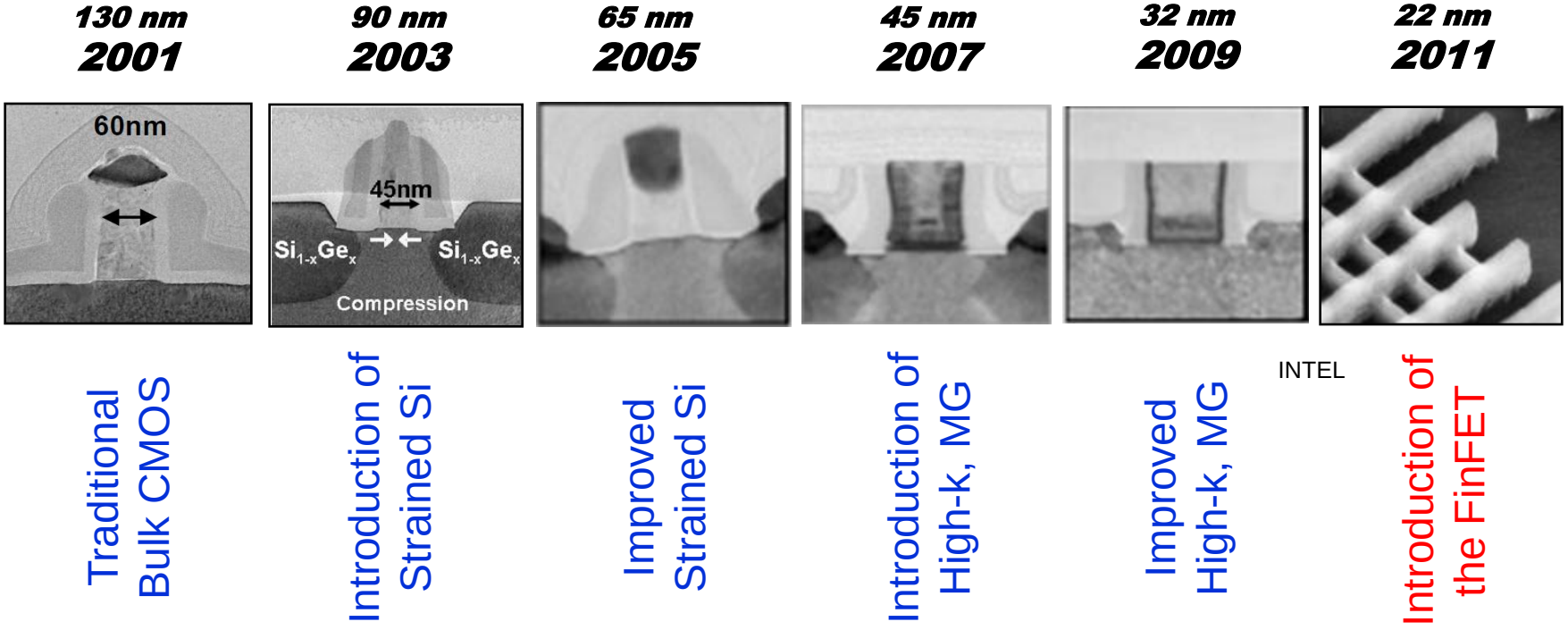
Gate Scaling Crisis (IV) - Solutions

- **Options: FDSOI, FinFET, trigate, gate-all-around, π-gate**



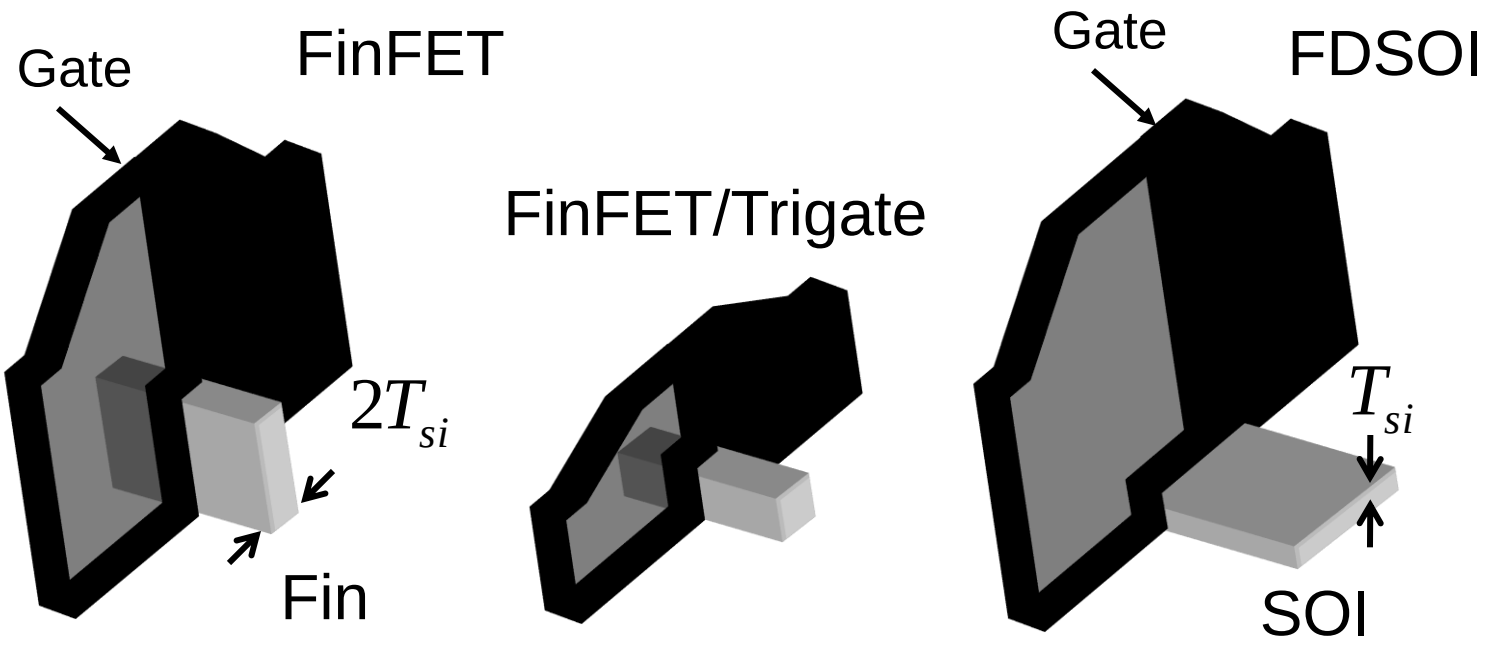
- **In these architectures scaling length includes T_{si} which can be varied independently from the gate oxide thickness**
- **Multiple gates help control short-channel effects**

Introduction of the FinFET



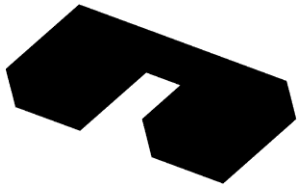
- **To solve the scaling crisis Intel introduced the FinFET device architecture in the 22 nm node**
  - **(also described as a tri-gate or 3D transistor)**

Historical Detour – FinFET, FDSOI

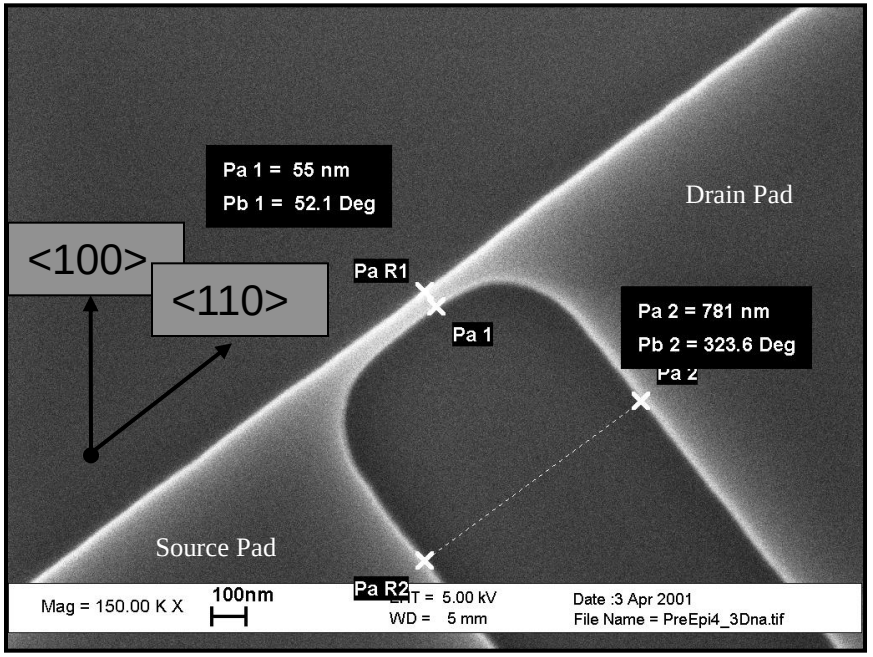


- **IBM, Intel, and TSMC have been developing FinFET and FDSOI technology**
- **I will take a step back and look at some IBM FinFET development work from 2001-2003**

FinFET- Fin Formation

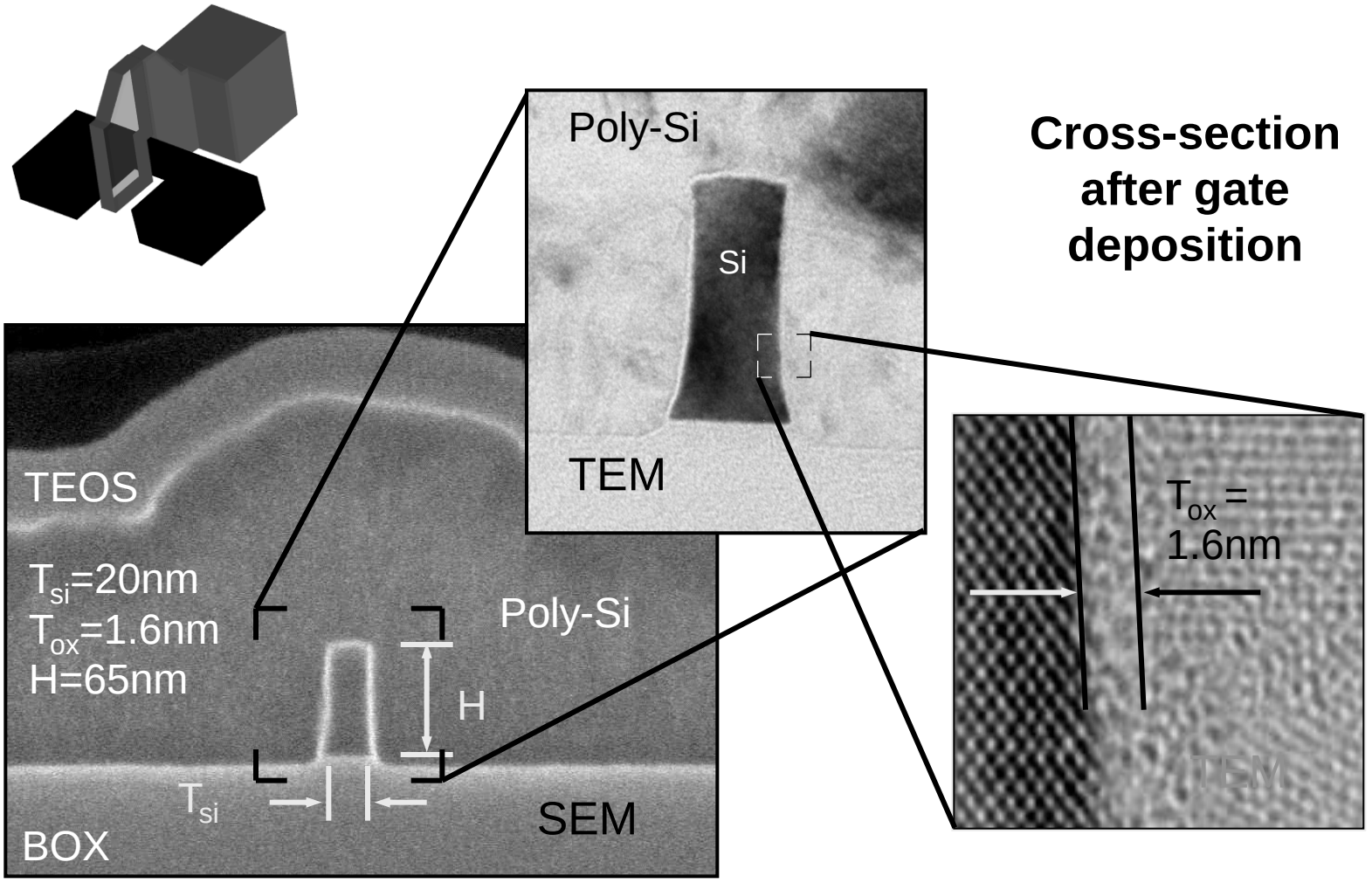


- **Start with SOI**
- **Etch silicon Fin**
- **Gate oxidation**
- **Gate deposition (poly-Si in this case)**

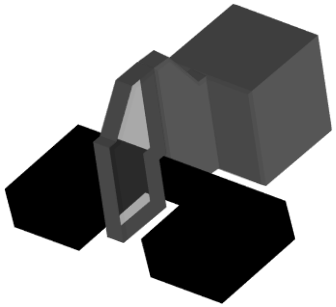


A <110> directed Fin after etch

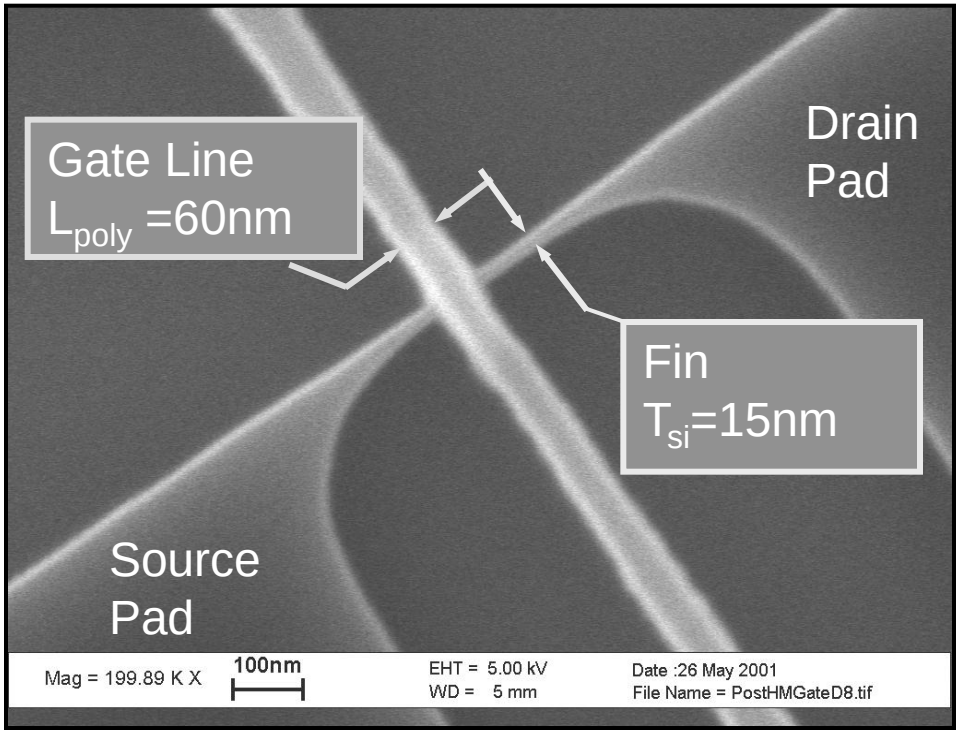
FinFET- Gate Stack



FinFET- Gate Etch, Spacer etch

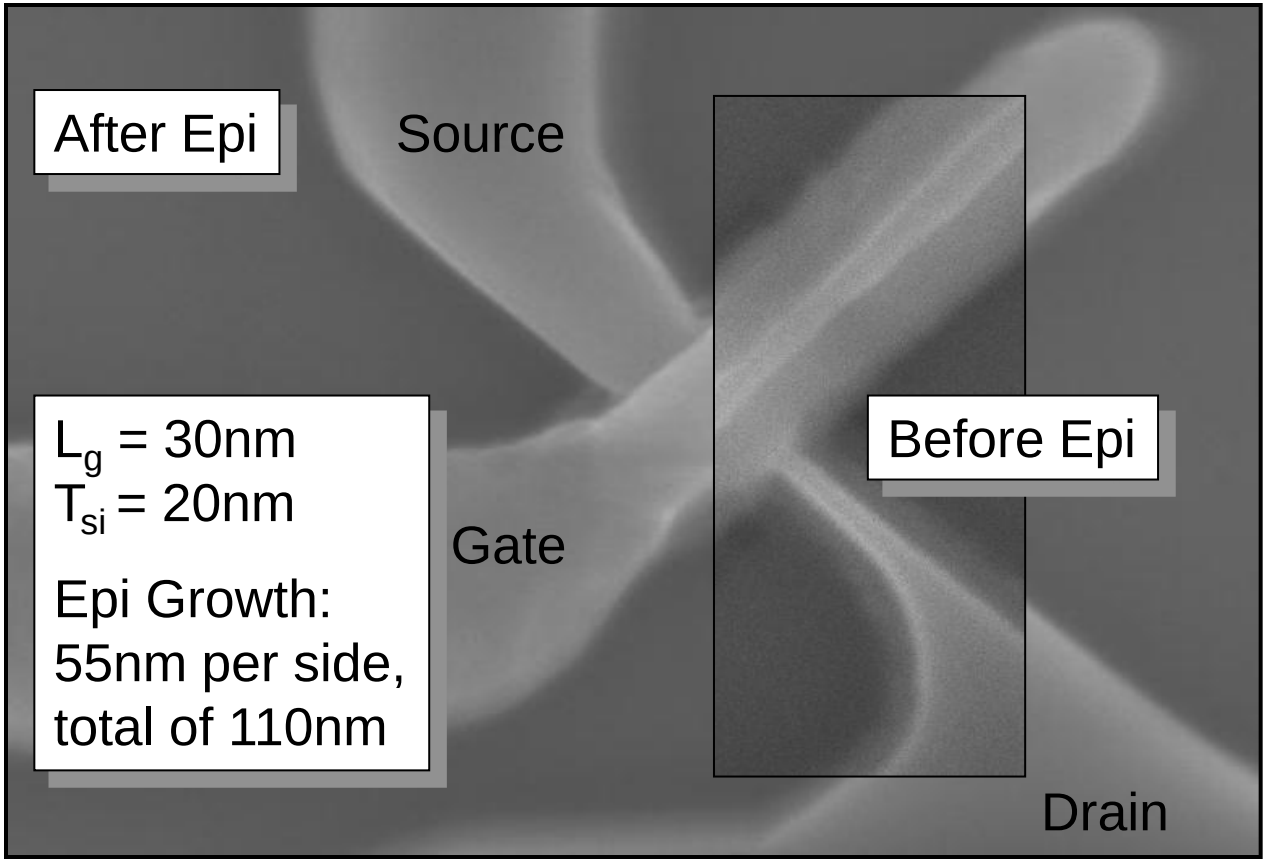


- **Gate etch requirement**
  - **Must over-etch gate from the sides of the fin without damaging corners**
- **Spacer etch also can't damage the fin**



Top-down SEM after gate etch

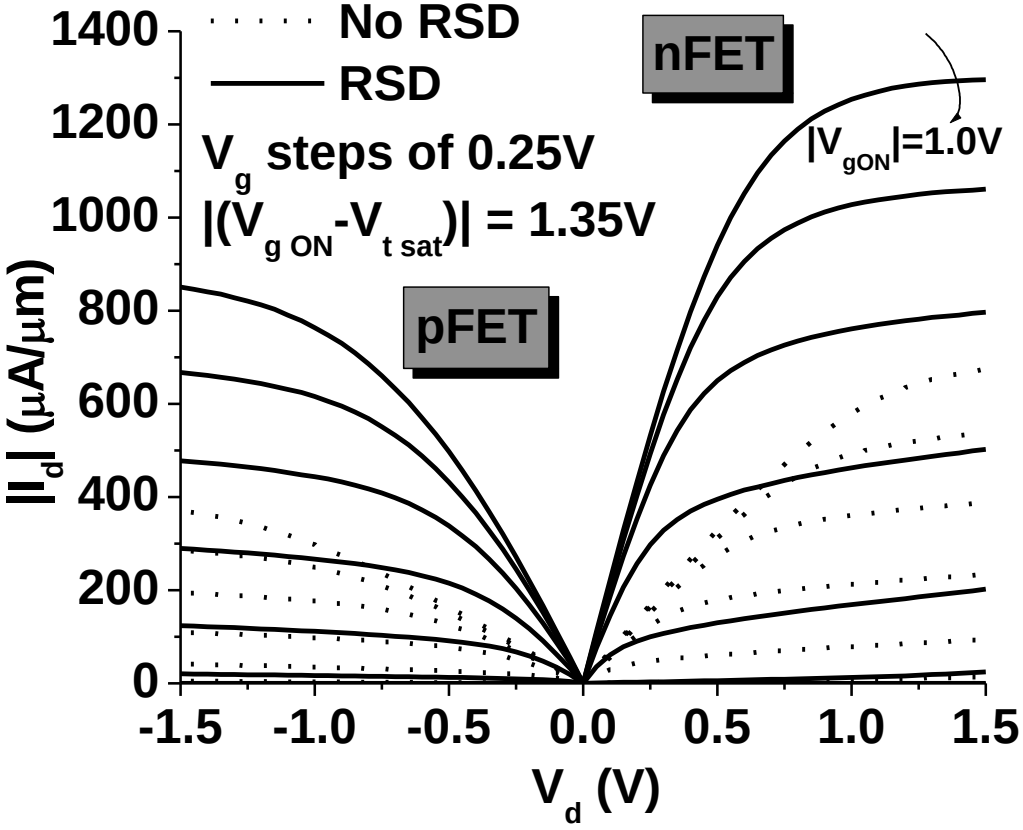
FinFET- Raised Source/Drain



Top-down SEM before and after raised source/drain (RSD)

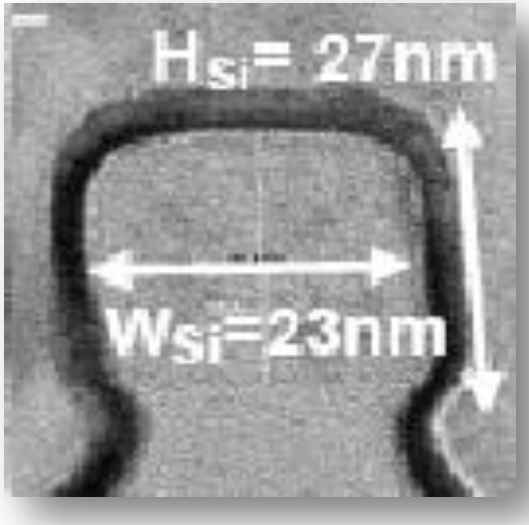
FinFET- Electrical Results

- RSD has significant impact on FinFET current
- NMOS and PMOS current ratio is impacted by the <110> fin direction
  - <110> hole mobility is higher than <100>
  - <110> electron mobility is lower than <100>



FinFET for 22 nm Node

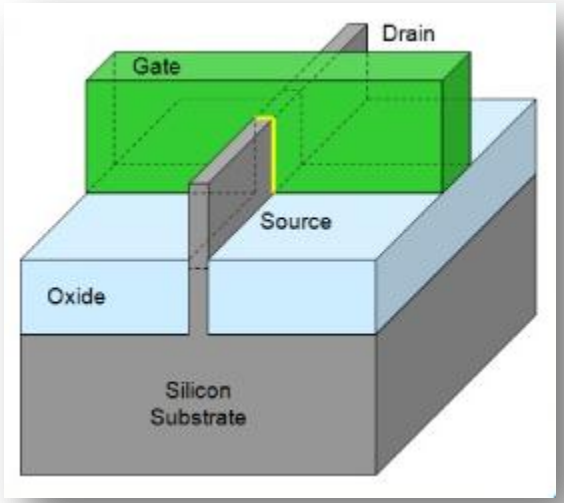
- **FinFET structures are being implemented at the 22 nm node**
- **All the critical device enhancements must be integrated into the FinFET for it to be competitive**
- **Strain Engineering**
  - **Liner and spacer strain is easy to implement in FinFETs, FinFETs maybe easier to strain for NMOS enhancement**
  - **E-SiGe processes are more challenging for FinFETs but could be implemented in RDS for PMOS**
- **Metal Gate, High-k**
  - **Not significantly different than integration into bulk devices**
  - **More flexibility with the workfunction**

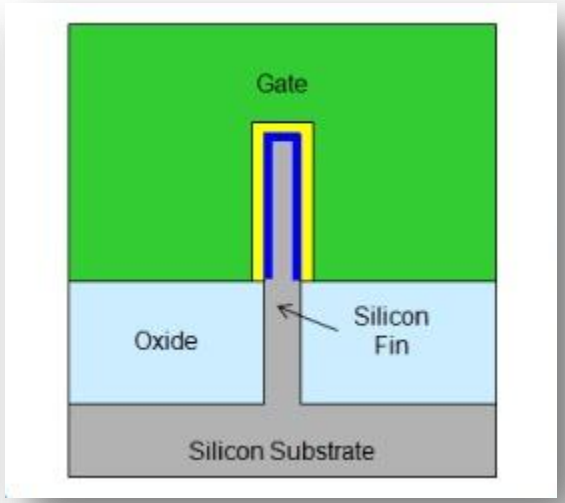


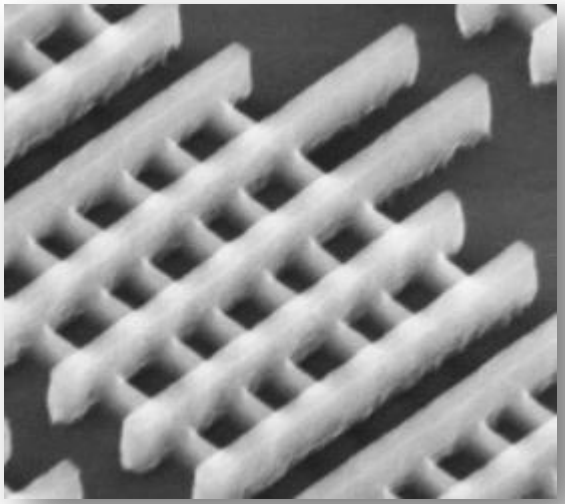
Intel's metal gate, high-k FinFET at Research stage (2006), not the final 22nm device (2011)

J. Kavalieros et.al, VLSI Symposium Tech p. 50-51, 2006

FinFET for 22 nm Node





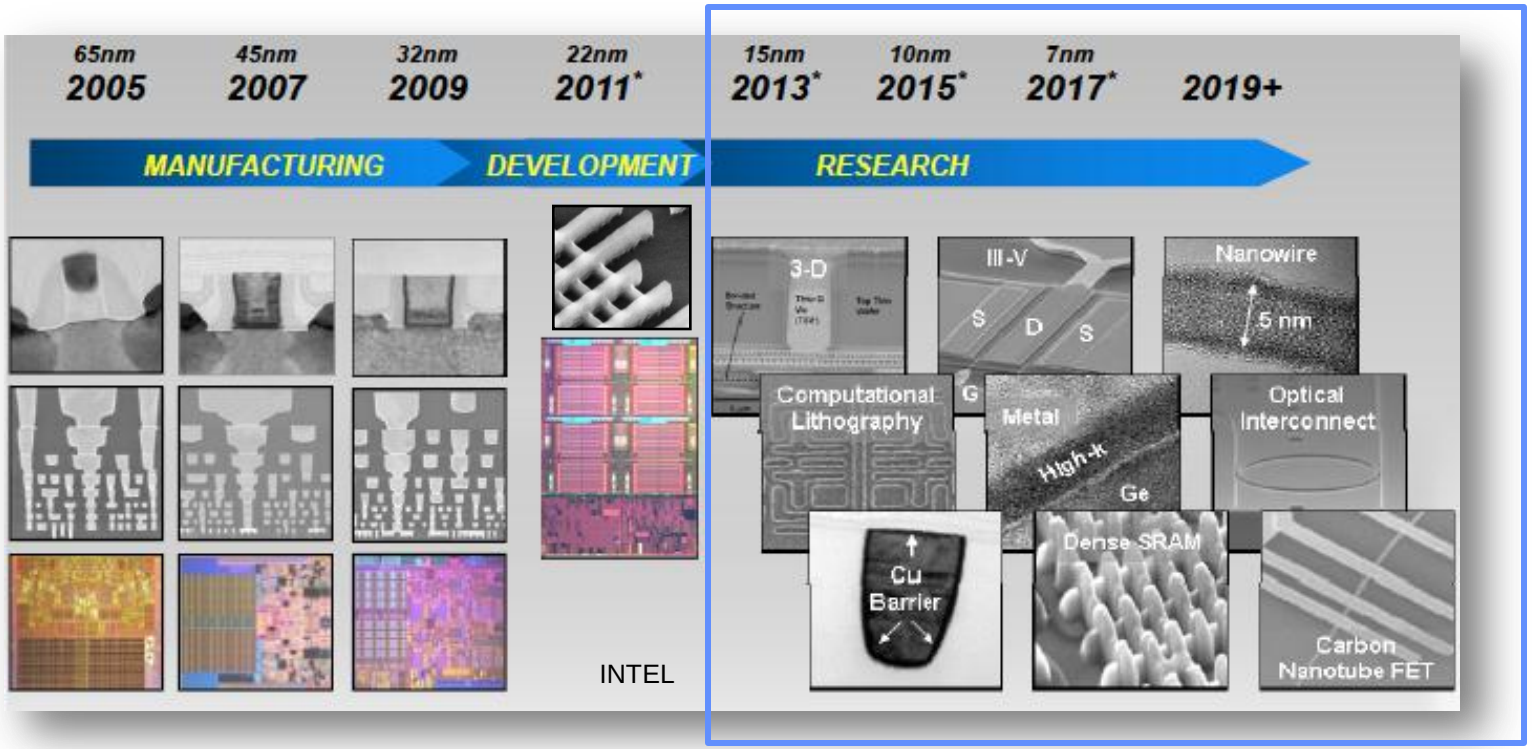


Intel's bulk FinFET

- **Not much is known about the 22 nm node yet**
- **It is known that the device is a bulk FinFET, with high-k / metal-gate, and very likely with some stress liners**
- **Stay tuned to IEDM 2011 in December**

INTEL – Press Releases

Into the Future



- **In what direction will future technology develop?**
  - **Will the next decade of nanotechnolgy be as exciting as this one?**
  - **As usual there are many technology options competing for attention**

K. Kuhn - IEDM 2010 15nm Technology Short Course

Into the Future

SILICON

- Scaled silicon wrap around gate devices
- Massive 3D integration
- Near and subthreshold electronics
- Tunneling devices

EVERYTHING ELSE

- Ge and III-V devices
- Graphene devices
- Nanotube devices
- Organic devices
- Quantum computing
- Relays? Really?!

While non-silicon technologies may establish niche markets, but my prediction is that when you retire the predominant logic technology will still be based on silicon

Summary

- I hope I gave you a clearer understanding of where CMOS technology is and where it is going
  - Silicon has a very rich past and a promising future
  - Silicon maybe the dominant technology for next century
  - So if you don't do research in silicon, at least pay attention in class

- I will be at IITB for the next year
  - Feel free to contact me anytime at:

jakub@ee.iitb.ac.in