SANTA CLARA UNIVERSITY	ELEN 115 Spring 2023	Dr. S. Krishnan

Lab 6: MOSFET characteristics and CMOS Logic Gates

I. OBJECTIVES

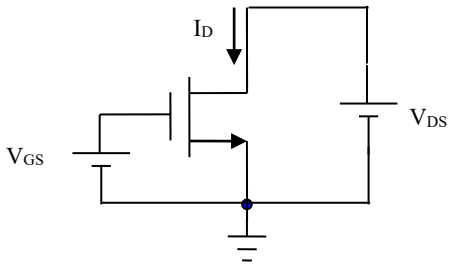
- To trace the **i-v** curves for a MOSFET.
- To study CMOS Logic gates

II. LAB

Part 1: MOS i-v characteristics

(a) Draw the MOS circuit given in Figure 1 in LTSpice (Make sure you connect the Body Terminal to Ground). You will use the NMOS4 component from the library.

Figure 1



(b) Edit the MOSFET model to provide the model parameters as used in the prelab. You can do this by including a command .MODEL MYNMOS NMOS VTO=0.6 KP=30u LAMBDA=0 GAMMA=0

(c) Connect a **DC** voltage source from drain to ground and call it VDS. Connect a **DC** voltage source from gate to ground and call it VGS.

(d) Set up a DC simulation that is a nested sweep. The statement is shown below.
.dc VDS 0 2.5 0.1 VGS 0 2.5 0.5

(e) Run the simulation and plot the collector current I_D vs. VDS for various VGS.

(f) Note the three regions of operation of the MOSFET – cutoff, linear and saturation.

Part 2: iv curve of a MOSFET

(i) Use the curve tracer in the lab to plot iv curves of the various MOSFETs given to you.

(ii) Note down the i-v curves of the various MOSFETs you measure.

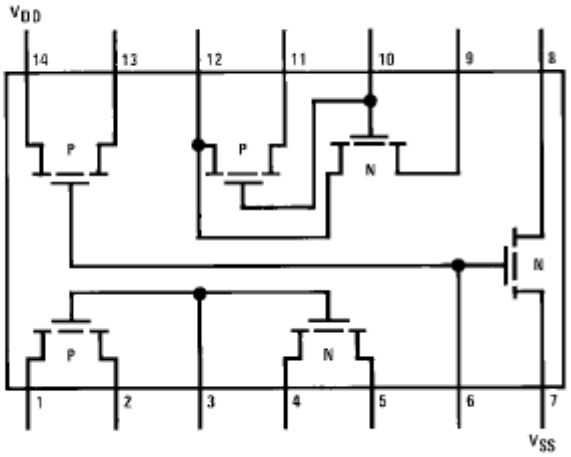
TA Check Point: Complete Part 2 and show your TA that you are proficient in using the curvetracer.

Part 3: Physical build of CMOS Logic gates

You will be using the chip CD4007C whose pinout is shown below. The data sheet gives you all the electrical details of the chip. Remember to connect power and ground to the chip.

Connection Diagram

Pin Assignments for DIP and SOIC



Note: All P-channel substrates are connected to V_{DD} and all N-channel substrates are connected to V_{SS}.

Top View

A. <u>NOT gate</u>

(a) Look at this chip pinout and draw a schematic with pin numbers for the NOT logic gate.
(b) Build a logic inverter or NOT gate using the CD4007C chip provided to you.
(c) Provide a pulse input that switches between "0" (0V) and "1" (5V).
(d) Observe the output to obtain the truth table for the gate.
(e) Explain the operation of this gate and what each MOSFET is doing.

B. <u>NAND gate (2 input)</u>

(a) Look at this chip pinout and draw a schematic with pin numbers for the NAND logic gate.
(f) Build a two-input NAND gate using the CD4007C chip provided to you.
(b) Provide pulse inputs for inputs A and B that switch between "0" (0V) and "1" (5V).
(c) Observe the output to obtain the truth table for the gate.
(d) Explain the operation of this gate and what each MOSFET is doing.

C. <u>OR gate (2 input)</u>

(a) Look at this chip pinout and draw a schematic with pin numbers for the OR logic gate.
(b) Build a two-input OR gate using the CD4007C chip provided to you.
(c) Provide pulse inputs for input A and B that switch between "0" (0V) and "1" (5V).
(d) Observe the output to obtain the truth table for the gate.
(e) Explain the operation of this gate and what each MOSFET is doing.

<u>IV. REPORT</u>

Prepare a detailed report that includes all simulation results. The lab report should contain the following:

Schematic printout of the circuits.
Printout of simulation results.
Answers to questions in the prelab and laboratory procedure.