Group Number:

NAMES (FIRST AND LAST NAME):

In-Class Assignment 3

ELEN 21/COEN 21 – Fall 2022
Instructor: Maria Kyrarini
Date: 11/15/2022
Time: 1 hour and 30 minutes
Number of pages: 3

Important Notes:

- Be sure to read all the problems carefully and answer all questions.
- Be sure to answer all parts of each question.
- **Submit only one answer for each question.**
- Multiple solutions for one question will not be graded.
- **Clearly show all the steps of your work.**
- **Answers without explanation will not be graded.**
- The Engineering School Honor Code applies.

Problem 1 (30 points)

Design a counter using positive edge D flip-flops that will count as follows:

- when X=0 and Y=0, the counter runs through the following states: 3,2,1,0,3,2,...
- when X=0 and Y=1, the counter runs through the following states: 0,1,2,3,0,1,...
- when X=1 and Y=d, the counter runs through the following states: 0,2,0,2,...

Draw a simplified circuit with a minimum number of flip-flops and a minimum network of AND, OR, NOT, and XOR gates.

Note: You can use the following Boolean Expression without proving it:

- $\overline{x \oplus y} = \bar{x} \cdot \bar{y} + x \cdot y$

Problem 2 (30 points)

A Moore state machine has an input w and an output z. The machine is a sequence detector that produces z = 1 when it detects 01; otherwise z = 0.

a) Draw the state diagram and provide the state-assigned table with the one-hot encoding approach. [10 points]
b) Derive a simplified circuit from the state-assigned table using JK flip-flops. **Note:** Do not draw the simplified circuit but describe it with equations. [20 points]

Problem 3 (30 points)

A Moore state machine has an input w and two outputs z1, z2. The machine is a sequence detector that produces z1 = 1 (z2 = 0) when it detects 111 and z2=1 (z1=0) when it detects 101; otherwise z1, z2 = 0.

a) Draw the state diagram. [20 points]
b) Provide the state table and the minimum state-assigned table. [10 points]

Problem 4 (10 points)

A universal shift register can shift in both the left-to-right and right-to-left directions, can hold values and it has parallel-load capability. Draw a circuit for such a 2-bit universal shift register.
Note: The problem will NOT be graded if explanation is missing.

Boolean Algebra Properties

5a.	$x \cdot 0 = 0$	10a.	$x \cdot y = y \cdot x$	*Commutative*
5b.	$x + 1 = 1$	10b.	$x + y = y + x$	
6a.	$x \cdot 1 = x$	11a.	$x \cdot (y \cdot z) = (x \cdot y) \cdot z$	*Associative*
6b.	$x + 0 = x$	11b.	$x + (y + z) = (x + y) + z$	
7a.	$x \cdot x = x$	12a.	$x \cdot (y + z) = x \cdot y + x \cdot z$	*Distributive*
7b.	$x + x = x$	12b.	$x + y \cdot z = (x + y) \cdot (x + z)$	
8a.	$x \cdot \overline{x} = 0$	13a.	$x + x \cdot y = x$	*Absorption*
8b.	$x + \overline{x} = 1$	13b.	$x \cdot (x + y) = x$	
9.	$\overline{\overline{x}} = x$	14a.	$x \cdot y + x \cdot \overline{y} = x$	*Combining*
		14b.	$(x + y) \cdot (x + \overline{y}) = x$	
		15a.	$\overline{x \cdot y} = \overline{x} + \overline{y}$	*DeMorgan's theorem*
		15b.	$\overline{x + y} = \overline{x} \cdot \overline{y}$	
		16a.	$x + \overline{x} \cdot y = x + y$	
		16b.	$x \cdot (\overline{x} + y) = x \cdot y$	
		17a.	$x \cdot y + y \cdot z + \overline{x} \cdot z = x \cdot y + \overline{x} \cdot z$	*Consensus*
		17b.	$(x + y) \cdot (y + z) \cdot (\overline{x} + z) = (x + y) \cdot (\overline{x} + z)$	