

Group Number: 5

NAMES (FIRST AND LAST NAME):

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In-Class Assignment 1

ELEN 21/COEN 21 - Fall 2022

Instructor: Maria Kyrarini

Date: 10/4/2022

Time: 1 hour and 20 minutes Number of Problems: 3

Important Notes:

Be sure to read all the problems carefully and answer all questions.

• Be sure to answer all parts of each question.

• Submit only one answer for each question. Multiple solutions for one question will NOT be graded.

• Clearly show all the steps of your work.

• Answers without detailed explanations will NOT be graded.

• The Engineering School Honor Code applies.

Problem 1 (30 points)

Implement the following function using only 2-to-1 multiplexers and NOT gates:

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$$f=\overline{w}_2w_3+\overline{w}_1w_2\overline{w}_3+w_2\overline{w}_3w_4+w_1\overline{w}_2\overline{w}_4$$

Note: AND, NAND, OR, NOR, XOR gates are not available.

Problem 2 (35 points)

For the logic function $f(w,x,y,z)=\prod M(1,7,12,13,14,15)\cdot d(0,2,8,10)$ (Note: the *d* represents the don't cares):

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a) Show the truth table. [5 points]

b) Draw a completely labeled K-map. [5 points]

- c) Write the algebraic expression for the minimized Sum of Products (SoP) and minimized Product of Sum (PoS) implementation of this function using the K-map. **Note:** Show the circles on the K-map. [10 points]
- d) Write a Verilog program using structural code that implements the SoP. [5 points]

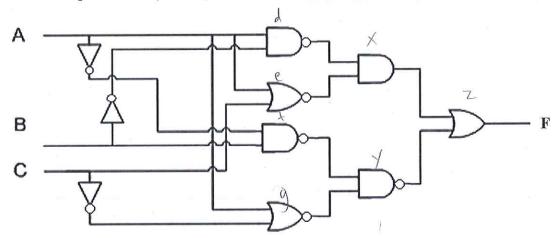
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Problem 3 (35 points)

Simplify the following circuit by using Boolean Algebra properties. Assume that you have **only** 2-input and 3-input NAND gates. It is known that $\overline{x+y+z} = \overline{x} \cdot \overline{y} \cdot \overline{z}$. Draw the simplified circuit.

Note: NOT, AND, OR, NOR, XOR gates are not available.

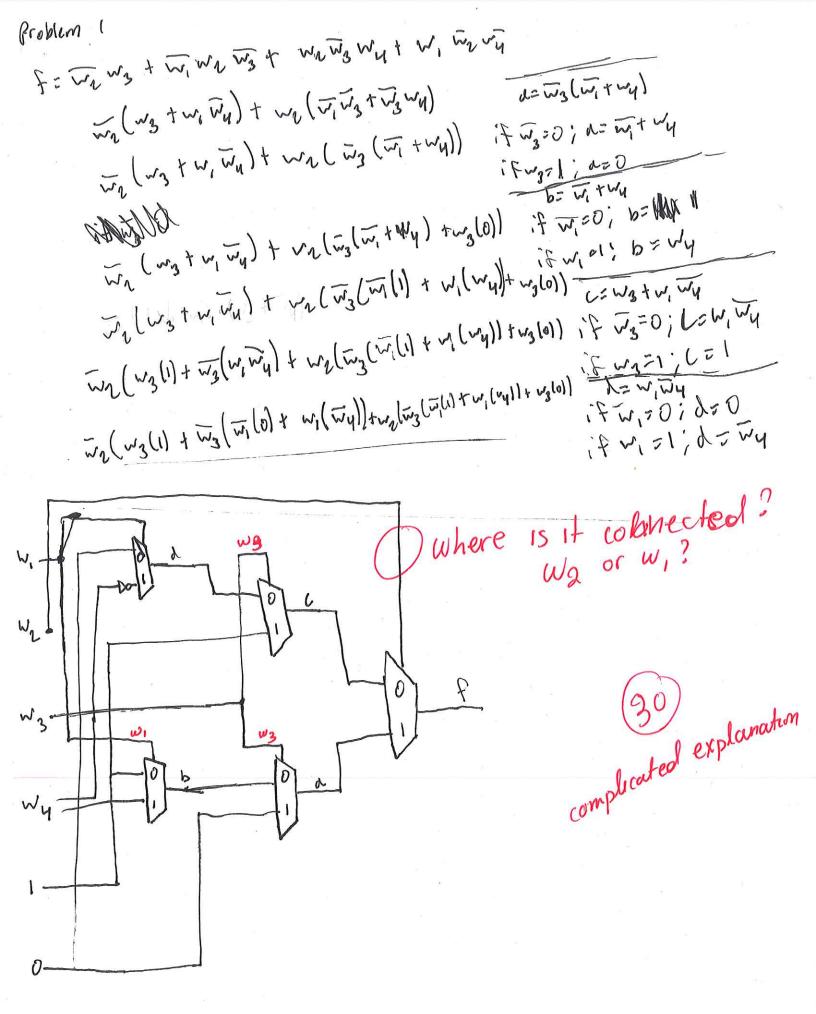
Note: Simplification by K-maps will NOT be graded.



Boolean Algebra Properties

17b. $(x+y) \cdot (y+z) \cdot (\overline{x}+z) = (x+y) \cdot (\overline{x}+z)$

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. Problem 2

$$f(w, x, y, z) = \prod M(1, 7, 12, 13, 14, 15)$$

 $\circ d(0, 2, 8, 10)$

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Problem 2 " i

POS:
$$f = \overline{w \cdot x \cdot y} + x \cdot y \cdot z + \overline{w} \cdot x$$

$$= (w + x + y) \cdot (\overline{x} + \overline{y} + \overline{z}) \cdot (\overline{w} + \overline{x})$$
(5)

@ p.xa + E.W + W.Z + X.W . 7 - 1 - 5

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 $(x + y + z) \cdot (x + y + z) \cdot (y + x + y)$

SOP structural Verilog: module problem 2d (w, x, y, Z, f); input w, x, y, z; output f; not (a, w); // a= W not (b, x); 1/ b= X not (c, y); 11 6= 4 // d= 2 not (d, z); and (h, w, b); and (i, b, y); and (j, a, d); and (k, a, x, c); 410) or (f, h, i, j, k);

endmodule

i er y

Problem 3:

$$F = (AB \cdot A+C) + \overline{AB \cdot A+C}$$

$$= \overline{AB + (A+C)} + \overline{AB + A+C}$$

$$= \overline{AB + (A+C)} + \overline{AB + A+C}$$

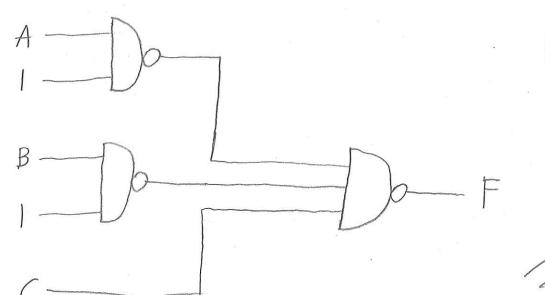
$$= \overline{AB + A+C} + \overline$$

(2) = - 0

Continued for Problem 3:

Reverse Enable Property:

Simplified Circuit:





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