Applications of the MOSFET in analog systems

Noble Huang (Mulia Widjaja)
Harrison Shaw
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Lab 7
ELEN 115L Wed 2:15 PM

Objective:

In this lab we will study the MOSFET as a switch in sample and hold systems. We will also be studying MOS inverting amplifiers.

Procedure:

Complete each section of the lab. For each section show:

- Show circuit schematics of each circuit you construct on LTSpice.
- Show screenshots of all plots and waveforms.
- Answer all the questions posed in the handout.

Part 1: MOSFET as a Switch

Part A: NMOS Switch

a-e). See circuit below. On our circuit we left the capacitor at 1nF per the description in the image rather than 10nF.

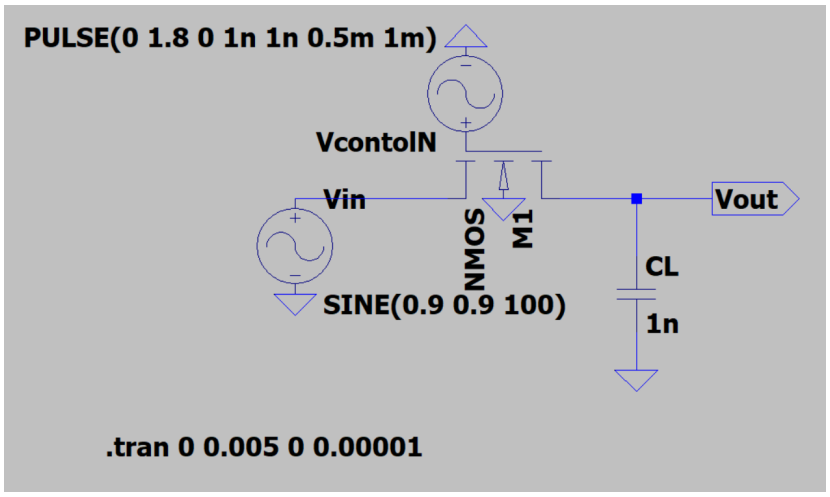


Figure 1: NMOS Switch Circuit in LTSpice

f). Output Screenshot from transient analysis:

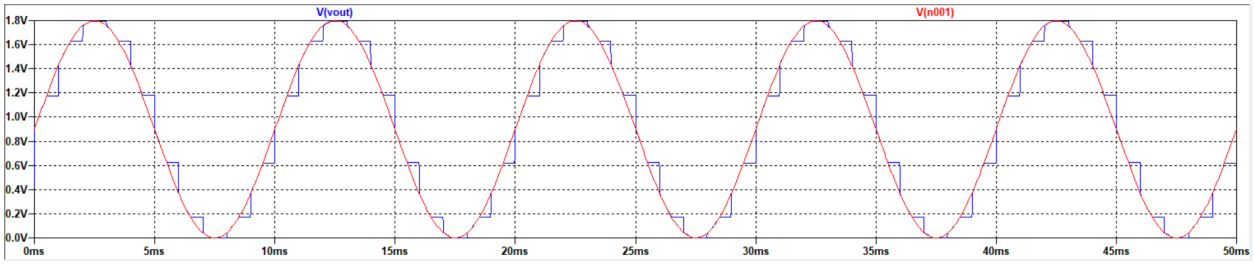


Figure 2: Vin and Vout for transient input

g). This graph looks like this because when the voltage goes up to 1.8V the switch turns on and the Vout steps up until it reaches 1.8V. When the input voltage reuters back down to 0V the Vout value follows in steps.

Part B: PMOS Switch

a-e). See circuit below. On our circuit we left the capacitor at 1nF per the description in the image rather than 10nF.

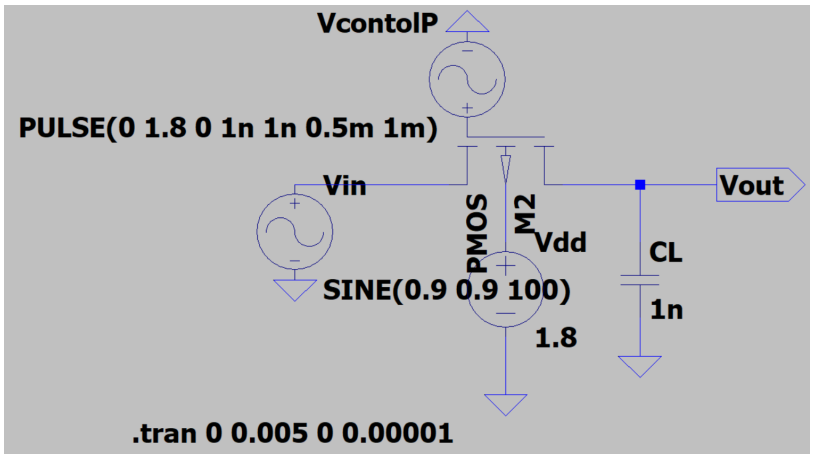


Figure 3: PMOS Switch Circuit in LTSpice

f). Output Screenshot from transient analysis:

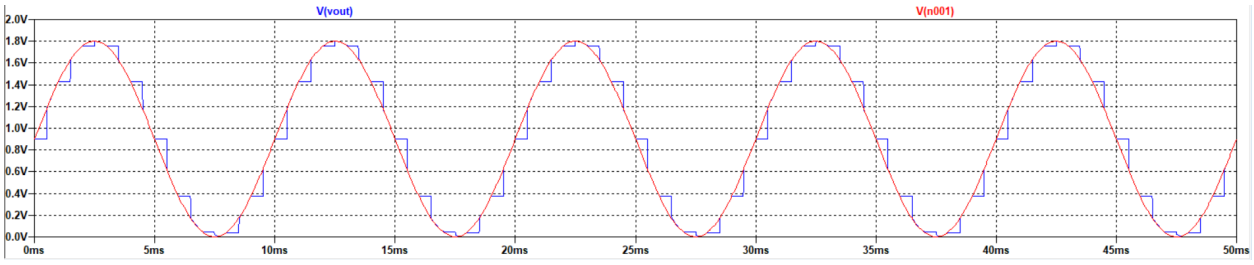


Figure 4: Vin and Vout for transient input

g). The graph looks like this because when the voltage goes up to 1.8V the switch turns on and the Vout steps up until it reaches 1.8V. When the input voltage reuters back down to 0V the Vout value follows in steps. In the PMOS configuration the steps occur at the opposite times as with the NMOS configuration.

Part C: Transmission Gate

a). See circuit below. Gate inputs are offset to provide an output.

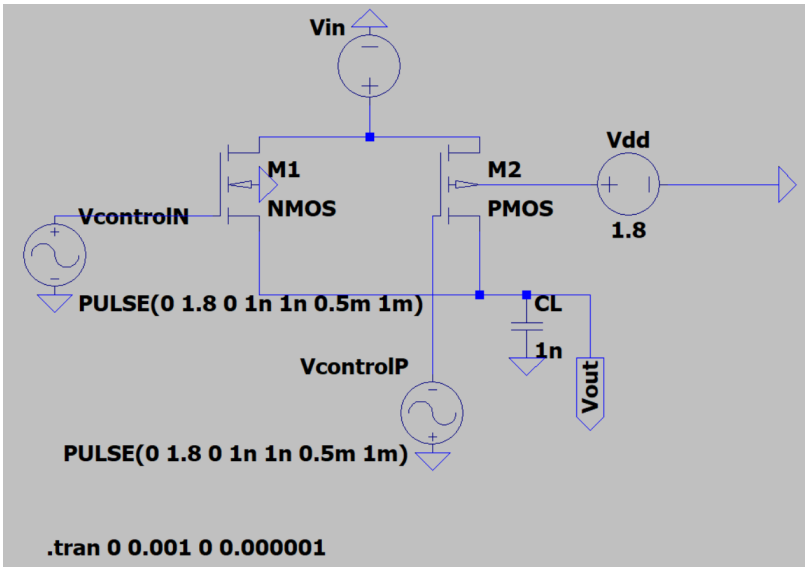


Figure 5: NMOS and PMOS connected in parallel

b). Output Screenshot from transient analysis:

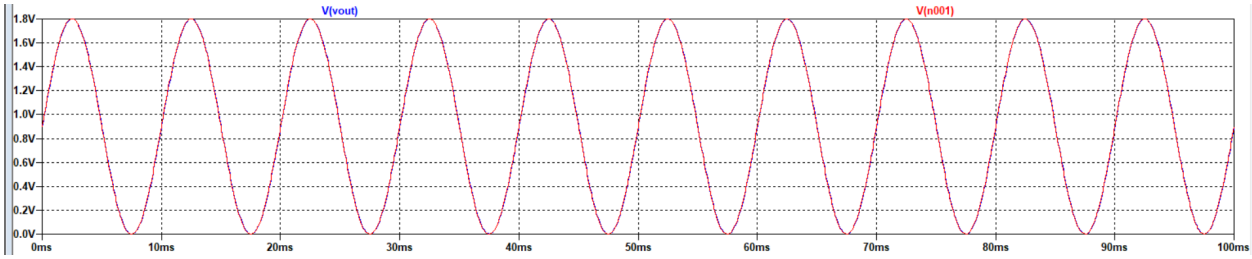


Figure 6: Vin and Vout for transient input

c). This graph looks

<u>Part 2: MOS inverting amplifier</u>

a-c). See circuit below. We have added the parameters for the values given in the Prelab using the command pictured below.

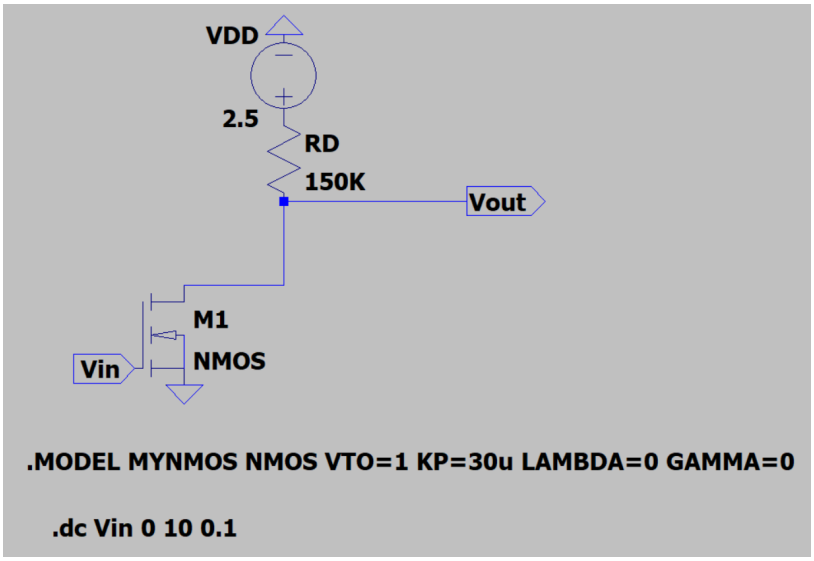


Figure 7: MOS Inverting Amplifier

d). The Voltage Transfer Curve is pictured below with Vout vs Vin.

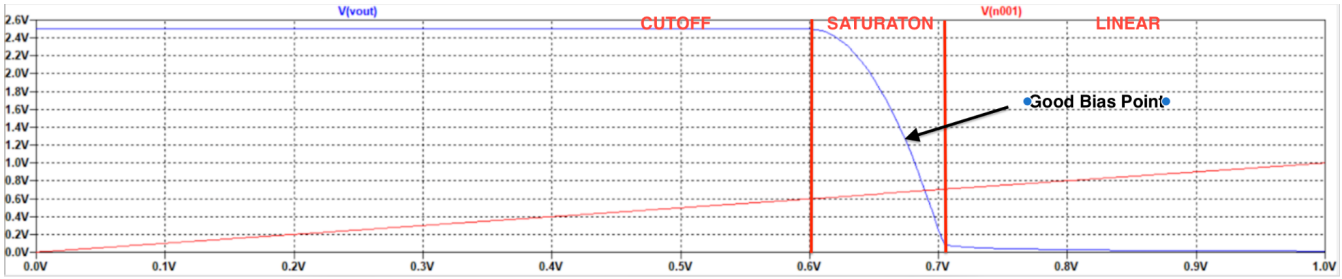


Figure 8: Vout vs Vin for the MOS inverting amplifier.

e). MOS as an analog amplifier

a. *On your plot indicate for what portion the MOS transfer curve is linear.*
The Linear part is when the Vin is greater than 0.7 V.

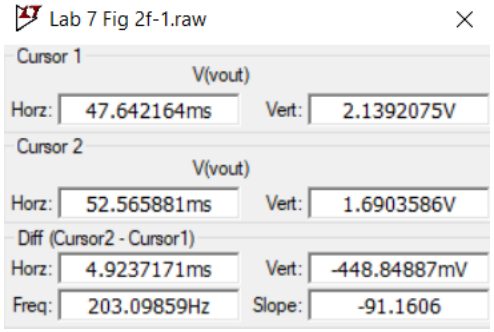
b. *Indicate what would be an optimal BIAS point for use of this circuit as an analog amplifier.*
Optimal BIAS point: Point Anywhere within Saturation Region. See above.
It would be when Vin = 0.65V and Vout = 1.4V.

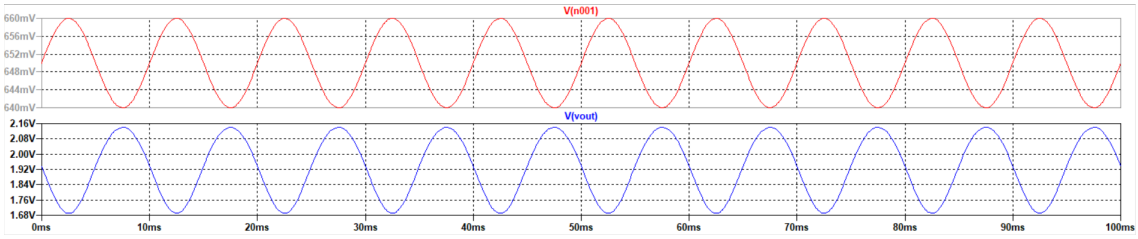
c. *What is the gain at this point? Hint: Find the slope.*
Slope in saturation region is -22.45

d. *What is the input signal that can be given to satisfy the small signal approximation?*
Answer: **0.1 V**

e. *Give an input to this amplifier with the DC bias from (b) and signal input from (d).*
Done, see below.

f. Run a transient analysis with the input you obtain from e and observe the output signal. Note the DC and signal values.



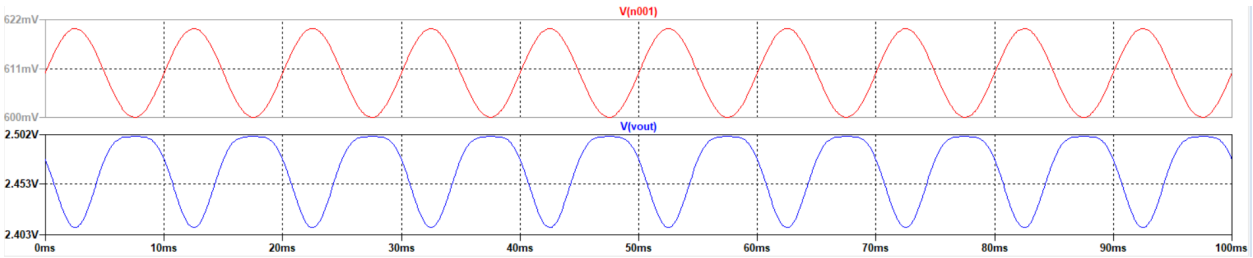


f). MOS as a Logic Inverter

a. *Mark the portions of the curve that help you use the device as an inverter.*

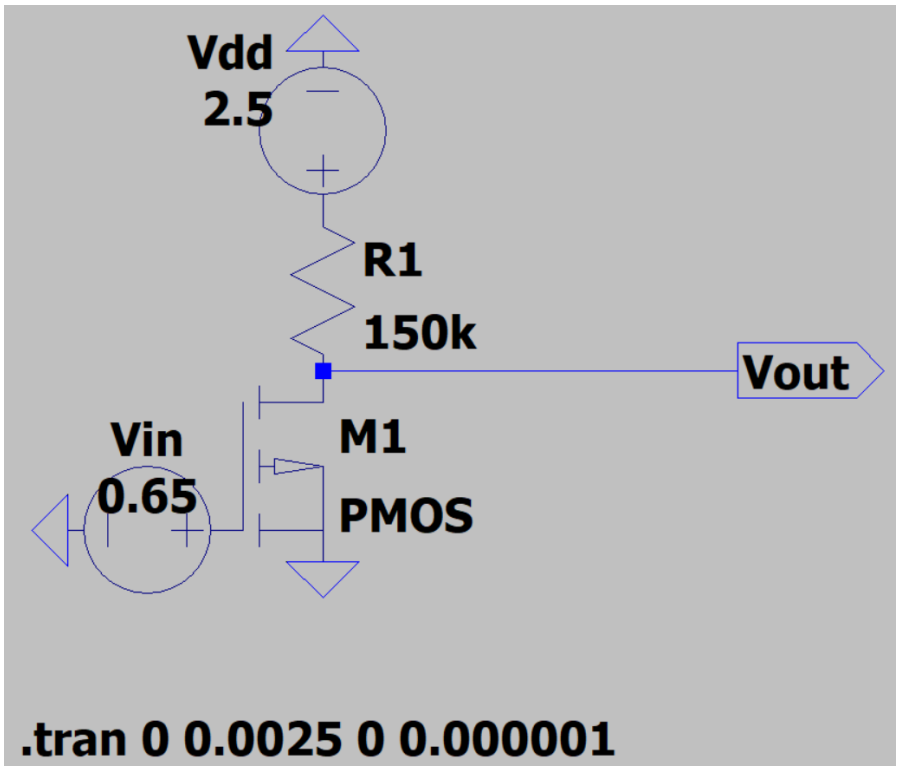
The device functions as an inverter when in the middle of the curve in the saturation mode as seen in the curve shown above.

b. *Run a transient analysis giving a pulse signal as logic input to this inverter and see the logic output. What do you observe for the high and low values at the output?*



Low end of input where vin = 0.61. The output curve begins to exhibit a non-symmetrical pattern as the tops of the wave flatten out.

c. *Find the current drawn from Vdd. Observe the values during the flat portions of the pulse and during the transitions from low to high and high to low. What do you observe for power consumed?*



d. *Increase RD to 500 KΩ and rerun part (c). What do you observe? What can you comment on the ideal load value for a perfect inverter.*