SANTA CLARA UNIVERSITY	ELEN 115 Spring 2023	Shoba Krishnan

Laboratory #5: Diode Rectifiers

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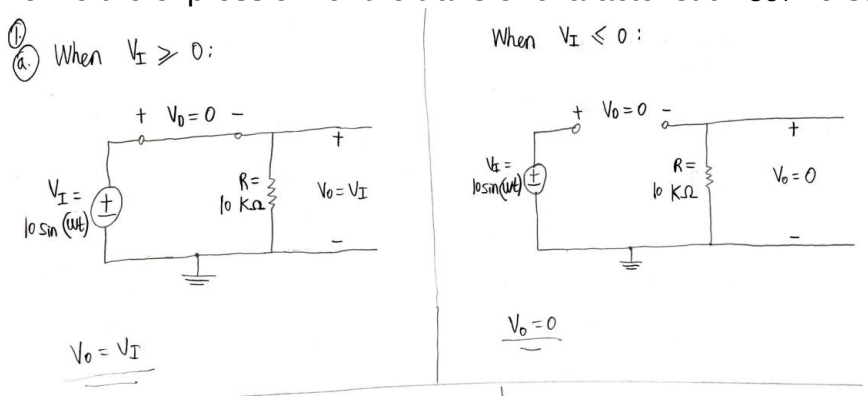
PRE-LAB

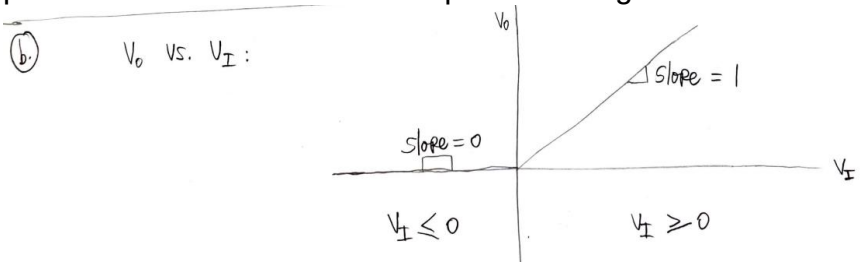
1. For the diode circuit shown in Figure 1, consider the diode to be ideal. The input voltage v_I given to the circuit is a sinusoid with a peak value of 10V.

   For the circuit

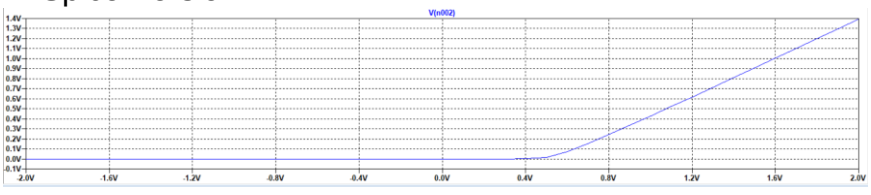
   (a) Derive the expression for the transfer characteristic v_{OUT} versus v_I for the circuit.



   (b) Plot the transfer characteristic v_{OUT} versus v_I indicating the values of all significant points and the values of the slopes of all segments.

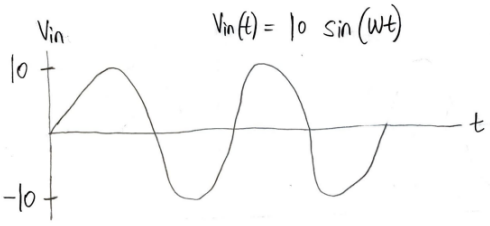


   LTSpice Version:



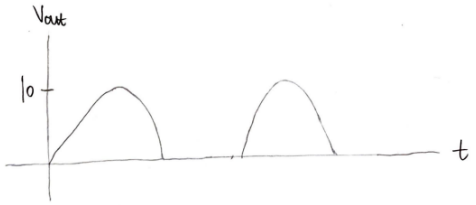
   (c) Draw the corresponding output voltage v_{OUT} vs. time for two cycles of the the input v_I

(c)



If $V_{in} \leq 0$: then $V_{out} = 0$ → Effect on $V_{out}(t)$: V_{out}: Clipped at 0 V_1 instead of going all the way down to -10 V

$V_{out} = 10 \sin(\omega t)\ ?\ V_{in} \geq 0\ :\ 0$ (Ternary operator)



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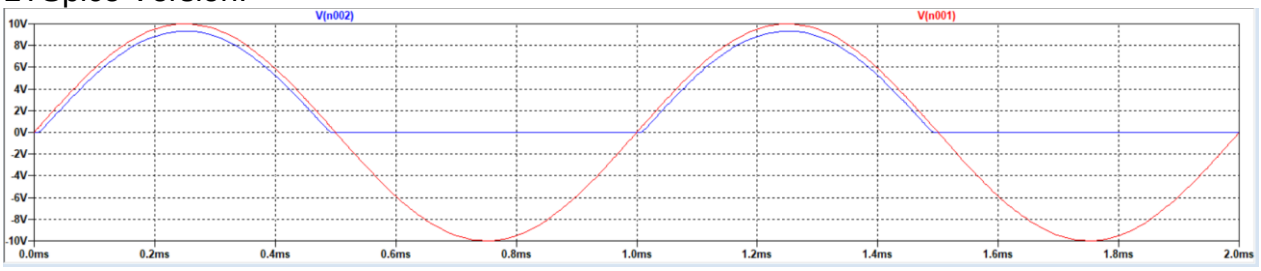
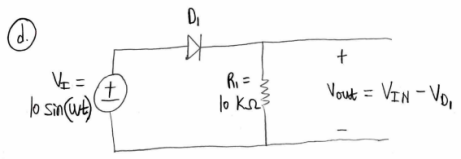


(d) Find the peak diode current.



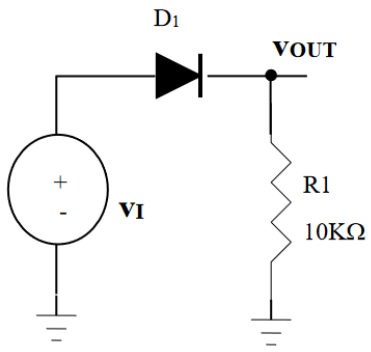
Peak Diode current $= \frac{V_{IN} - V_{D1}}{R_1}$ → "peak": Must use Vin at peak

$= \frac{10 - V_{D1}}{10000}$ (*)

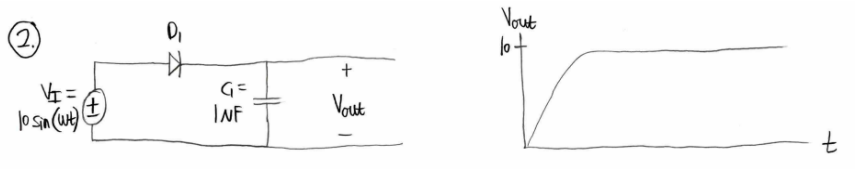
(*): V_{D1} appears to be unknown

(e) Find the maximum reverse voltage seen by the diode.

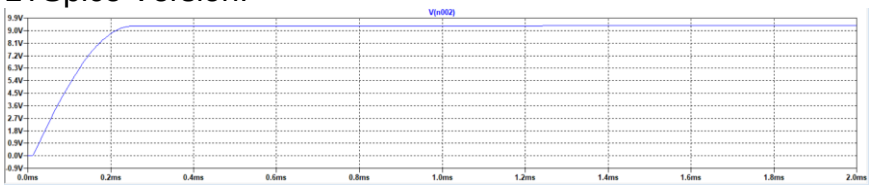
Figure 1



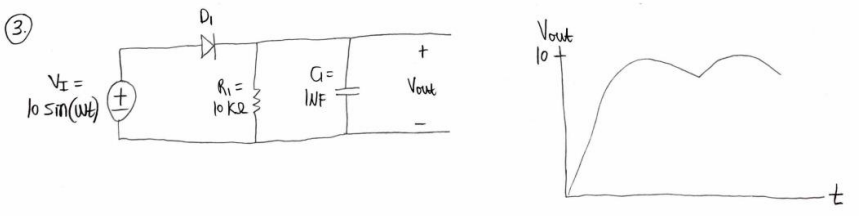
2. If a capacitor is connected **instead of** the resistor R1 in Figure 1, draw the corresponding output voltage v_{OUT} vs. time for two cycles of the the input v_I.



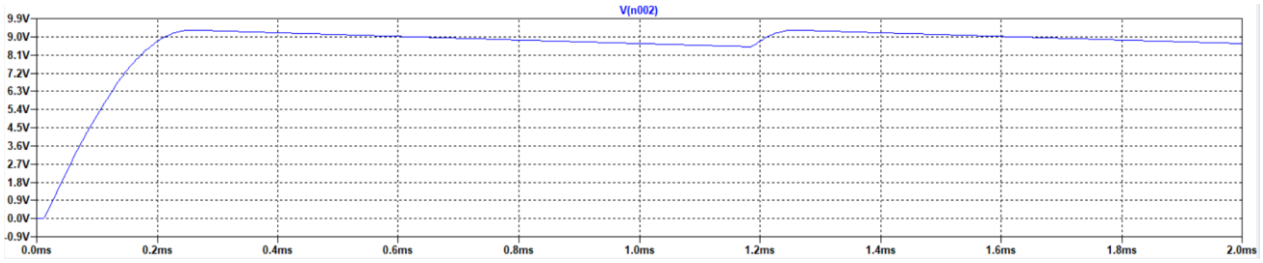
LTSpice Version:



3. If a capacitor is connected **in parallel with** the resistor R1 in Figure 1, draw the corresponding output voltage v_{OUT} vs. time for two cycles of the the input v_I.



LTSpice Version:


V(n002)
9.9V
9.0V
8.1V
7.2V
6.3V
5.4V
4.5V
3.6V
2.7V
1.8V
0.9V
0.0V
-0.9V
0.0ms
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
1.2ms
1.4ms
1.6ms
1.8ms
2.0ms