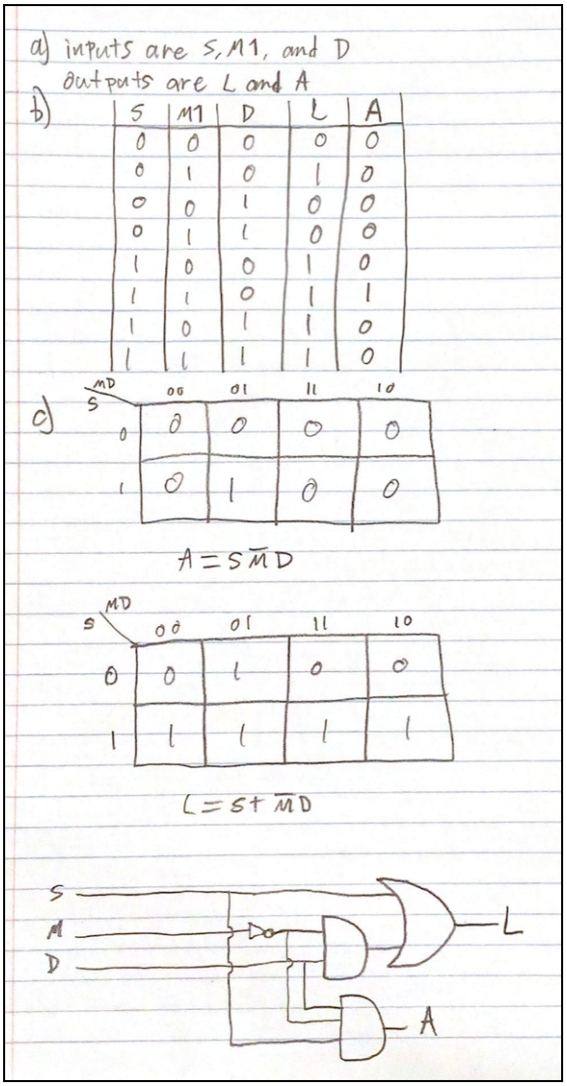
Introduction

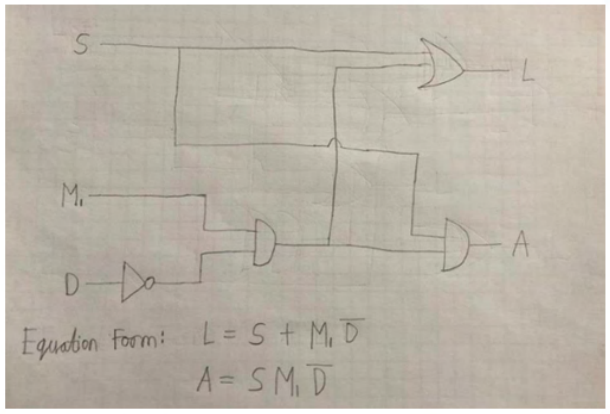
In this lab, we designed a controller to meet the requirements of the provided problem statement. Like in Lab 1, it controlled a light with a switch and motion activation, as well as an alarm. It also included a disable switch to turn off the motion activation. After being designed in a schematic in the pre-lab, it was implemented through the Altera Quartus II design program, to then be tested on an FPGA. Two versions of pre-labs can be seen below.



Inputs: S, M1, D
Outputs: L, A

Pre-Lab 2

S	M1	D	L	A
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	1
1	1	1	1	0



Describe the procedures your group took to complete the construction and testing of your motion sensor circuits:

For this lab, we utilized a device referred to as the Altera (Intel) Cyclone IV FPGA. In order for a program to be executed, we created a schematic in a software program called Quartus II. We implemented many steps in order to achieve and ensure success in using Quartus II. As per following are the steps:

1. Set up a license by editing the environment variables.

2. Create new values to store the license files. We checked if the license is inserted into the program. Since we observed that the Mentor® Questa® window appears, we are determined to start the program.

3. Create a new project and put it in the appropriate directory. This is our first project so that we were not necessitated to add additional files. The project must match the FPGA device that we were handling, which was EP4CE115F29C7 in the Project Wizard.

4. Add a Schematic File under Design Files. After this one, we dragged all the appropriate logic gates and pins onto the circuit schematic.

5. Save our schematics inside **Lab 2** folder.

6. Use the .qsf file and renamed it Lab2.qsf

7. Put the .qsf file inside my lab folder.

8. Assign the respective LED accordingly with the program. (I put them in order)

9. Import pin assignments from the qsf file.

10. Compile design and clicked play icon via a logic gate with a green color

11. Construct **University program VWF**

12. Encounter the **Node Finder** button

13. Click on List button

14. Saved VWF file named Waveform.vwf

15. Came upon Run -> Functional Simulation which Placed generated files in **simulation/qsim**

16. **Simulation** under **EDA Tool Settings**

17. Select "**Questa Intel FPGA**"

18. Make "**simulation/qsim**" for **Output Directory** of **EDA Netlist Writer settings**

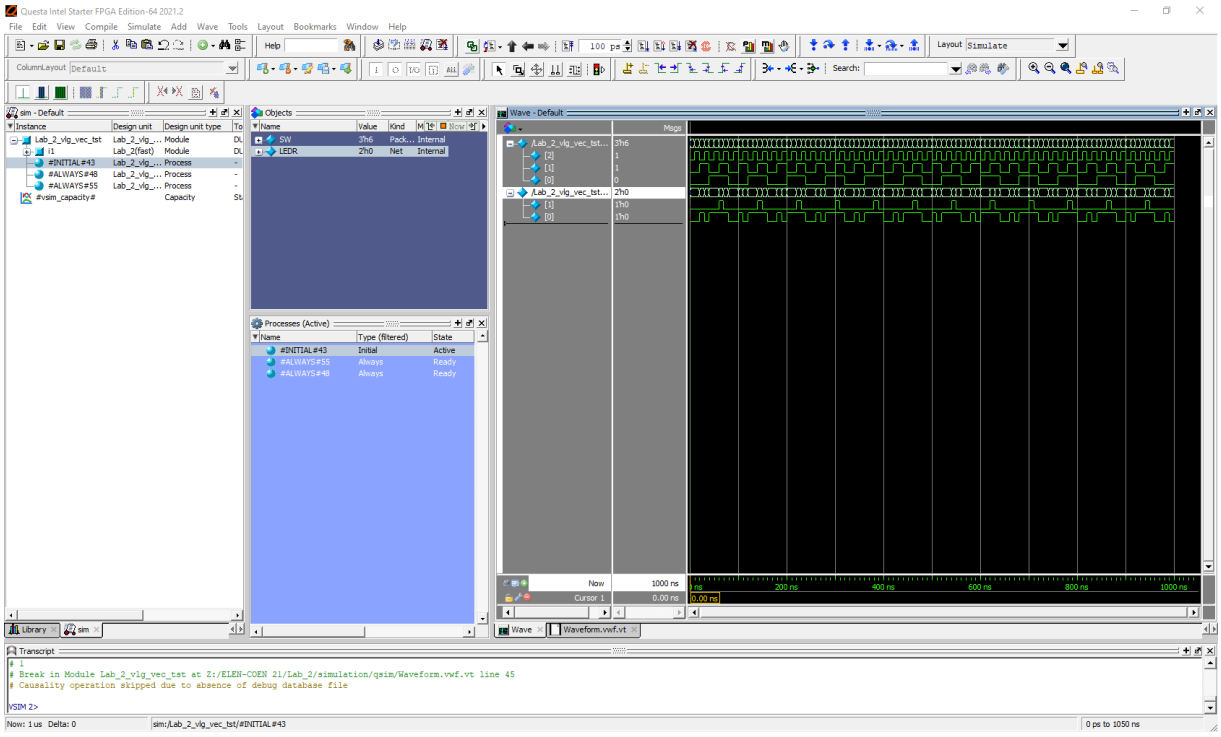
19. Provide the **Compile Test Bench** with check mark to click the **Test Benches**

20. Undergo the configure test bench setting

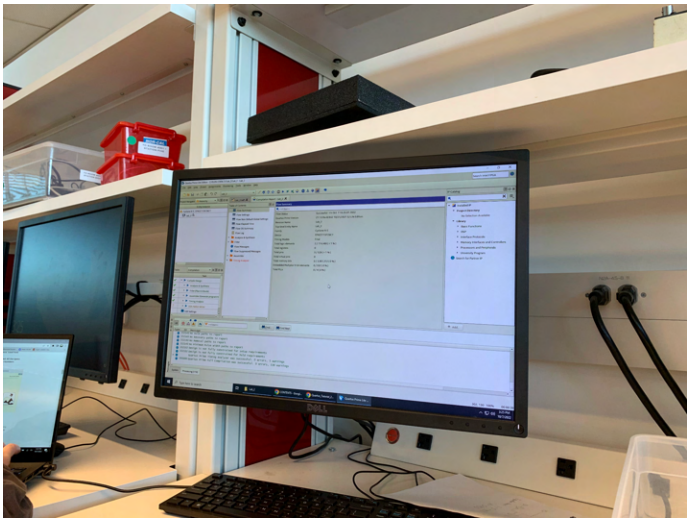
21. Make a new Test Bench called Lab_test_vlg_vec_tst.

22. Put "C:/Apps/intelFPGA_lite/21.1/questa_fse/win64" in the Directory Path for the Both the **Questa Sim** and **Questa Intel** FPGA EDA Tool.

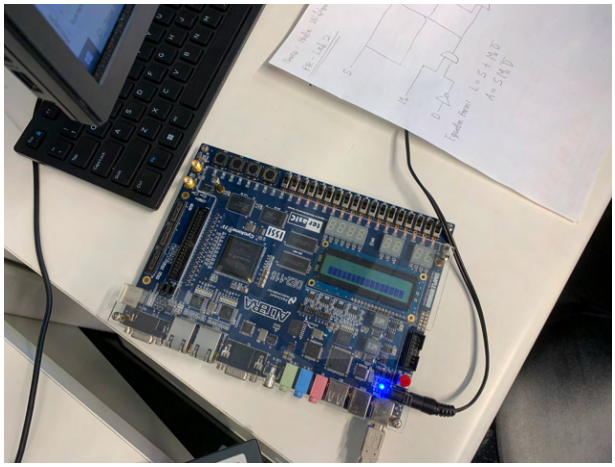
23. Run the **Simulation Tool**. Below is the simulation results:



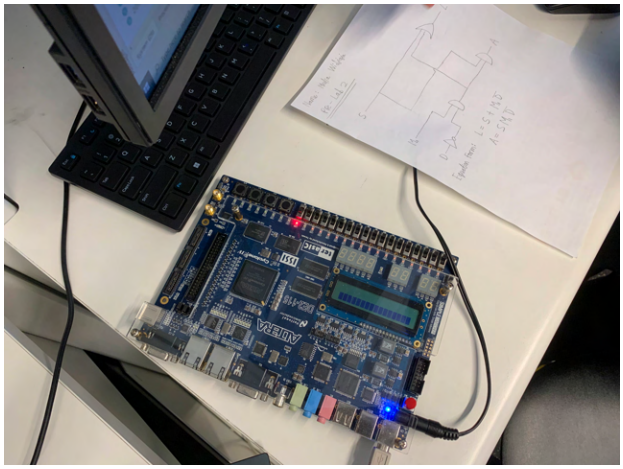
24. Finally, we uploaded the program to the Altera (Intel) Cyclone IV FPGA. Proof of successful download to FPGA:



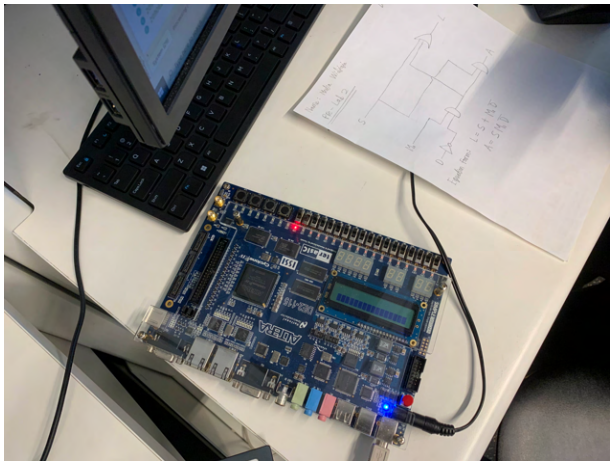
Case 1: Where manual switch (S) is off, and no motion (M) is detected



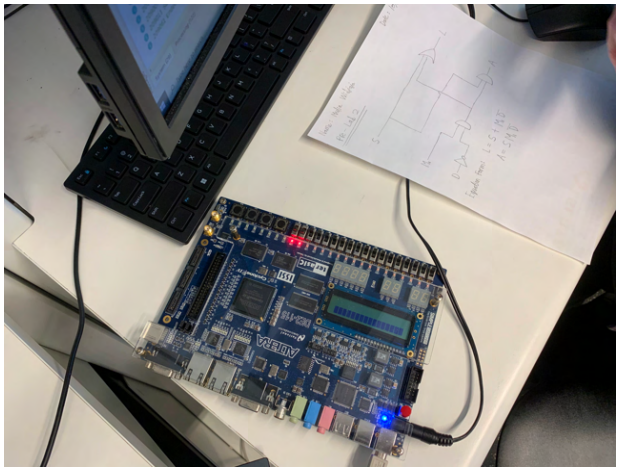
Case 2: Where manual switch (S) is on, and no motion (M) is detected



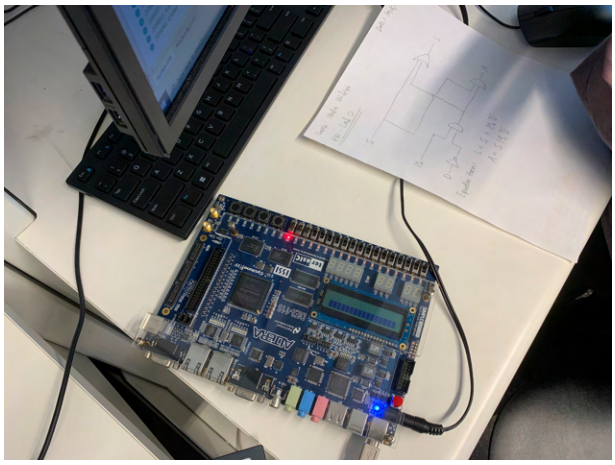
Case 3: Where manual switch (S) is off, and a motion (M) is detected



Case 4: Where manual switch (S) is on, and a motion (M) is detected



Case 5: Where manual switch (S) is on, and a motion (M) is detected, but the Disable Switch is on



1. **In Laboratory 1, what would you have had to change to use three motion detectors such that any of three different motion detectors could turn on the light and could also turn on the buzzer if the light were already on because the manual switch S was on? Specifically consider the component changes or additions, the wiring changes, and the testing.**
   An extra OR gate would have been added for the multiple motion detectors. The wiring would be the three motion detectors being the inputs of the OR gate and its output being wired identically to the single motion detector in lab 1.

2. **Compare that to the changes you would need to make for the Altera FPGA implementation of a logic circuit using three motion detector inputs.**

   An extra OR gate would have been added for many motions in the FPGA implementation software program. There would perhaps be more complexity for the time diagram, since there would be more inputs than the original one.