Group Number: Group 9: Shiyu Ye

NAMES (FIRST AND LAST NAME): Mulia Widjaja (Noble)
Venus Li

In-Class Assignment 3

ELEN 21/COEN 21 – Fall 2022
Instructor: Maria Kyrarini
Date: 11/15/2022
Time: 1 hour and 30 minutes
Number of pages: 3

Important Notes:

- Be sure to read all the problems carefully and answer all questions.
- Be sure to answer all parts of each question.
- **Submit only one answer for each question.**
- Multiple solutions for one question will not be graded.
- **Clearly show all the steps of your work.**
- **Answers without explanation will not be graded.**
- The Engineering School Honor Code applies.

$26 + 25 + 30 + 4 = 85$

Problem 1 (30 points)

Design a counter using positive edge D flip-flops that will count as follows:

- when X=0 and Y=0, the counter runs through the following states: 3,2,1,0,3,2,...
- when X=0 and Y=1, the counter runs through the following states: 0,1,2,3,0,1,...
- when X=1 and Y=d, the counter runs through the following states: 0,2,0,2,...

Draw a simplified circuit with a minimum number of flip-flops and a minimum network of AND, OR, NOT, and XOR gates.

Note: You can use the following Boolean Expression without proving it:

- $\overline{x \oplus y} = \bar{x} \cdot \bar{y} + x \cdot y$

Problem 2 (30 points)

A Moore state machine has an input w and an output z. The machine is a sequence detector that produces z = 1 when it detects 01; otherwise z = 0.

a) Draw the state diagram and provide the state-assigned table with the one-hot encoding approach. [10 points]
b) Derive a simplified circuit from the state-assigned table using JK flip-flops. **Note:** Do not draw the simplified circuit but describe it with equations. [20 points]

Problem 3 (30 points)

A Moore state machine has an input w and two outputs z1, z2. The machine is a sequence detector that produces z1 = 1 (z2 = 0) when it detects 111 and z2=1 (z1=0) when it detects 101; otherwise z1, z2 = 0.

a) Draw the state diagram. [20 points]
b) Provide the state table and the minimum state-assigned table. [10 points]

Problem 4 (10 points)

A universal shift register can shift in both the left-to-right and right-to-left directions, can hold values and it has parallel-load capability. Draw a circuit for such a 2-bit universal shift register. **Note:** The problem will NOT be graded if explanation is missing.

Boolean Algebra Properties

5*a*.	$x \cdot 0 = 0$
5*b*.	$x + 1 = 1$
6*a*.	$x \cdot 1 = x$
6*b*.	$x + 0 = x$
7*a*.	$x \cdot x = x$
7*b*.	$x + x = x$
8*a*.	$x \cdot \overline{x} = 0$
8*b*.	$x + \overline{x} = 1$
9.	$\overline{\overline{x}} = x$

10*a*.	$x \cdot y = y \cdot x$	*Commutative*
10*b*.	$x + y = y + x$	
11*a*.	$x \cdot (y \cdot z) = (x \cdot y) \cdot z$	*Associative*
11*b*.	$x + (y + z) = (x + y) + z$	
12*a*.	$x \cdot (y + z) = x \cdot y + x \cdot z$	*Distributive*
12*b*.	$x + y \cdot z = (x + y) \cdot (x + z)$	
13*a*.	$x + x \cdot y = x$	*Absorption*
13*b*.	$x \cdot (x + y) = x$	
14*a*.	$x \cdot y + x \cdot \overline{y} = x$	*Combining*
14*b*.	$(x + y) \cdot (x + \overline{y}) = x$	
15*a*.	$\overline{x \cdot y} = \overline{x} + \overline{y}$	*DeMorgan's theorem*
15*b*.	$\overline{x + y} = \overline{x} \cdot \overline{y}$	
16*a*.	$x + \overline{x} \cdot y = x + y$	
16*b*.	$x \cdot (\overline{x} + y) = x \cdot y$	
17*a*.	$x \cdot y + y \cdot z + \overline{x} \cdot z = x \cdot y + \overline{x} \cdot z$	*Consensus*
17*b*.	$(x + y) \cdot (y + z) \cdot (\overline{x} + z) = (x + y) \cdot (\overline{x} + z)$	

① Present Next

X	Y	n_1 $Q_1(t)$	n_2 $Q_2(t)$	n_1 $Q_1(t+1)$	n_2 $Q_2(t+1)$
0	0	0	0	1	1
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	0	1	d	d
1	0	1	0	0	0
1	0	1	1	d	d
1	1	0	0	1	0
1	1	0	1	d	d
1	1	1	0	0	0
1	1	1	1	d	d

Y = d

y = d

0 = 00

1 = 01

2 = 10

3 = 11

I never write the same symbol for current and next states!

3, 2, 1, 0, 3 . . .

0, 1, 2, 3, 0 . . . .

You have to mention that next state is equal to ff input $D(t) = Q(t+1)$

0, 2, 0, 2

26

we need eq. for the ff inputs!

$n_1 n_2$ \ XY	00	01	11	10
00	1	0	1	1
01	0	1	d	d
11	1	0	d	d
10	0	1	0	0

?

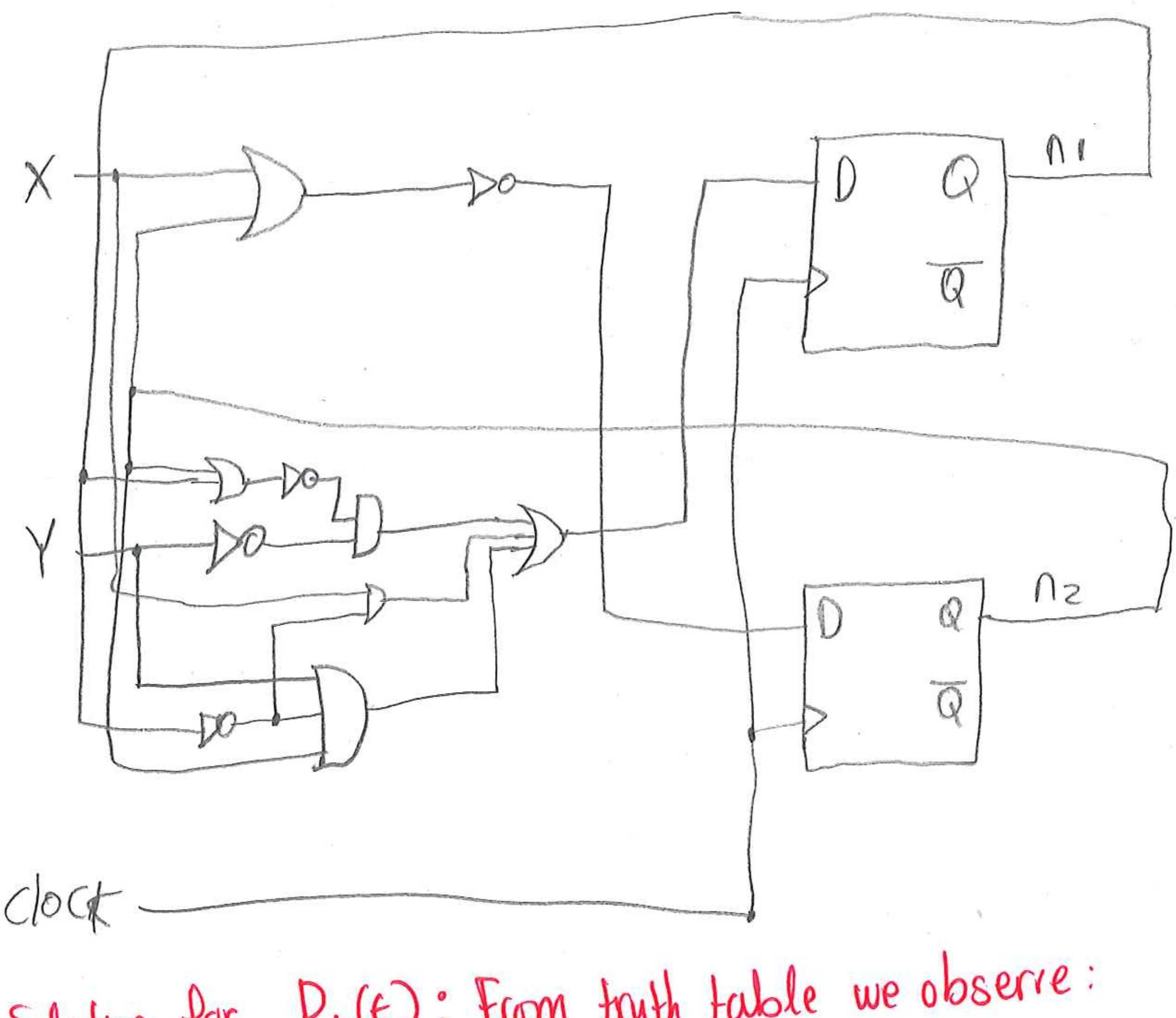
$$n_1 \text{(next)} = \overline{n_1} \cdot \overline{n_2} \cdot \overline{Y} + Y \cdot \overline{n_1} \cdot n_2 + \overline{n_1} \cdot X + n_1 \cdot n_2 \cdot \overline{Y}$$

$$= \overline{Y}\left(\overline{n_1 \oplus n_2}\right) + Y \overline{n_1} n_2 + \overline{n_1} X$$

$n_2(t+1)$:

$n_1 n_2$ \ XY	00	01	11	10
00	1	1	0	0
01	0	0	d	d
11	0	0	d	d
10	1	1	0	0

$$n_2(t+1) = \overline{n_2}\ \overline{X} = \overline{n_2 + X} = D_2(t)$$



Solution for $D_1(t)$: From truth table we observe:

For $x=0$: $y=0$: $D_1(t) = \overline{Q_1(t) \oplus Q_2(t)}$

$y=1$: $D_1(t) = Q_1(t) \oplus Q_2(t)$

For $x=1$: $D_1(t) = \overline{Q_1(t)}$

Therefore: $D_1(t) = \overline{x(t)}\left[\overline{y(t)}\left(\overline{Q_1(t) \oplus Q_2(t)}\right) + y(t)\cdot\left(Q_1(t) \oplus Q_2(t)\right)\right] + x \cdot \overline{Q_1(t)} =$

$= \overline{x(t)} \cdot \left(\overline{y(t) \oplus Q_1(t) \oplus Q_2(t)}\right) + x \cdot \overline{Q_1(t)}$

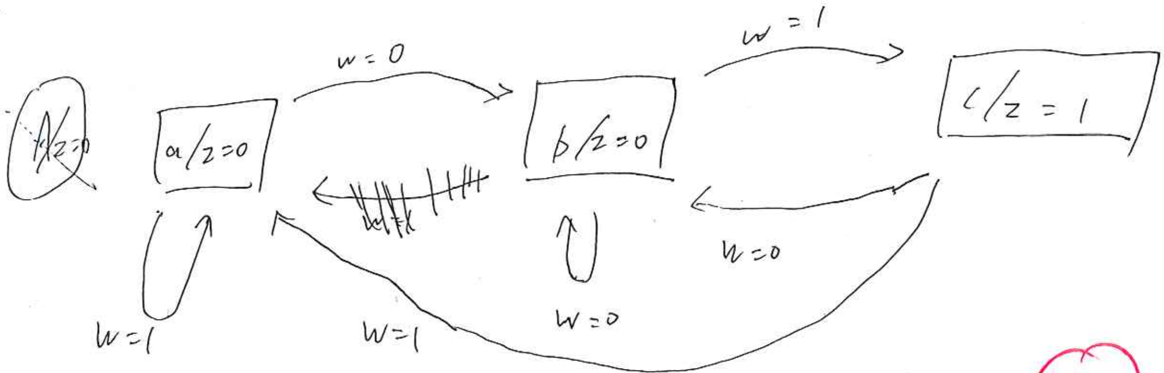
(2)

z = 1 , 01 , else , z = 0

(9.) state diagram state table one hot encoding

state nstate output

cstate



10

State Table:

Present States	Next States		Outputs
y	W=0	W=1	Z
A	B	A	0
B	B	C	0
C	B	A	1

A = 001

B = 010

C = 100

One hot Encoding

		pstate	nstates w=0	nstates w=1	output z
00	A	001	010	001	0
01	B	010	010	100	0
10	C	100	010	001	1

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

b

	present state		Next state		FF inputs				
w	Y_2	Y_1	y_2	y_1	J_2 ~~J_1~~	K_2 ~~K_1~~	J_1 ~~J_2~~	K_1 ~~K_2~~	Z
0	0	0	0	1	0	d	1	d	0
0	0	1	0	1	0	d	d	0	0
0	1	0	0	1	d	1	1	d	1
0	1	1	d	d	d	d	d	d	d
1	0	0	0	0	0	d	0	d	0
1	0	1	1	0	1	d	d	1	0
1	1	0	0	0	d	1	0	d	1
1	1	1	d	d	d	d	d	d	d

Q	Q(t+1)	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

You have to use the state assign table from a!

$J_2 = w \cdot Y_1$

Y_1 \ wY_2	00	01	11	10
0	0	d	d	0
1	0	d	d	1

$K_2 = 1$

Y_1 \ wY_2	00	01	11	10
0	d	1	1	d
1	d	d	d	d

$J_1 = \overline{w}$

Y_1 \ wY_2	00	01	11	10
0	1	1	0	0
1	d	d	d	d

$K_1 = w$

Y_1 \ wY_2	00	01	11	10
0	d	d	d	d
1	0	d	d	1

15

Z

Y_1 \ wY_2	00	01	11	10
0	0	1	1	0
1	0	d	d	0

$Z = Y_2$

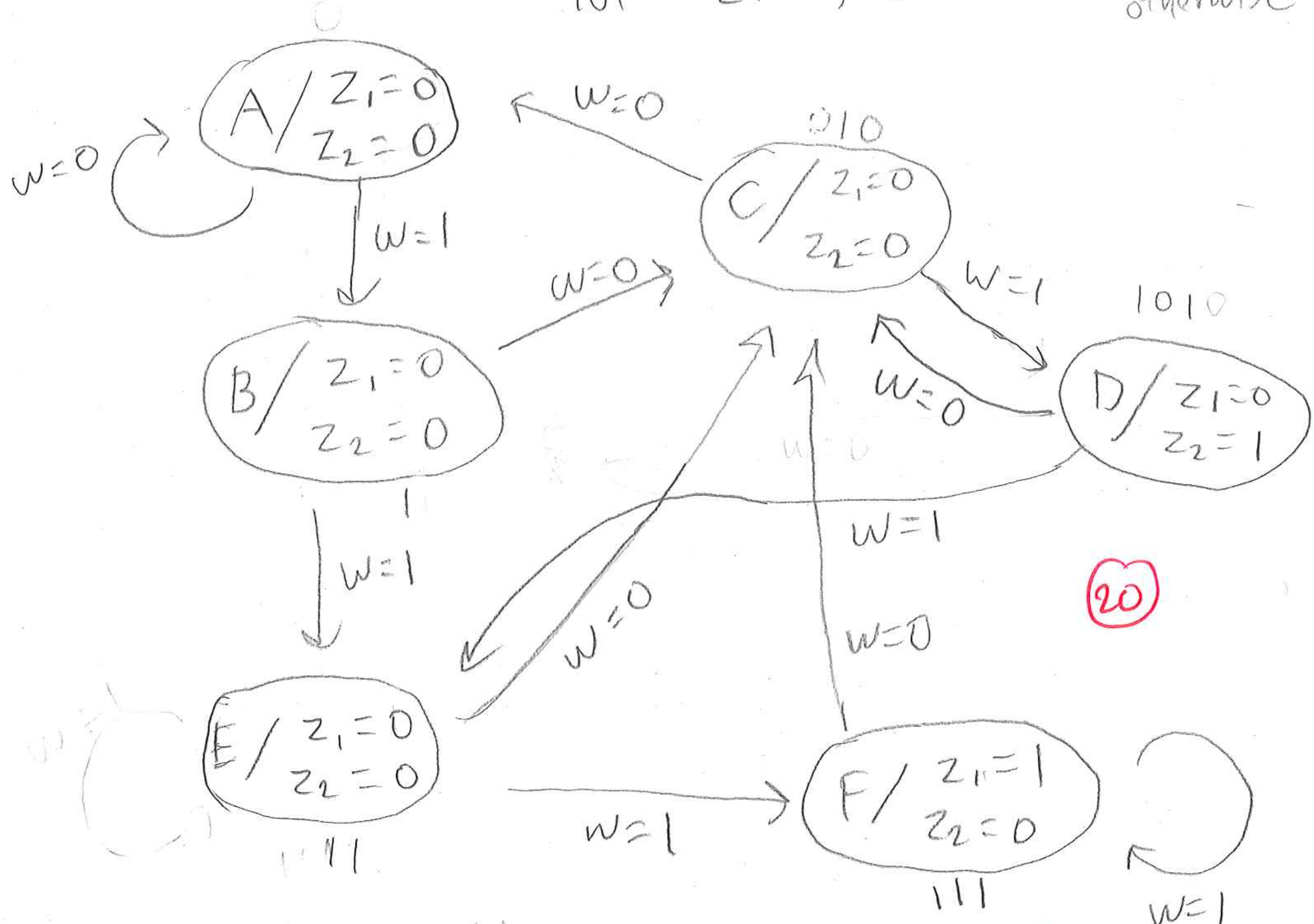
Problem 3

111 - Z1 = 1, Z2 = 0

101 - Z1 = 0, Z2 = 1

both 0 otherwise

a.



20

b. State table

Current State	Next state w=0	Next state w=1	Output Z_1	Output Z_2
A	A	B	0	0
B	C	E	0	0
C	A	D	0	0
D	C	E	0	1
E	C	F	0	0
F	C	F	1	0

Problem 3

b. Cont.

	Current state			Next state W=0			Next state W=1			Output	
	y_2	y_1	y_0	Y_2	Y_1	Y_0	Y_2	Y_1	Y_0	Z_1	Z_2
A	0	0	0	0	0	0	0	0	1	0	0
B	0	0	1	0	1	0	1	0	0	0	0
C	0	1	0	0	0	0	0	1	1	0	0
D	0	1	1	0	1	0	1	0	0	0	1
E	1	0	0	0	1	0	1	0	1	0	0
F	1	0	1	0	1	0	1	0	1	1	0
X	1	1	0	d	d	d	d	d	d	d	d
X	1	1	1	d	d	d	d	d	d	d	d

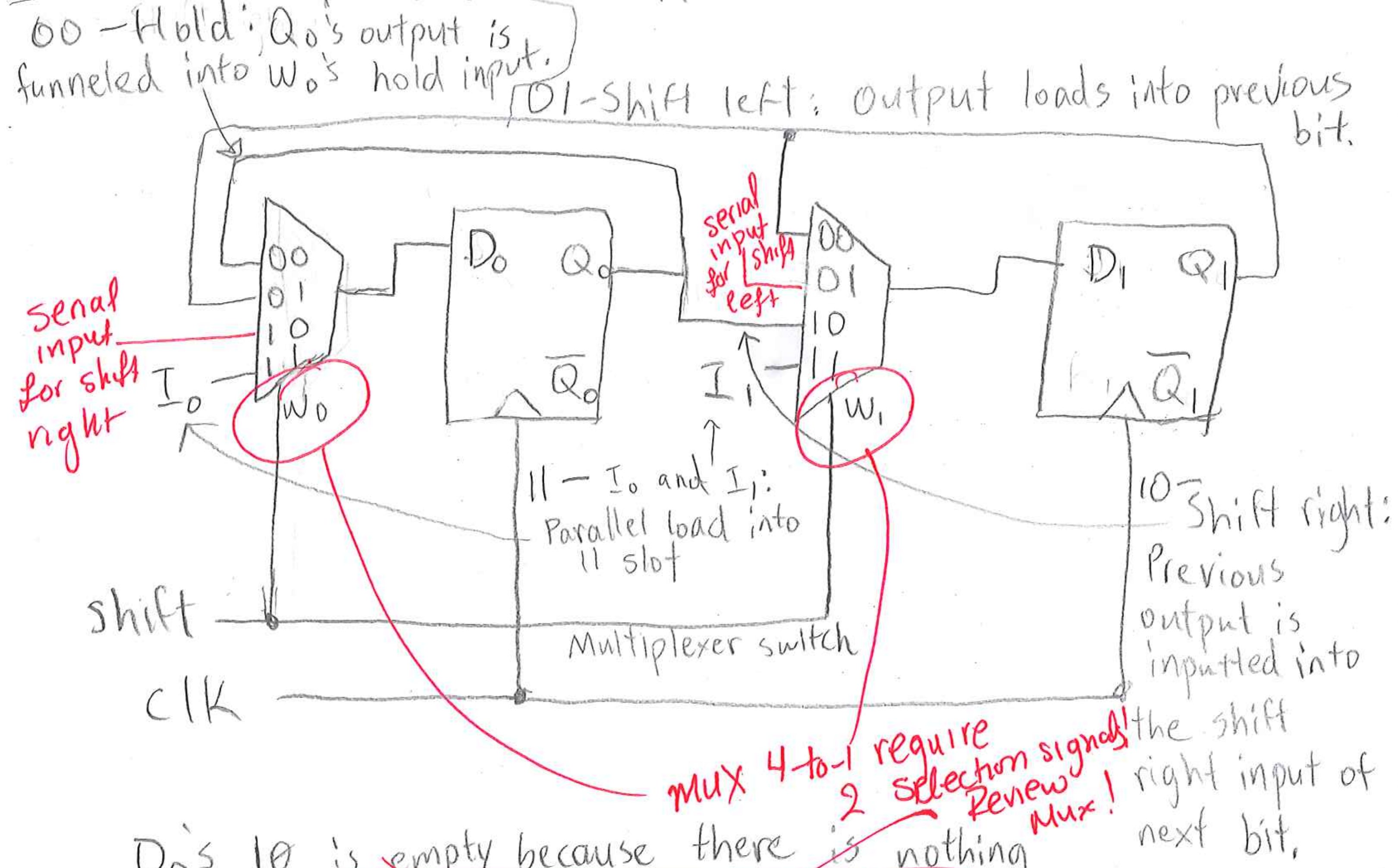
✓

10

Problem 4

- 2 bits
- Shift left 01
- Shift right 10
- hold 00
- Parallel load 11

W_1	W_0	Action
0	0	Hold
0	1	Shift left
1	0	Shift right
1	1	Parallel load



~~D_0's 10 is empty because there is nothing to "shift right" into its mux. D_1's 01 is also empty bc there is nothing on its right, to "shift left" from.~~

wrong!

4

PLEASE REVIEW MY HW SOLUTIONS AND HW FEEDBACK!