Homework 6

ELEN 21/COEN 21
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Lecture 9:

1. Look at the Verilog code below. What type of circuit does the code represent? Comment on whether or not the style of code used is a good choice for the circuit that it represents.

```
module problem4_18 (W, En, y0, y1, y2, y3);
   input [1:0] W;
   input En;
   output reg y0, y1, y2, y3;

   always @(W, En)
   begin
      y0 = 0;
      y1 = 0;
      y2 = 0;
      y3 = 0;
      if (En)
         if (W == 0)   y0 = 1;
         else if (W == 1)   y1 = 1;
         else if (W == 2)   y2 = 1;
         else   y3 = 1;
   end

endmodule
```

2. Write Verilog code for an 3-to-8 binary decoder.

Lecture 10:

3. Design a counter using JK positive edge flip-flops that will count as follows: 000, 100, 110, 011, 001, 000, 100, 110, …. Assume that all present states that do not belong to the requested sequence lead to state 000. Draw a simplified circuit.

4. Design a counter using JK negative edge flip-flops that will count as follows: 000, 001, 010, 011, 101, 000, 001, …. Draw a simplified circuit.

5. A state machine is defined by the state-assigned table shown below. Derive a circuit that realizes this state machine using a) D flip-flops and b) JK flip-flops.

Present state y_2y_1	Next state $w = 0$ Y_2Y_1	Next state $w = 1$ Y_2Y_1	Output z
0 0	1 0	1 1	0
0 1	0 1	0 0	0
1 0	1 1	0 0	0
1 1	1 0	0 1	1

6. A state machine has an input w and an output z. The machine is a sequence detector that produces z = 1 when the previous two values of w were 00 or 11; otherwise z = 0.
   a) Draw the state diagram.
   b) Provide the state table and the state-assigned table.