Inspiring Excellence

BRAC UNIVERSITY

CSE 350: Digital Electronics and Pulse techniques

Exp-04: Implementing Diode Logic (DL) , Resistor Transistor Logic (RTL) and Diode Transistor Logic (DTL) gates

Name:	Section:
ID:	Group:

Objectives

1. Construct Diode Logic (DL) gates.
2. Constructing a Resistor Transistor Logic (RTL) gate.
3. Constructing a Diode Transistor Logic (DTL) gate.
4. Understanding the circuit operations.

Equipment and component list

Equipment

1. Digital Multimeter
2. DC power supply

Component

- NPN Transistor (C828) - x1 piece
- Diode 1N4003 - x4 pieces
- Resistors -
  - 450 Ω - x2 piece
  - 2 KΩ - x2 pieces
  - 2.2 KΩ - x1 piece
  - 15 KΩ - x1 piece
  - 20 KΩ - x1 piece
  - 100 KΩ - x1 piece

Task 01: OR Gate

THEORY

In digital logic, a 2-input OR gate outputs a logical HIGH if at least one of the inputs is HIGH. Otherwise, the output of the OR gate is logical LOW.

In this task, we will implement a Diode Logic (DL) OR gate. In Fig. 1, we can see two input nodes (A and B) and one output node (Y) of the OR gate. We will consider 5V as logical HIGH input and 0V as logical LOW input in our experiment. Now, if any of the inputs are set to 5V, the corresponding diode is turned on. As a result, a current flows through that diode. This current ultimately flows through R towards the ground, thus creating a voltage drop across the R resistor. As R1 and R2 resistors are very small compared to R, the voltage drop across R will be close to 5V. In this case, we will consider the obtained output voltage at node Y to be logically HIGH. Next, if all the inputs are set to 0V, no current flows through the diodes and resistor R. As a result, the voltage drop across R will be zero. So, the output voltage will be 0V, which we will consider to be logically LOW.

Task-02: AND gate

THEORY

In digital logic, a 2-input AND gate outputs a logical LOW if at least one of the inputs is LOW. Otherwise, the output of the AND gate is logical HIGH.

Similar to the previous task, we will implement a Diode Logic (DL) AND gate. If any of the inputs are set to 0V, the corresponding diode is turned on. As a result, a current flows through that diode from the V_R voltage source. This current flows through R and creates a voltage drop across the resistor. As R_1 and R_2 resistors are very small compared to R, the voltage drop across R will be close to 5V. As a result, the obtained output voltage at node Y will be close to 0V which we will consider as logically LOW. Next, if all the inputs are set to 5V, no current flows through the diodes and resistor R. Therefore, the voltage drop across R will be zero. So, the output voltage will be the same as V_R or 5V, which is logically HIGH.

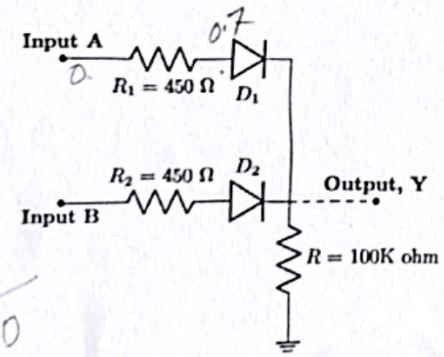


Fig 1: OR gate

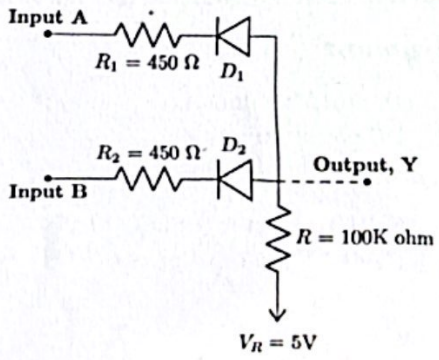


Fig 2: AND gate

Task-03: Inverter (NOT gate)

THEORY

In digital logic, an inverter or NOT gate is a logic gate which implements logical negation. It has a single input and a single output where the output is the exact opposite of the input. Meaning, if the input is Logical High, the output will be Logical Low and vice versa. The RTL implementation of an inverter circuit is shown in Figure 03.

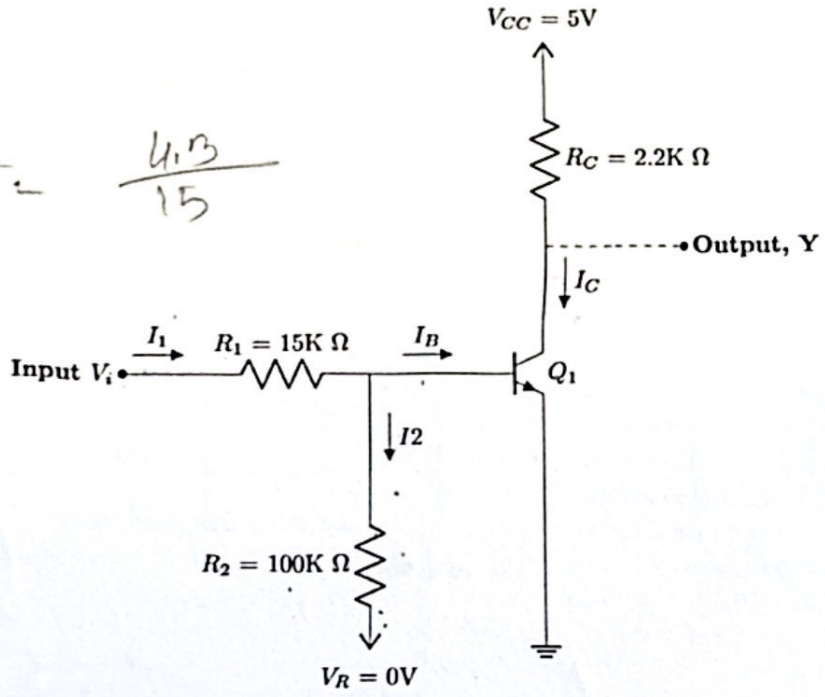


Fig 3: Inverter (NOT gate)

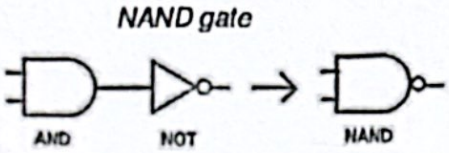
Here the input is applied to the base of a Transistor or, BJT (Q_1) through the resistor R_1 and the output is available at the collector terminal (point Y). We connect the ground terminal to the emitter node directly and to the base node through the resistor R_2. Hence, when the input V_i is LOW (0V), the 'Base' terminal of the transistor cannot be at a voltage higher than zero. For Q_1 to be turned ON, the Base-Emitter voltage difference must be greater than 0.5V. Thus, the BJT cannot turn ON when the input is LOW and operates in cutoff mode. This means Q_1 acts like an open circuit and the current passing through the R_C resistor (I_C) is zero. As a result, there will be no voltage drop in the resistor R_C and the voltage of the output point (Y) will be the same as V_{CC} = 5V (High).

On the other hand, if a HIGH input (5V) is applied at the input terminal (V_i), Q_1 will be driven into saturation mode. In this mode, the Collector-Emitter voltage difference (V_{CE}) is nearly 0.2V. As the emitter is connected to the ground terminal, the emitter voltage (V_E) is zero. Hence, the collector voltage will be close to 0.2V(LOW). Thus, the output of the circuit is always the opposite of the input.

Task-04: DTL NAND gate

THEORY

In this task, we will implement a Diode Transistor Logic (DTL) NAND gate. As can be seen in Fig. 4, a 2-input NAND gate outputs a logical HIGH if at least one of the inputs is LOW. Otherwise, the output of the NAND gate is logical LOW. It can be created by passing the output of an AND gate through an Inverter or NOT gate. One can build all other logic gates using such NAND gates. The DTL implementation of a NAND circuit is shown in Fig. 5.



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Figure 4: NAND gate Truth Table

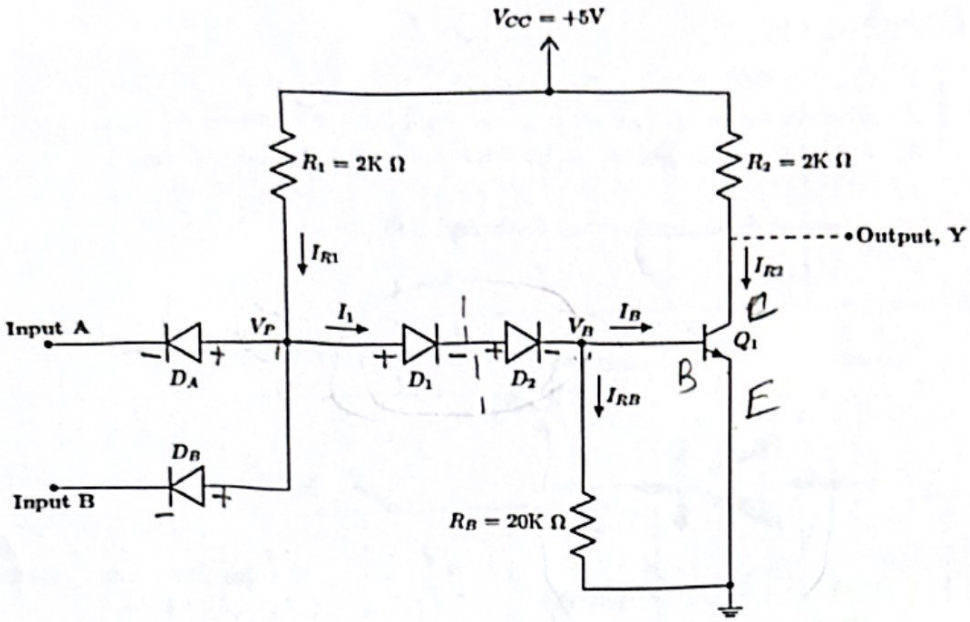


Figure 5: Diode Transistor Logic (DTL)

Diode–transistor logic (DTL) is a class of digital circuits that is the direct predecessor of transistor–transistor logic (TTL) and the successor of resistor-transistor logic (RTL). The output side of the basic DTL NAND circuit has a similar structure to the RTL inverter circuit, but it uses diode-logic AND on the input side. Thus, DTL circuits implement NAND gates by combining both DL and RTL logic, something that is not possible to do using solely RTL circuits or DL circuits. DTL also has better noise margin and fanout characteristics compared to RTL. (Noise margin indicates a circuit's immunity to noise, and fanout is the number of identical gates that a circuit can drive without facing errors).

On the input side of Fig. 5, we can see two diodes in reverse bias connection with respect to input - this acts as an AND gate circuit according to diode logic. The output of this AND gate is fed to the inverter input V_B (base terminal of BJT Q_1) through the diodes D_1 and D_2 creating the NAND circuit. The output is obtained at the collector terminal of Q_1.

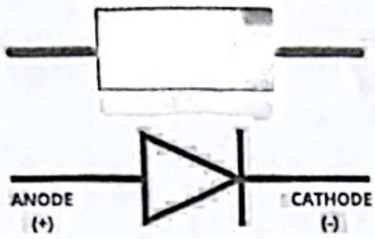
When both inputs are HIGH (5V), the cathode voltage of the diodes D_A and D_B become higher than their anode voltages. As a result, both input diodes operate in the reverse bias region (turned off/disconnected), and the node V_P has a high voltage level. This causes the transistor Q_1 to operate in the saturation mode and the NAND gate generates a LOW output. In this case, the voltage of point P (V_P) is close to 2.2V as the voltage of base terminal (V_B) in saturation is nearly 0.8V and there is a voltage drop of 0.7V in each of diodes D_1 and D_2.

When either input is LOW (0V), the corresponding input diode operates in the forward bias (turned on), and there is a voltage drop of 0.7V across the diode. Hence, the voltage at the node V_P becomes only 0.7V higher than the LOW voltage at the input and drops much below the 2.2V required to turn on the BJT Q_1. This causes the transistor Q_1 to work in the cutoff region and it acts like an open circuit. Hence, the current passing through the R_2 resistor (I_{R2}) is zero. As a result, there will be no voltage drop in the resistor R_2 and the voltage of the output point (Y) will be the same as V_{CC} = 5V (High).

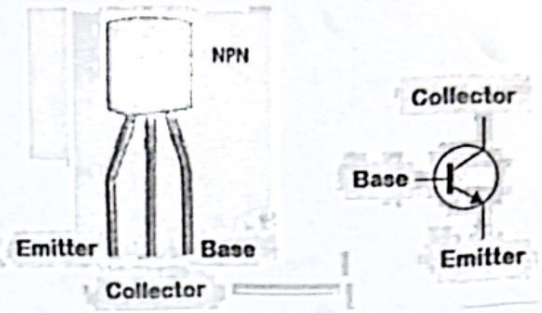
Procedure:

1. Connect the circuit as shown in Fig: 1, 2, 3 & 5.
2. Observe the output for all possible input combinations and thus verify the type of gate.
3. Fill up the following tables for OR gate, AND gate and Inverter.

The schematic and pin diagrams of diode and BJT are shown below:



Diode



Bipolar Junction Transistor (BJT)

Data Tables:

Table 1: OR Gate Data

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	0 mV	0mV	0 mA	0 mA	2.2 mV
0	5	0mV	21 mV	0 mA	0.0467mA	4.54mV
5	0	21.5mV	0 mV	0.0478mA	0 mA	4.49 mV
5	5	5.6mV	10.9mV	0.0124mA	0.0242mA	4.56mV

Table 2: AND Gate Data

$V_A(V)$	$V_B(V)$	$V_{R1}(V)$	$V_{R2}(V)$	$I_{R1}(mA)$	$I_{R2}(mA)$	$V_Y(V)$
0	0	5.6mV	16.2mV	0.0124mA	0.036mA	0.45V
0	5	21.5mV	0mV	0.45mA	0mA	0.5V
5	0	0mV	21.8mV	0mA	0.048mA	0.45V
5	5	0mV	0mV	0mA	0mA	4.8 V

Table 3: RTL inverter Data

V_i (V)	V_{R1} (V)	V_{R2} (V)	V_{RC} (V)	I_1 (mA)	I_2 (mA)	I_B (mA)	I_C (mA)	V_Y (V)
0	0V	0V	5V	0mA	0mA	0mA	2.27mA	5V
5	4.3V	0.6V	4.9V	0.286mA	6×10^{-3}mA	0.28mA	2.3mA	32.2mV

Table 4: NAND Gate Data

V_A (V)	V_B (V)	V_{DA} (V)	V_{DB} (V)	V_P (V)	I_{R1} (mA)	I_{R2} (mA)	V_B (mV)	V_Y (V)
0	0	0.5V	5.2V	6.2V			12.8mV	4.7V
0	5	0.6V	4.3V	0.6V			16.8mV	4.9V
5	0	4.3V	0.6V	0.6V			17.6mV	4.8V
5	5	2.8V	2.8V	1.95V			0.7V	19.9mV

Sudik 4/8/25

Signature

Lab Tasks:

Lab Task-01

Use a Multimeter as Ammeter to measure I_B and find the relation between the currents I_{R1}, I_B and I_{RB} when all inputs are **HIGH**

Lab Task-02

Remove the diodes D_1 and D_2 and then measure the output voltage for the four different input cases. Verify and briefly explain if the circuit still works properly as a NAND gate.

V_A (V)	V_B (V)	V_Y (V)
0	0	4.6V
0	5	3.7 V
5	0	3.4 V
5	5	19.8mV

Lab Task-03

Vary the **input A** from **0V to 5V** while keeping **input B** fixed at 5V. What is the **maximum** value of **input A** for which the **output** remains **HIGH**? [consider any voltage above 1V as **HIGH**]

1.8 V

Report

Please answer the following questions briefly in the given space.

1. Verify that the transistor will be operating in the saturation and cutoff region in two cases for the inverter circuit in figure 3 (Use experimental data for verification).

Ans. Saturation:

input, $V_i = 5V$

$V_{BE} = 0.8V$; $V_{CE} = 0.2V$

$V_{CE} = V_0 = 0.2V$ ($V_E = 0$)

∴ output is low

From table; $I_C = 2.3mA$

$I_B = 0.28mA$

$\beta_F = \frac{I_C}{I_B} = 8.21 < 30$

∴ assumption is correct

cut off:

$I_B = I_C = I_E = 0A$

Low input, $V_i = 0V$

$I_C = 0$

$\Rightarrow \frac{V_{CE} - V_0}{R_C} = 0$

$\Rightarrow \frac{5.03 - V_0}{2.2K} = 0$

$\therefore V_0 = 5.03V$

∴ output is high

Again, applying KCL,

$I_1 = I_B + I_2$

$\Rightarrow \frac{V_i - V_B}{R_1} = 0 + \frac{V_B - 0}{R_2}$

$\Rightarrow \frac{-V_B}{15K} = \frac{V_B}{100K}$

$\therefore V_B = 0.077V = V_{BE}$

$\therefore V_{BE} < 0.5V$

∴ Assumption is correct.

2. For an OR gate circuit, should I_{R1} and I_{R2} be equal theoretically when $V_A = V_B = 5V$? Did you obtain a similar result in your experiment? Explain briefly.

Ans. When $V_A = V_B$, we get little difference in result of I_{R1} and I_{R2} due to technical error. We didn't get the exact same but I_{R1} and I_{R2} values are very close. As it is practical experiment, so some factor vannies from person to person and affect the vales

For $V_A = V_B = 5.04V$, we got $I_{R1} = 0.0129mA$ and $I_{R2} = 0.0242mA$

3. (For both OR & AND gate circuits) Will the diodes D_1 and D_2 turn ON, if $V_A = V_B = 6V$ and $V_R = 5V$? Explain briefly.

Ans. For OR gate, D_1 and D_2 turns on because to activate a diode, it atleast needs 0.7V drop above the cathode So, in this scenario, due to 0.7V drop in both diodes, it will activate D_1 and D_2 in OR gate combination.

On the other hand, for AND gate, D_1 and D_2 remains off due to presence of 6V at both input of diode. $V_A = V_B = 6V$; $V_R = 5V$

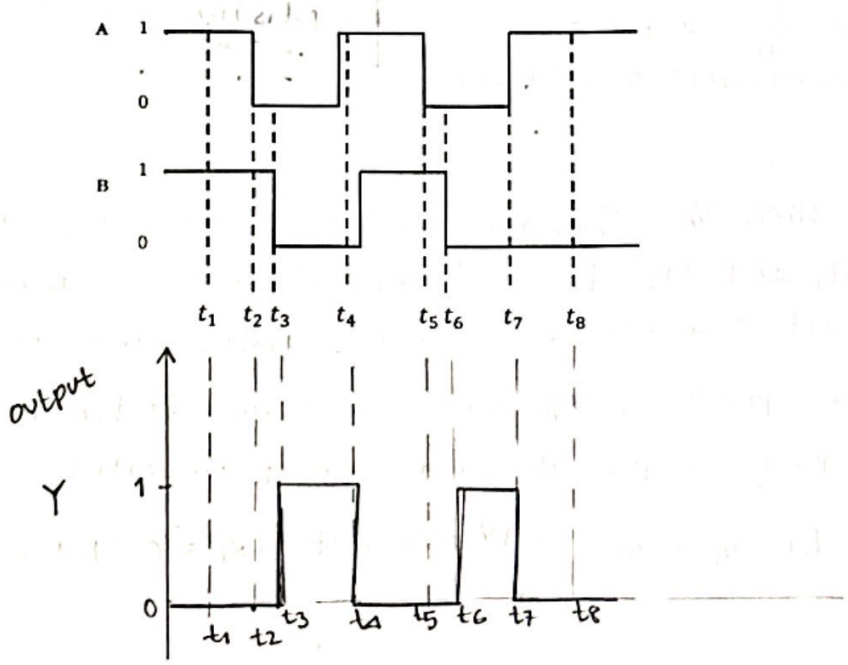
$\therefore V_0 - 0.7 = 5 - 0.7 = 4.3 < 6V$

So, the D_1 and D_2 remains off.

4. What is the function of $V_R = 0V$ at the base of an inverter in figure 3?

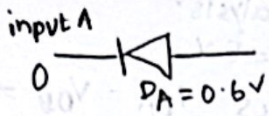
Ans. At the base of an inverter for $V_R = 0V$ is the operational point. So, when the input is 0V and terminal base at 0. For transistor to be switched on, the V_{BE} must be greater than 0.7V. So, the BJT can't be switched on at low input & cut off mode. So, there will no voltage drop at R_C as there's no current flow. And the output V_0 remains same as V_{CC}. So the output is high when input is low.

5. Assuming AND gate, Draw the output.



6. Using experimental data, find the operating mode of Q_1 in figure 5 of the DTL when input A is LOW and input B is HIGH. Additionally, find whether diodes D_A and D_B are ON or OFF (by using the voltage across them).

Ans. For diode,



For $V_A = 0$ and $V_B = 5$ V,

Voltage across Diode A, $V_{DA} = 0.6$ V and its on and current flows from V_p through D_A to input A (0V).

Again, for D_B is off and in reverse bias and no current follows and disconnect from circuit and $V_{DB} = 4.8$V

For transistor,

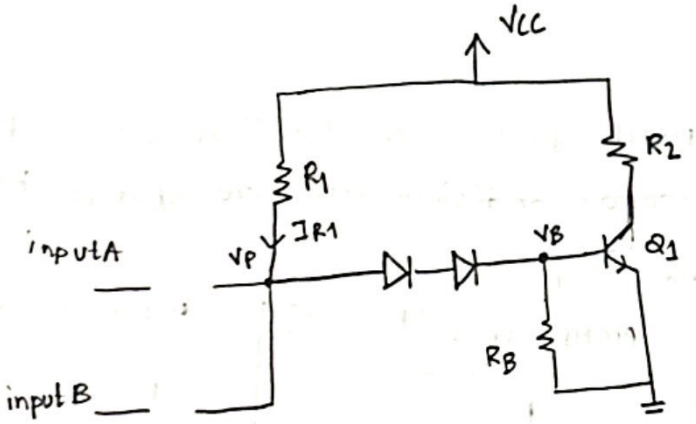
$V_p = 0.6$ is insufficient to switch D_1 and D_2 on in series,

And base voltage := $V_p - V_{D1} - V_{D2} = 0.6V - 0.7V - 0.7V = -0.8V$

as the base voltage is negative and Q_1 doesn't turn on

$\therefore Q_1$ operates in cut off mode.

7. Assume that the output of the circuit shown in Fig: 5 of the DTL is LOW. Draw the partial circuit consisting of only those components which remain active.



8. Use the relation you found in Lab Task 1 between the currents I_{R1}, I_B and I_{RB} when all inputs are HIGH to verify the operating mode of Q1. [Assume beta (β_F) ≥ 100]

Diode state Analysis:

$V_A = V_B = 5\,V$

Both diodes $V_{DA} = V_{DB} = 2.8V$ which indicates both are reverse biased and they are off.

I_{R1}

$I_{R1} = \frac{V_{CC} - V_P}{R_1}$

$= \frac{(5 - 1.95)V}{5K\Omega}$

$= 0.203mA$

I_B

$V_B = V_P - V_{D1} - V_{D2}$

$= 1.95 - 0.7 - 0.7$

$= 0.55V$

$V_{RB} = 0.5V$

$I_B = \frac{V_{RB}}{V_B} = 0.25mA$

I_{RB}

$V_{RB} = \frac{V_P - V_{BE}}{R_B} = \frac{1.95 - 0.7}{20K\Omega} = 0.0625\,mA$

I_B

$I_B = I_{R1} - I_{RB} = 0.1405\,mA$

operating mode:

$I_B \times \beta_F = 14.05\,mA$ which is langer than collector current.

~~140mA~~

∴ Q1 in saturation mode.

9. In a DTL NAND gate, when one input is held HIGH, its diode becomes reverse-biased and effectively removed from the circuit. Based on this, can the gate function as a DTL inverter (NOT gate)? Justify your answer using the behavior of the circuit and the NAND gate truth table.

Yes the DTL NAND gate can function as a DTL inverter ~~on some condition~~. when one input is held 5V.

~~Then~~ Truth table comparison

input A	NAND output (B = High)	inverter output
0 (Low)	1	1
1 (high)	0	0

When input A is Low, D_A conducts and Q1 in cut off mode as a result output is high.

So, the DTL NAND gate can function as DTL inverter when one input is fixed to High because it makes the NAND truth table identical to inverter under this condition

10. Write a discussion and include the following: your overall experience, accuracy of the measured data, difficulties experienced, and your thoughts on those.

While performing task-01 and task-02 of OR gate and AND gate using diode, we didn't face any difficulties and took values easily. And our experimented values are close to theoritical values.

But while doing task-03, we had to use BJT for inverter or not gate implementation. The multimeter was giving some errors in values. But later on solved by fixing the connection of loosely connected wires. Thus we concluded our experiment.