Interfacing with 8255A Programmable Peripheral Interface (PPI)

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Abstract—**Microprocessor is capable of handling fewer I/O devices itself. To expand its capability, it is necessary to add other hardware. The Intel 8255A Programmable Peripheral Interface is used for this task. It can be easily interfaced with the Microprocessor and requires no external logic. This report contains the detail information about the 8085 Microprocessor Training kit and 8255A expansion kit. Examples citing different modes of operation of 8255A PPI are also included.**

I. Introduction

8255A PPI provides additional I/O capability for the Microprocessor. Devices like transducers, keyboards, displays, printers, etc can be interfaced with the Microprocessor easily. This basic concept of interfacing can be very helpful for the Computer engineers and help them build up the concept in Microprocessor based instrumentation systems.

II. The 8085 trainer kit

MPS 85-3 is Intel 8085 Microprocessor trainer kit used in the laboratory. It is all in one kit for software and hardware development and for research purposes. The board contains the following components.

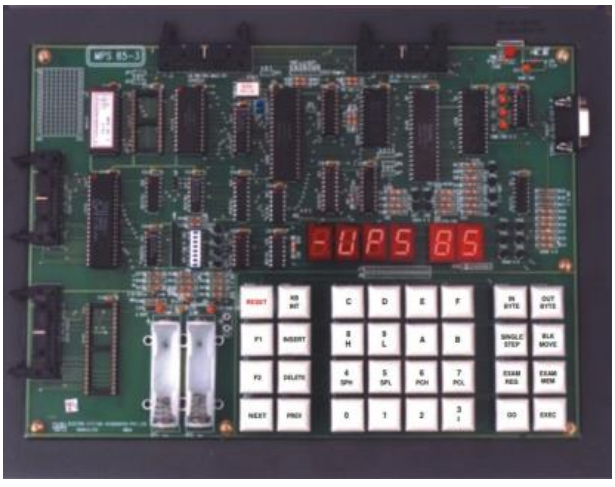

Fig.1. 8085 Microprocessor Trainer Kit

A. 8255A

There are two 8255A available to give 48 programmable I/O lines. One of them is mapped at the base address of 40H and another is mapped at the base address of 00H. The I/O lines of each 8255A are connected to 26 pin ribbon cable connectors J1 (for 8255A at 00H) and J2 (for 8255A at 40H). Using these connectors, the external devices such as seven segment displays, keyboards, servo motor, etc. can be interfaced.

B. Bus Expansion

Fully de-multiplexed and buffered TTL compatible system bus signals (address, data and control lines) are brought out through two 26 pin ribbon cable connectors J3 and J4 for expansion. The bus expansion is used to monitor and control the external devices which are interfaced with the kit.

C. 8255 Expansion Kit

Expanded using J3 and J4 connectors of the Microprocessor Kit and is mapped at base address of 80H.

III. 8255A PPI

The 8255A is a Programmable Peripheral Interface (PPI) device designed for the use in Intel Microcomputer systems. Its function is that of the general purpose IO component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices.

The 8255A is a 40 pin DIP chip. It is a high performance device with 24 programmable pins. It is compatible with all Intel and most other microprocessors. The 24 pins are IO pins grouped into 3 ports of 8 pins each: Port A, Port B, Port C. Each of the ports can be programmed as either an input or an output port. Port C is further divided into Port C_{lower} and Port C_{upper} of 4 bits each.

A. Data Bus Buffer

The three-state bi-directional 8 bit buffer is used to interface the 8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus.

B. Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

1) (RD) Read: A "low" on this input pin enables 8255 to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255.

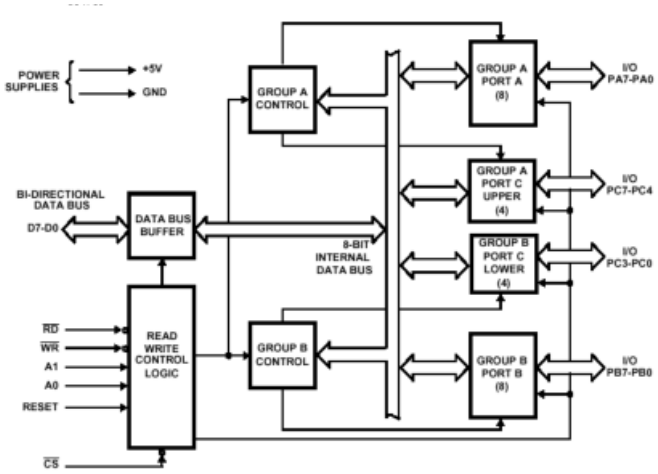

Fig. 2. Functional Block Diagram of 8255A PPI

2) (WR) Write: A "low" on this input pin enables the CPU to write data or control words into the 8255.

3) RESET: A "high" on this pin initializes the control register to 9BH and all ports (A, B, C) are set to the input mode.

4) (CS) Chip Select, A_o, and A_1: The combination of these bits is used for the device and port selection. The CS is connected to the decoded address, while A_0 and A_1 are connected to MPU address lines.

TABLE I
PORT SELECTION SIGNAL OF 8255 PPI

CS	A_1	A_0	Selection
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	No Selection

C. Control Word

Control word is the content of the control register. It specifies the I/O of each port as well as the Bit Set/Reset capabilities of Port C. the two modes of control word are:

1) I/O Mode: In this mode, D_7 of the control word is 1. Bits $D_6 – D_0$ determines the various modes of I/O of the three ports.

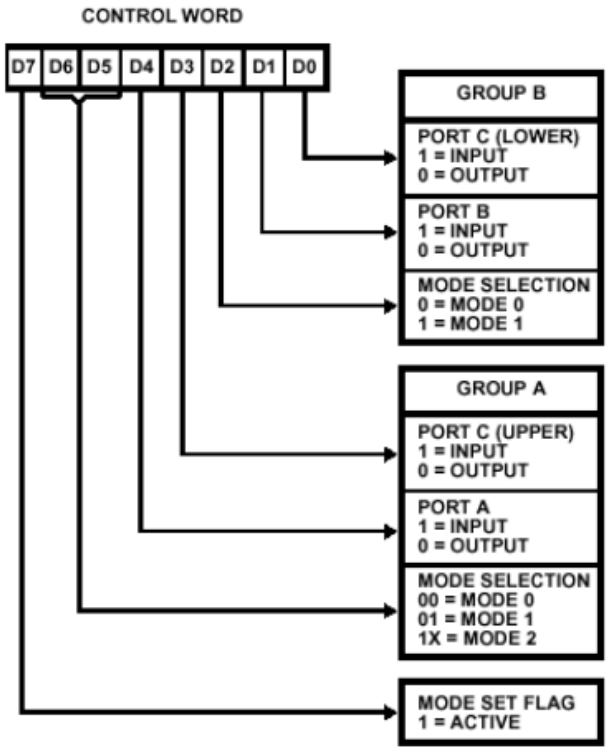

Fig. 3. 8255A Control Word Format in I/O Mode

2) BSR Mode: This mode is called the Bit Set/Reset Mode. The D7 bit is 0. This mode is used to set or reset the individual pins of Port C.

D. Modes of Operation

The ports of 825A can be operated in various ways as described below:

1) Mode 0: This is the basic I/O mode. It provides the simple input and output functionality to all the three ports and no handshaking signals are required in this mode.

2) Mode 1: This mode is called the Strobe I/O mode. It provides a means for transferring I/O data to or from a specified Port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals. The basic characters of Mode 1 are:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control / data port

- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8bit data port.

3) Mode 2: This mode is also called Strobe Bi-Directional I/O. It provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available. The basic characters of Mode 2 are:

- Used in Group A only
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

IV. 8255A EXPANSION KIT

It is a circuitry with 8255A chip to learn more about the working of the PPI. The interface has 4 DIP switches SW1, SW2, SW3 and SW4. The 8255A ports A and B can be configured as output ports by sending the appropriate control word to its control register, and keeping the switches SW1 and SW3 respectively in output position. Switches SW2 and SW4 will have no effect then.

The 8255A port A can be configured as input port by using appropriate control word and keeping SW1 in input position. When the program executes, it reads the status of switch SW2. Similarly, port B can be configured as input in software while keeping SW3 in input position. When the program executes, it reads the status of SW4 position.

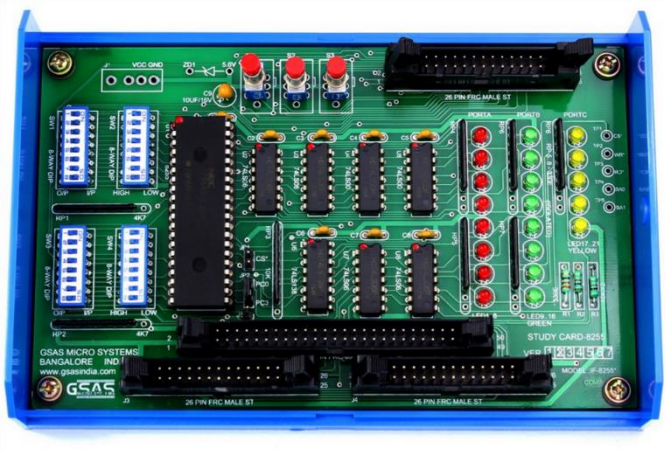

Fig. 4. 8255A Expansion Kit

8 red LEDs are provided to read the status of port A and 8 green LEDs are provided to read the status of port B. But only 5 yellow LEDs are provided to read the handshake signal status (port C). The strobe signals (PC2, PC4 and PC6) are not provided. These LEDs can be seen at the right side of the board in Fig 4.

Switches S1, S2 and S3 are provided to simulate STB and ACK signals (top side of board in Fig 4) in Mode 1 and 2. Provision is made for connecting buffered external interrupt (RST 7.5, etc.) to J5 by keeping the jumper JP2 at PC0 or PC 3 depending on the type of mode.

The interface has 4 connectors named as J2, J3, J4, and P1. J3 and J4 are reserved for connecting to MPS 85-3 trainer. All the 24 I/O lines are brought out to the J2 connector. But port C lines are used as handshake signals. So the user cannot use those lines (only port A and B lines available to user). P1 connector is not used.

IV. INTERRUPTS IN MICROPROCESSOR

The interrupt is a state where the external device informs the MPU that it is ready to communicate and requires attention. Interrupts can be both hardware and software types which can again be maskable that requiring immediate response or non-maskable that can be responded some time later. There are two types of Interrupts. They are:

A. Hardware Interrupts

There are several interrupts pin in the Microprocessor which are used while performing such interrupts. For 8085, there are eight interrupt pins.

TABLE II
HARDWARE INTERRUPTS IN 8085

Priority	Interrupt	Trigger	Maskable	Call Location
1	TRAP	Edge and Level	No	0024H
2	RST 7.5	Level	Yes	003CH
3	RST 6.5	Level	Yes	0034H
4	RST 5.5	Level	Yes	002 CH
5	INTR	Level	Yes	X

B. Software Interrupts

Software interrupts are performed with the help of software (programs). The software interrupts in 8085 are:

1) *RST Instructions:* RST stands for restart. These are 1 byte instructions that transfer the program execution to a specific location on 00H.
2) *EI (Enable Interrupt) and DI (Disable Interrupt:* These are 1-byte instructions that are used to enable or disable maskable interrupts in 8085.
3) *SIM:* It stands for Set Interrupt Mask. It is a 1-byte instruction that reads the contents of the accumulator and enables or disables (set mask)

the interrupts RST 7.5, RST 6.5, and RST 5.5 according to the content of the accumulator. It is also used for resetting the RST 7.5 flip-flop. It helps to implement serial I/O.

4) *RIM (Read Interrupt Mask):* It is also a 1-byte instruction. It is used to read interrupt masks. It loads the accumulator with the 8-bits showing the current status of the interrupt masks. The bits $D_{4,}$ D_5, and $D_{6\ identify}$ the pending interrupts.

VI.CONCLUSION

The basics of interfacing I/O devices to the 8085 microprocessor were studied with the help of 8255A PPI expansion kit. Interfacing peripheral devices to the Microprocessor is very important for a computer engineer. The solution to the lab assignments are given in the Appendices below.

VII. APPENDIX

TABLE III

SOLUTION OF PROBLEM 1(A)

Address	Label	Mnemonics	Opcode
8000		MVI A,81	3E 81
8002		OUT 43	D3 43
8004		MVI A,AA	3E AA
8006		OUT 40	D3 40
8008		MVI A, 55	3E 55
800A		OUT 41	D3 41
800C		RST 5	EF

TABLE IV

SOLUTION OF PROBLEM 1(B)

Address	Label	Mnemonics	Opcode
8000		MVI A,81	3E 81
8002		OUT 43	D3 43
8004		MVI A,0D	3E 0D
8006		OUT 43	D3 43
8008		MVI A, 09	3E 09
800A		OUT 40	D3 40
800C		MVI A,05	3E 05
800E		OUT 41	D3 41
8010		MVI A,01	3E 01
8012		OUT 41	D3 41
8014		RST 5	EF

TABLE V

SOLUTION OF PROBLEM 1(C)

Address	Label	Mnemonics	Opcode
8000		MVI A,80	3E 80
8002		OUT 43	D3 43
8004		MVI A,0D	3E 0D
8006		OUT 43	D3 43
8008		MVI A,09	3E 09
800A		OUT 40	D3 40
800C		MVI A,05	3E 05
800E		OUT 41	D3 41
8010		MVI A,01	3E 01
8012		OUT 41	D3 41
8014		RST 5	EF

TABLE VI

SOLUTION OF PROBLEM 2(A)

Address	Label	Mnemonics	Opcode
8000		MVI A,90	3E 90
8002		OUT 83	D3 83
8004		MVI A,AA	3E AA
8006		OUT 80	D3 80
8008		OUT 81	D3 81
800A		OUT 82	D3 82
800C		RST 5	EF

TABLE VII

SOLUTION OF PROBLEM 2(B)

Address	Label	Mnemonics	Opcode
8000		MVI A,80	3E 80
8002		OUT 43	D3 83
8004		MVI A,01	3E 01
8006		OUT 82	D3 82
8008		RLC	07
8009		OUT 82	D3 82
800B		RLC	07
800C		OUT 82	D3 82
800E		RLC	07
800F		OUT 82	D3 82
8011		RLC	07
8012		OUT 82	D3 82
8014		RLC	07
8015		OUT 82	D3 82
8017		RLC	07
8018		OUT 82	DE 82
801A		RLC	07
801B		OUT 82	D3 82
801D		RST 5	EF

TABLE VII

SOLUTION OF PROBLEM 3(A)

Address	Label	Mnemonics	Opcode
8000		MVI A,90	3E 90
8002		OUT 83	D3 83
8004		MVI A,80	3E 80
8006		OUT 43	D3 43
8008		IN 80	D3 80
800A		OUT 81	D3 81
800C		OUT 40	D3 40
800E		RST 5	EF

TABLE IX

SOLUTION OF PROBLEM 3(B)

Address	Label	Mnemonics	Opcode
8000		MVI A,92	3E 92
8002		OUT 83	D3 83
8004		MVI A,80	3E 80
8006		OUT 43	D3 43
8008		IN 80	DB 80
800A		MOV B,A	47
800B		IN 81	DB 81
800D		ADD B	80
800E		OUT 40	D3 40
8010		JNC SKIP	D2 17 80
8013		MVI A,01	3E 01
8015		OUT 42	D3 42
8017	SKIP :	RST 5	EF

TABLE X

SOLUTION OF PROBLEM 4(A)

Address	Label	Mnemonics	Opcode
8000		MVI A ,B0	3E B0
8002		OUT 83	D3 83
8004		MVI A,09	3E 09
8006		OUT 83	D3 83
8008		MVI A,0E	3E 0E
800A		SIM	30
800B		EI	FB
800C	LOOP :	JMP LOOP	C3 0C 80
8FB3		JMP 9000	C3 00 90
9000		IN 80	DB B0
9002		OUT 81	D3 81
9004		EI	FB
9005		RET	C9

TABLE XI

SOLUTION OF PROBLEM 4(B)

Address	Label	Mnemonics	Opcode
8000		MVI A,86	3E 86
8002		OUT 83	D3 83
8004		MVI A,05	3E 05
8006		OUT 83	D3 83
8008		MVI A,0D	3E 0D
800A		SIM	30
800B		EI	FB
800C	LOOP :	JMP LOOP	C3 0C 80
8FB3		JMP 9000	C3 00 90
9000		IN 81	DB B1
9002		OUT 80	D3 80
9004		EI	FB
9005		RET	C9

TABLE XII

SOLUTION OF PROBLEM 5(A)

Address	Label	Mnemonics	Opcode
8000		MVI A,CO	3E C0
8002		OUT 83	D3 83
8004		MVI A,09	3E 09
8006		OUT 83	D3 83
8008		MVI A,0D	3E 0D
800A		OUT 83	E3 83
800C		MVI A,0D	3E 0D
800E		SIM	30
800F		EI	FB
8010	LOOP :	JMP LOOP	C3 10 80
8FB9		JMP 9000	C3 00 90
9000		IN 80	DB 80
9002		OUT 81	D3 81
9004		MVI A,0F	3E 0F
9006		OUT 80	D3 80
9008		EI	FB
9009		RET	C9

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