LIST OF PUBLICATIONS

- [1] K. Rosvall, T. Mohammadat, G. Ungureanu, J. Öberg, and I. Sander, "Exploring power and throughput for dataflow applications on predictable noc multiprocessors," in 2018 21st Euromicro Conference on Digital System Design (DSD), Aug 2018, pp. 719–726. [Online]. Available: https://ieeexplore.ieee.org/document/8491891
- [2] J. Öberg, "Synthesis of vliw accelerators from formal descriptions in a real-time multi-core environment," in *Proceedings of the 14th FPGAworld Conference*, ser. FPGAworld '17. New York, NY, USA: ACM, 2017, pp. 23–29. [Online]. Available: http://doi.acm.org/10.1145/3135997.3135999
- [3] M. Fakih, A. Lenz, M. Azkarate-Askasua, J. Coronel, A. Crespo, S. Davidmann, J. C. Diaz Garcia, N. G. Romero, K. Grttner, S. Schreiner, R. Seyyedi, R. Obermaisser, A. Maleki, J. berg, M. T. Mohammadat, J. Prez-Cerrolaza, I. Sander, and I. Sderquist, "Safepower project," *Microprocess. Microsyst.*, vol. 52, no. C, pp. 89–105, Jul. 2017. [Online]. Available: https://doi.org/10.1016/j.micpro.2017.05.016
- [4] R. Seyyedi, M. Mohammadat, M. Fakih, K. Gruttner, J. Oberg, and D. Graham, "Towards virtual prototyping of synchronous real-time systems on noc-based mpsocs," in 2017 12th IEEE International Symposium on Industrial Embedded Systems (SIES), June 2017, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/7993375
- [5] A. Lenz, M. A. Blzquez, J. Coronel, A. Crespo, S. Davidmann, J. C. D. Garcia, N. G. Romero, K. Grttner, R. Obermaisser, J. berg, J. Perez, I. Sander, and I. Sderquist, "Safepower project: Architecture for safe and power-efficient mixed-criticality systems," in 2016 Euromicro Conference on Digital System Design (DSD), Aug 2016, pp. 294–300. [Online]. Available: https://ieeexplore.ieee.org/document/7723566
- [6] P. I. Diallo, S. Attarzadeh-Niaki, F. Robino, I. Sander, J. Champeau, and J. Oberg, "A formal, model-driven design flow for system simulation and multi-core implementation," in 10th IEEE International Symposium on Industrial Embedded Systems (SIES), June 2015, pp. 1–10. [Online]. Available: https://ieeexplore.ieee.org/document/7185067
- [7] H. Ezzeddine, J. berg, and F. Robino, "Validation of pipelined double-precision floating point operations in a multi-core environment implemented on fpga using the forsyde/noc system generator tool suite," in 2014 NORCHIP, Oct 2014, pp. 1–6. [Online]. Available: https://ieeexplore.ieee.org/document/7004748
- [8] F. Robino and J. Öberg, "From simulink to noc-based mpsoc on fpga," in *Proceedings of the Conference on Design, Automation & Test in Europe*, ser. DATE '14. 3001 Leuven, Belgium, Belgium: European Design and Automation Association, 2014, pp. 328:1–328:4. [Online]. Available: http://dl.acm.org/citation.cfm?id=2616606.2617074
- [9] F. Robino and J. Öberg, "The heartbeat model: A platform abstraction enabling fast prototyping of real-time applications on noc-based mpsoc on fpga," in 2013 8th International Workshop on Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC), July 2013, pp. 1–8. [Online]. Available: https://ieeexplore.ieee.org/document/6581536
- [10] N. P. Mand, F. Robino, and J. berg, "Artificial neural network emulation on noc based multi-core fpga platform," in *NORCHIP 2012*, Nov 2012, pp. 1–4. [Online]. Available: https://ieeexplore.ieee.org/document/6403122
- [11] J. Öberg and F. Robino, "A noc system generator for the sea-of-cores era," in *Proceedings of the 8th FPGAWorld Conference*, ser. FPGAWorld '11. New York, NY, USA: ACM, 2011, pp. 4:1–4:6. [Online]. Available: http://doi.acm.org/10.1145/2157871.2157875