Concordia University

Department of Electrical and Computer Engineering

COEN313 – Digital Systems Design II (3.5 credits) – Winter 2018

Course Coordinator:

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Section	Days	Time		Professor / TA
Lecture	-T-J---	16:15~17:30	**H-407**	Ait Mohamed, Otmane
Tut: WA	M------	10:15~11:00	**H-420**	Marwan, Ammar m_amma@encs.concordia.ca
Tut: WB	M------	10:15~11:00	**FG-B055**	Goel Anish an_goe@encs.concordia.ca

1. Calendar Description

Prerequisite: COEN231, COEN 212 or COEN312. Two-level and multi-level logic optimization techniques. Hardware description languages (VHDL) for synthesis and simulation. Asynchronous design. Algorithmic state machines. Clocking and clock skew. Metastability. Self-timed concepts. Finite state machine (FSM) optimization. State reduction. FSM partitioning. Programmable logic devices and field programmable gate arrays. Data path and control design for processors. Testing issues. Lectures: three hours per week. Tutorial: one hour per week. Laboratory: 15 hours total.

2. Course Objectives

This course will introduce students to Digital Design concepts through VHDL and synthesis of digital circuits. The student will also be exposed to programmable logic devices such as FPGAs. Sequential state

machine design techniques will be explored. Asynchronous sequential logic will be also presented. These objectives may be slightly modified to suit timing considerations.

3. Course Learning Outcomes (CLOs)

Upon successful completion of the course, students will be able to

1. Gain insights into the various system representations (behavioral, structural and physical) used to describe digital systems.
2. Implement the top-down digital system design process to gradually transform an abstract high-level system description into a detailed low-level structural description.
3. Apply basic modeling concepts of VHDL including pure structural descriptions, abstract behavioral descriptions, and test benches.
4. Develop familiarity with the basic VHDL constructs (including concurrent and sequential statements) and understand the relationship between them and the hardware components.
5. Employ good design practices and guidelines to create synthesizable VHDL descriptions of combinational and sequential logic circuits.
6. Demonstrate skills in implementing RT-level circuits including combinational circuits, regular sequential circuits, and finite state machines.
7. Use the register transfer methodology (including RT operations, data path, control path and ASMD charts) to realize sequential algorithms in hardware.
8. Use Electronic Design Automation (EDA) tools proficiently for digital system design: VHDL design entry, simulation and synthesis.

4. Graduate Attributes

This course emphasizes and develops the following CEAB (Canadian Engineering Accreditation Board) graduate attributes and indicators:

Graduate Attribute	Indicator	Level of knowledge	Evaluation	CLO
A knowledge base for engineering	KB-3. Knowledge base in a specific domain (ELEC and COEN)	Intermediate	Midterm, Final exam	1, 2, 3, 4
Design	DE-1. Define the objective DE-2. Idea generation and selection DE-3. Detailed design DE-4. Validation and implementation	Intermediate Intermediate Intermediate Intermediate	Lab	5, 6, 7, 8

5. Evaluation

There will be five (5) lab works, a midterm exam, and a final exam. In addition, there will be 10% of the mark assigned upon the completion of the assigned problems before and after each topic on the zyBook platform (see Section 6.2).

Evaluation tool	Weight
Participation Activities	10%
Lab Works	25%
Midterm Exam	25%
Final Exam	40%

6. Course Organization

6.1. Lectures

There will be two lectures a week. Each lecture lasts approximately 1 hour and 15 minutes. The course slides will be based on zyBook platform. You are required to read and complete all participation activities assigned before lectures.

6.2. Web-based ZyBook

Digital Design zyBook is written from scratch for the web. So, it looks very different from a textbook. zyBook authors use less text, because some concepts are better taught with:

- **Animations**: Figures often try to teach a dynamic concept: Programs execute one statement at a time; a graph is plotted point by point; electrons flow across a resistor. Numerous figures with lengthy explanations can be replaced by one animation. If a picture is worth a thousand words, an animation is worth five thousand.
- **Learning questions**: A page of text is like a lecture. A paragraph plus interactive questions is like a dialogue. One student said "I feel like the zyBook is working with me rather than speaking to me". Thus, after defining a concept with brief text, a zyBook author uses questions to provide examples, expound, and more.

A **participation activity** is typically an animation or learning question, for which a student's completion is visible to an instructor, and for which any student can get 100% completion just by participating. An animation's steps just need to be viewed. A learning question just needs to be eventually answered correctly, and answers are available to students.

Participation activities are NOT homework problems, quizzes, or supplementary to the text. They are an integral part of the reading material. Many concepts only exist in activities. The questions' explanations are key elements, especially for wrong answers that seek to break down misconceptions (a proven-important part of teaching).

A **challenge activity** requires the student to answer correctly, and answers are not provided to the student. A CA is akin to traditional homework: Small tasks that give students practice. In education lingo, they are formative assessments. CA's give students immediate feedback, aiding the learning. Some CA's are algorithmically-generated. Some provide solutions if a wrong answer is entered, requiring the student to then answer a different problem. Some are "progressions", algorithmically-generating an easy problem initially, and increasing in difficulty (about 5 levels) after the student gets a level right.

You need to follow the following procedure to get access to Digital Design zyBook:

Sign in or create an account at learn.zybooks.com

Enter zyBook code

CONCORDIACOEN313AitMohamedWinter2018

Subscribe

Other references:

- Pong P.Chu. RTL Hardware Design using VHDL, Coding for Efficiency, Portability, and Scalability, John Wiley & Sons, Inc., 2006.
- M. Morris Manos, Digital Design Third Edition, Prentice Hall .
- T. Obuchowicz, It's Only VHDL (But I Like It), Prentice Hall.

6.3. Tutorial Workshop

During the tutorial session you will discuss and solve challenging/participation questions based on the Zybook platform. You need to arrive prepared to the tutorial workshop(TW). Attendance to the TW is mandatory.

6.4. Laboratory work

- There will be 5 laboratory experiments.
- For more details on the labs, refer to the COEN 313 Laboratory Guidelines.
- You must attend all laboratory sessions, participate in the experiments, and secure **at least 50%** in the laboratory grade to pass the course!

6.5. Midterm Exam

The midterm exam is scheduled for: Thursday, Feb 15. The midterm will take place during the regularly scheduled class time in classroom (16h15 to 17h30). It will be your responsibility to ensure your availability for the exam. All the material covered before the exam date will be included in the exam.
Notes:

- There will be no make-up midterm exam. Students absent from the midterm exam for any reasons will receive 0% for their midterm grade and will write the final exam for 65% of their total grade.
- Students absent from the midterm and the final will receive an R grade if they get less than 30%.

6.6. Final Exam

The final exam is scheduled by the University. The date and place will be announced later.

- Final will be counted for 65% of your total grade, if you do better on final. That is, the larger of {(65%*final), (40%*final+25%*midterm)} will be used.

7. Tentative Course Plan

1- Combinational Logic

2- Sequential Logic
3- Datapath Component
4- RTL Design
5- Asynchronous Design

Notes:

- In the event of extraordinary circumstances beyond the University's control, the content and/or evaluation scheme in this course is subject to change.
- At the beginning of the course you need to submit 2 Expectation of Originality Forms: one to the course instructor, and one to your lab demonstrator together with your 1st lab report.
- The expectation of originality form can be found at: http://www.concordia.ca/content/dam/encs/docs/Expectations-of-Originality-Feb14-2012.pdf.
- Each lab report needs to have a cover sheet that must have the following sentence: "I certify that this submission is my original work and meets the Faculty's Expectations of Originality" and your signature.
- Only ENCS approved calculators will be allowed in a midterm and final exams.
- Cell phones are not allowed in a midterm and final exams. An Academic Misconduct Incident report will be issued to any student who is in possession of any unauthorized electronic device in a midterm and final exams. (Please note just turning the cell phone off is not ok, it must not be in the student's possession.)

8. Academic Honesty

You are training to be a professional engineer. Consequently, we expect you to behave like a professional. A professional engineer is polite, considerate and respectful of others. It is rude, inconsiderate, and disrespectful to your fellow students and to the professor to talk in class or arrive late to the lecture. No one can learn if you are chatting to your neighbor!

All Concordia University students must abide by the University's Academic Code of Conduct (Concordia University Undergraduate Calendar Section 16.3.13). Any suspected violation of the Code will be turned over to a University Committee for investigation.
The Academic Code of Conduct is available at:
http://www.concordia.ca/students/academic-integrity/code.html

9. List of Services

Concordia Counselling and Development offers career services, psychological services, student learning services, etc.
The Concordia Library Citation and Style Guides
Advocacy and Support Services
Student Transition Centre
New Student Program
Access Centre for Students with Disabilities
Student Success Centre
The Academic Integrity Website
Financial Aid & Awards
Health Services