Titel des Vortrags

Name des Autors

Arheitsbereich Wissenschaftliches Rechnen Fachbereich Informatik Fakultät für Mathematik, Informatik und Naturwissenschaften Universität Hamburg

2015-01-01





Name des Autors Titel des Vortrags 1/23

Gliederung (Agenda)

- 1 The problem at hand
- 2 What is vectorization?
- 3 Vectorizing code
- 4 Conclusion
- 5 Literatur

Name des Autors Titel des Vortrags 2 / 23

The problem at hand

OO

Making code run faster

The Program:

Simulation/Game/Analytics which processes huge amounts of data. It is already written in an data oriented style.

The Problem:

The execution time is way to high.

What can we do?

Making code run faster

Steps of making code faster:

- reduce cash misses
- manual optimizations
- parallelization
- reduce overhead
- buying better hardware
- buying more hardware

Name des Autors Titel des Vortrags 4 / 23

Making code run faster

Steps of making code faster:

- reduce cash misses
- manual optimizations
- parallelization
- => vectorization <=</p>
- reduce overhead
- buying better hardware
- buying more hardware

Name des Autors Titel des Vortrags 5 / 23

What does vectorization mean?

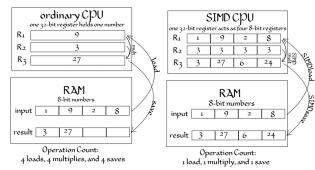
Vectorization

What is Vectorization? The use of a cpu's:

vector units

Name des Autors Titel des Vortrags 7 / 23

- special computation units
- every modern cpu implements them
- calculate multiple results from multiple inputs in one cycle



Name des Autors Titel des Vortrags 8 / 23

Vectorization

What is Vectorization? The use of a cpu's:

- vector units
- full vector registers

Name des Autors Titel des Vortrags 9/23

Vector Registers

(U)Int8x16	Lanes per type in a 128-bit SIMD register															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
(U)Int16x8	1		2		3		4		5		6		7		8	
(U)Int32x4 Float32x4	1 (x)				2 (y)				3 (z)				4 (w)			
Float64x2	1 (x)								2 (y)							

Titel des Vortrags Name des Autors 10 / 23

Vectorization

What is Vectorization?

The use of a cpu's:

- vector units
- full vector registers
- extended set of cpu instructions

Name des Autors Titel des Vortrags 11 / 23

Extended vector instructions

MOVAPS(x,y)z moves a memory line starting with x and with y size to vector register z MOV(x,y) moves single value from memory x into scalar register y

Name des Autors Titel des Vortrags 12 / 23

Instruction naming

Example:

movaps

mov = move

u = unaligned

p = packaged

s = single precision

Name des Autors Titel des Vortrags 13 / 23

avx/sse/avx512 different architectures provide different instruction sets (each new version introduced more) so older architectures do not have all instructions mention double precision instruction (when added)

Titel des Vortrags Name des Autors 14 / 23

What makes my code eligible for vectorization?

- calculations over arrays
- code must be in the innermost loop
- no if statements
- no uninlined function calls

Name des Autors Titel des Vortrags 15 / 23

How can I use vectorization?

The compiler does that for us if we tell him to. Example for gcc:

- gcc standard optimizations does not vectorize
- O3 enables auto vectorization
- -O3 does it by using the -ftree-vectorize flag
- -fopt-info-vec enables vectorization report

16 / 23 Name des Autors Titel des Vortrags

```
void test(float * vec1, float * vec2, float * res) {
    for (unsigned long i = 0; i < vector_size; i++) {
        res[i] += vec2[i] * vec1[i];
        res[i] /= vec2[i];
        res[i] -= vec1[i];
    }
}</pre>
```

■ TODO add restrict explanation(compiler checks for overlaping arrays -> more assem code) restrict can be dangerous since it trusts the programmer to be right. use with caution. While explaining show assembler code

```
void test(float *__restrict vec1, float *__restrict vec2, :
    for (unsigned long i = 0; i < vector_size; i++) {
       res[i] += vec2[i] * vec1[i];
       res[i] /= vec2[i];
       res[i] -= vec1[i];
    }
}</pre>
```

TODO add explanation for alignment (compiler does not know automatically how long a type is and checks for it resulting in more assembler code)

```
typedef float_32 attribute((aligned(32)))
void test(float_32 *_restrict vec1,
          float 32 * restrict vec2,
          float 32 * restrict res)
{
    for (unsigned long i = 0; i < vector size; i++) {
        res[i] += vec2[i] * vec1[i]:
        res[i] /= vec2[i]:
        res[i] -= vec1[i]:
```

Zusammenfassung

- Zusammenfassung 1
 - Unterpunkt 1
 - Unterpunkt 2
- Zusammenfassung 2
 - Unterpunkt 1
 - Unterpunkt 2
- Quelle: [?]

Name des Autors Titel des Vortrags 22 / 23

Literatur

Name des Autors Titel des Vortrags 23 / 23