Calculation of Total Integrated Noise in Analog Circuits

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***Abstract*—Electronic noise is a significant and fundamental issue in the design of analog circuits. In the widely used class of switched-capacitor circuits, the noise metric of interest is the so-called total integrated noise. Closed-form expressions for this quantity are unavailable in literature for all but the simplest circuit configurations that involve first- and second-order noise transfer functions. The lack of these expressions has prevented design automation and performance optimization without relying on repetitive simulations. In this paper we provide a general formula for calculating the total integrated noise in arbitrary circuits. The results are applied to two popular operational transconductance amplifier (OTA) circuits; a two-stage Miller-compensated architecture and a two-stage cascode-compensated topology. Simulations show that the calculated noise for these circuits is in close agreement with SPICE simulations.**

***Index Terms*—Thermal noise, total noise power, two-stage OTA.**

I. Introduction

ELECTRONIC noise poses a fundamental limitation on the performance of analog circuits. Thermal and flicker noise are two main noise sources in MOS circuits. Thermal noise is the output current fluctuation due to the random thermal motion of carriers in the channel. It has a Gaussian probability density function and a white power spectral density up to the terahertz frequency range. The channel noise is usually modeled as an equivalent current source between the drain and source terminals and its one-sided PSD in active region is approximately given by

$$S_{it}(f) = 4kT\gamma g_m \left(\frac{A^2}{Hz}\right) \tag{1}$$

where k is the Boltzmann constant, $k = 1.38 \times 10^{-23}$ J/K, T is the absolute temperature in degrees kelvin, γ is a coefficient equal to 2/3 for long channel devices [1] and g_m is the transconductance of the transistor. Flicker noise can be modeled by adding another current source. Yet it is often negligible and can be handled following the presented approach with small modifications.

In order to obtain the electronic noise at the component level, the transfer function of each noise source to the output must be calculated. The total integrated noise is then found by integrating the product of the noise PSD with the magnitude square of the noise transfer function (NTF):

$$N_x = \int_0^\infty S_x(f)\left|H_x(f)\right|^2 df. \tag{2}$$

The same calculation applies to sampled noise in switched-capacitor (SC) circuits where the noise is shaped by a filter and is sampled on a capacitor at the output [2]. Discrete-time noise samples are essentially instantaneous values of a continuous-time noise process. Therefore, the sampled noise has the same mean-square value as the continuous noise that is given by the above integral.

For a first- or second-order NTF the integral in (2) can be solved using the following equations [3]:

$$\int_0^\infty \left|\frac{1}{1+\frac{s}{\omega_0}}\right|^2 df = \frac{\omega_0}{4} \tag{3}$$

$$\int_0^\infty \left|\frac{1}{1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}}\right|^2 df = \frac{\omega_0 Q}{4} \tag{4}$$

$$\int_0^\infty \left|\frac{\frac{s}{\omega_0}}{1+\frac{s}{\omega_0 Q}+\frac{s^2}{\omega_0^2}}\right|^2 df = \frac{\omega_0 Q}{4}. \tag{5}$$

However, a problem arises with the calculation of higher order integrals that do not have closed-form solutions available. Many practical circuits of interest cannot be represented accurately by a second-order approximation. Therefore this approach has had limited practicality and exact noise power can only be obtained from simulations. This dependence on simulation is especially prohibitive in equation-based optimization of circuits [4] where we need to have a self-contained set of equations that can reliably describe the circuit.

In this paper, the solution to the general noise power integral is derived. Section II gives the mathematical solution of the integral. Section III considers two popular OTA architectures and derives equations for the noise power of individual elements. Throughout the paper, noise sources are limited to the thermal noise of resistors and active transistors. The contribution of load transistors is neglected for the sake of simplicity.

II. Calculation of $\int_0^\infty \left|N(s)/D(s)\right|^2 df$

In calculating such improper integrals, we make use of the residue theorem [5] which states that: If $f(z)$, a function of a complex variable z, is regular within a closed contour C except at a finite number of poles, then:

$$\oint_C f(z)dz = 2\pi j \sum \text{Residues of f(z) within C} \tag{6}$$

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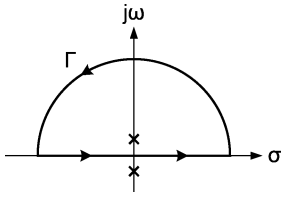

Fig. 1. Integral contour in complex plane.

where the integral is taken counterclockwise around C.

Dealing with rational functions of polynomials, a function is regular at all points except the roots of its denominator. According to the residue theorem, the integral around a closed path is equal to $2\pi j$ times the sum of residues calculated at the denominator poles that lie within the area. A residue associated with a simple pole can be calculated from:

$$\mathrm{Res}\frac{N(z)}{D(z)}\Big|_{z=p} = \frac{N(p)}{\frac{dD}{dz}\Big|_p}. \tag{7}$$

As an example, suppose we want to calculate $I_0 = \int_0^\infty 1/(1+x^2)dx$. To make use of the residue theorem we should convert the line integral to one around a closed contour. We, therefore, complete the integral along the real axis by a very large semicircle such that the integral along this semicircle vanishes (Fig. 1). Therefore:

$$\oint_C \frac{1}{1+z^2}dz = \int_{-\infty}^{\infty}\frac{1}{1+x^2}dx + \underbrace{\int_\Gamma \frac{1}{1+z^2}dz}_{0}. \tag{8}$$

The integrand has simple poles at $z = \pm j$, and at the pole *within* the contour at $z = j$ the residue is computed from (7) as $1/(2j)$. Hence

$$2I_0 = \int_{-\infty}^{\infty}\frac{1}{1+x^2}dx = 2\pi j\cdot\frac{1}{2j} = \pi \Rightarrow I_0 = \frac{\pi}{2}. \tag{9}$$

Likewise, we can write:

$$I = \int_0^\infty \left|\frac{N(s)}{D(s)}\right|^2 df = \frac{1}{2}\frac{2\pi j}{2\pi}\sum_{\omega_i}\mathrm{Res}\frac{N(j\omega)N(-j\omega)}{D(j\omega)D(-j\omega)} \tag{10}$$

where $s = j\omega = j2\pi f$ and $1/2\pi$ is added since integration is with respect to f rather than ω.

The ω_i's are those poles of the denominator $D(j\omega)D(-j\omega)$, that lie in the upper half plane. The problem is that the denominator might not have closed-form solution for its poles. However, we note that if ω_i is a pole in the upper half plane, then $s_i = j\omega_i$ is equivalent to rotating ω_i counterclockwise by 90° and thus lies in the left half plane. We should, therefore, find the roots of $D(s)D(-s)$ that lie in the LHP. Yet, the roots of $D(s)$ are the roots of the characteristic equation or the closed-loop poles and lie in the LHP for a stable circuit. The roots of $D(-s)$ on the other hand, all lie in the RHP. The residues are therefore the solutions of $D(j\omega) = 0$.

Using (7) we can calculate the residues as

$$\begin{aligned}&\mathrm{Res}\left[\frac{N(j\omega)N(-j\omega)}{D(j\omega)D(-j\omega)}\right]_{\omega_i}\\ &= \frac{N(j\omega_i)N(-j\omega_i)}{\frac{d}{d\omega}\left[D(j\omega)D(-j\omega)\right]_{\omega_i}}\\ &= \frac{N(j\omega_i)N(-j\omega_i)}{j\left[D'(j\omega)D(-j\omega) - D(j\omega)D'(-j\omega)\right]_{\omega_i}}\\ &= \frac{N(j\omega_i)N(-j\omega_i)}{j[D'(j\omega_i)D(-j\omega_i)]} \triangleq \frac{F(\omega_i)}{G(\omega_i)}.\end{aligned} \tag{11}$$

Combining (10) and (11) we can write:

$$I = \frac{j}{2}\sum_{i=1}^{n}\frac{F(\omega_i)}{G(\omega_i)}. \tag{12}$$

Here we will provide a general method to calculate the above expression. Before we get to the main path, a few simple theorems are presented. At the end of this section, we will use these to provide a closed-form solution of (2).

From linear algebra we know that if a square matrix $A \in \mathbf{R}^{n\times n}$ has n distinct eigenvalues, then it is diagonalizable and can be written in the form [6]:

$$A = T\Lambda T^{-1} \tag{13}$$

where Λ is a diagonal matrix containing the (sorted) eigenvalues of A and T is the matrix whose columns are the (normalized) eigenvectors of A, arranged to match the order of their corresponding eigenvalues in Λ.

Diagonalization greatly assists in matrix calculations

$$\begin{aligned}A^k &= \left(T\Lambda T^{-1}\right)^k = T\Lambda T^{-1}T\Lambda T^{-1}\cdots T\Lambda T^{-1}\\ &= T\Lambda^k T^{-1} = T\mathbf{diag}(\lambda_1^k,\ldots,\lambda_n^k)T^{-1}.\end{aligned} \tag{14}$$

Similarly for any analytic function f that is given by power series:

$$f(x) = \sum_i a_i x^i \tag{15}$$

we can write

$$f(A) = Tf(\Lambda)T^{-1} = T\mathbf{diag}\left(f(\lambda_1),\ldots,f(\lambda_n)\right)T^{-1} \tag{16}$$

where we have overloaded f to denote both a scalar function $f:\mathbf{R}\to\mathbf{R}$ and a matrix function $f:\mathbf{R^{n\times n}}\to\mathbf{R^{n\times n}}$, the choice of which is determined from the context.

The trace of a product of square matrices stays the same under any cyclic permutations of the matrices. Therefore

$$\begin{aligned}\mathbf{Tr}(f(A)) &= \mathbf{Tr}(Tf(\Lambda)T^{-1}) = \mathbf{Tr}(T^{-1}Tf(\Lambda))\\ &= \mathbf{Tr}(f(\Lambda)) = \sum_{i=1}^{n} f(\lambda_i).\end{aligned} \tag{17}$$

Consequently, the trace of a matrix function is equal to the sum of the function at the eigenvalues of the matrix. On the other

hand, we proved in (12) that the noise integral is proportional to the sum of a rational function at the poles of the circuit. To link the above two results we only need to find a matrix with the system poles as its eigenvalues. Not surprisingly, a matrix is already identified with this property. For every monic polynomial $p(t) = c_0 + c_1 t + \ldots + c_{n-1}t^{n-1} + t^n$ its so-called *companion* matrix is defined as:

$$C(p) = \begin{bmatrix} 0 & 0 & \ldots & 0 & -c_0 \\ 1 & 0 & \ldots & 0 & -c_1 \\ 0 & 1 & \ldots & 0 & -c_2 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \ldots & 1 & -c_{n-1} \end{bmatrix}. \tag{18}$$

The characteristic polynomial of C is equal to p, so its eigenvalues are the roots of $p(t) = 0$ [6]. The companion matrix associated with a transfer function in an electric circuit can be found from its denominator polynomial and in our case from the denominator of the noise transfer function in (10).

Next we expand $D(s)$ in terms of ω and normalize to get a leading coefficient of one

$$\begin{aligned} D(s) &= \sum_{i=0}^{n} d_i s^i = \sum_{i=0}^{n} d_i (j\omega)^i = \sum_{i=0}^{n} a_i \omega^i \\ &= a_n \left(\frac{a_0}{a_n} + \frac{a_1}{a_n}\omega + \cdots + \frac{a_{n-1}}{a_n}\omega^{n-1} + \omega^n \right) \end{aligned} \tag{19}$$

where $a_i \triangleq j^i d_i$

The companion matrix of the circuit is:

$$C(D) = \begin{bmatrix} 0 & 0 & \ldots & 0 & -\frac{a_0}{a_n} \\ 1 & 0 & \ldots & 0 & -\frac{a_1}{a_n} \\ 0 & 1 & \ldots & 0 & -\frac{a_2}{a_n} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \ldots & 1 & -\frac{a_{n-1}}{a_n} \end{bmatrix}. \tag{20}$$

To find the noise integral, we take $f \triangleq F/G$ and $A = C(D)$. Therefore:

$$\begin{aligned} \mathbf{Tr}(f(A)) &= \mathbf{Tr}\left(G^{-1}(C)F(C)\right) \\ &= \sum_{i=1}^{n} \frac{F(\lambda_i)}{G(\lambda_i)} = \sum_{i=1}^{n} \frac{F(\omega_i)}{G(\omega_i)}. \end{aligned} \tag{21}$$

Finally combining (10) and (21) we summarize the result of our derivation in Fig. 2. The integrals corresponding to third- and fourth-order transfer functions are also derived and presented in (22) and (23), respectively, shown at the bottom of the page. These examples will be applied to two example circuits in the next section.

$$I_n = \int_0^\infty \left|\frac{N(s)}{D(s)}\right|^2_{s=j\omega} df = \frac{j}{2}\mathbf{Tr}\left(G^{-1}(C)F(C)\right)$$

where:

$$\begin{aligned} F(\omega) &= N(j\omega)N(-j\omega) \\ G(\omega) &= j[D'(j\omega)D(-j\omega)] \end{aligned}$$

$$C = \begin{bmatrix} 0 & 0 & \ldots & 0 & -a_0/a_n \\ 1 & 0 & \ldots & 0 & -a_1/a_n \\ 0 & 1 & \ldots & 0 & -a_2/a_n \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \ldots & 1 & -a_{n-1}/a_n \end{bmatrix}, \quad a_i = j^i d_i$$

and d_i's are the coefficients of D: $D = \sum_{i=0}^{n} d_i s^i$

Fig. 2. Algorithm for calculating the integral I_n.

As a final remark, note that in the derivation we have implicitly assumed the circuit has simple poles. First, (7) does not hold for poles of higher multiplicities. Instead, the residue of a function f at a pole of order $n > 1$ can be found by

$$\text{Res f(z)}\big|_{z=p} = \frac{1}{(n-1)!}\lim_{z\to p}\left(\frac{d}{dz}\right)^{n-1}\left((z-p)^n f(z)\right). \tag{24}$$

Thus we should construct a separate expression for such poles and the integral can not be written in the form of a single sum as in (12). Secondly, diagonalization in the form (13) may not be possible when the poles are not simple. Although this later limitation can be bypassed by using a more general matrix decomposition, the former is essential to our approach. Yet note that a higher order pole can be regarded as the limiting case of simple poles with infinitesimal distances. Furthermore the noise integral is a physical quantity and can not have singularity. Therefore the result derived from our approach in the limit (or after cancelling common terms in the numerator and denominator) is also valid for the case with non-simple poles.

III. Noise Analysis of Two-Stage OTA

Next the calculation of total integrated noise in analog circuits will be discussed. As an example, two popular OTAs (two-stage, Miller- and cascode-compensated) in feedback configuration are considered. Noise contribution of individual components are derived and the obtained results are verified with simulation. In calculating the transfer function of noise sources to the output, equivalent half-circuit models are used. A general discussion about the scope of validity of half-circuit method is presented in the Appendix .

A. Miller-Compensated OTA

The Miller-compensated OTA uses a resistor in series with the compensation capacitance to eliminate the right half-plane zero

$$I_3 = \int_0^\infty \left|\frac{n_2 s^2 + n_1 s + n_0}{d_3 s^3 + d_2 s^2 + d_1 s + d_0}\right|^2_{s=j\omega} df = \frac{1}{4}\,\frac{n_2{}^2 d_1 d_0 + n_1{}^2 d_3 d_0 + n_0{}^2 d_3 d_2 - 2\,n_2\,n_0\,d_3\,d_0}{d_3\,(d_2\,d_1 - d_3\,d_0)\,d_0} \tag{22}$$

$$I_4 = \frac{1}{4}\frac{n_3^2 d_3 d_0^2 + 2n_3 n_1 d_4 d_1 d_0 - n_3^2 d_2 d_1 d_0 - n_2^2 d_4 d_1 d_0 - n_1^2 d_4 d_3 d_0 - n_0^2 d_4 d_3 d_2 + 2n_2 n_0 d_4 d_3 d_0 + n_0^2 d_4^2 d_1}{d_4(d_4 d_1^2 - d_3 d_2 d_1 + d_3^2 d_0) d_0}. \tag{23}$$

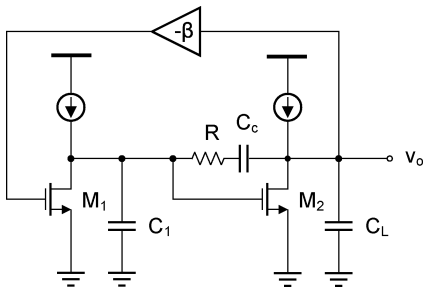

Fig. 3. Two stage Miller-compensated OTA with feedback factor β.

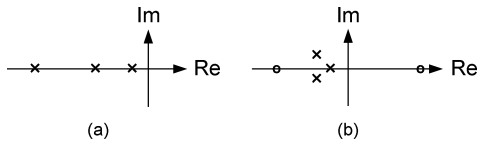

Fig. 4. Closed-loop pole–zero plots of (a) Miller-compensated and (b) cascode-compensated OTAs in the s-plane.

[7], as shown in Fig. 3. It has two split-apart poles at the output of each stage and another pole due to the series RC branch. A plot showing the position of closed loop poles is shown in Fig. 4(a). A closer inspection reveals additional nondominant poles/zeros but usually considering those mentioned above is enough to describe the circuit behavior or to design it.

The contribution of each noise source is obtained by integrating the magnitude square of its corresponding transfer function to the output. For example to find the noise due to M_1 we should evaluate the integral in (25), shown at the bottom of the page. Answers follow from the formulae we derived in the previous section and are given below. N_1 and N_2 denote the noise of M_1 and M_2 respectively and N_3 is the noise power of the resistor.

$$\Delta \triangleq C_cC_L + C_cC_1 + C_LC_1 \tag{26}$$

$$D \triangleq \beta g_{m1}g_{m2}RC_c(C_1 + C_L) + (g_{m2} - \beta g_{m1})\Delta \tag{27}$$

$$N_1 = \frac{kT\gamma}{\beta C_cD}\left[g_{m2}\Delta + \beta g_{m1}C_c^2(1 - g_{m2}R)^2\right] \tag{28}$$

$$N_2 = \frac{kT\gamma g_{m2}}{C_cC_LD}\left[C_L(C_1 + C_c)^2 + RC_1C_c^2(g_{m2} - \beta g_{m1} + \beta g_{m1}g_{m2}R)\right]$$

$$N_3 = \frac{kT\gamma C_c}{C_LD}\left[\beta g_{m1}g_{m2}RC_1 + g_{m2}^2RC_L + g_{m2}C_1 - \beta g_{m1}C_1\right]. \tag{29}$$

The circuit also has a zero which can be moved to infinity by setting $R = 1/g_{m2}$. In this case the above results simplify to

$$D \triangleq g_{m2}\Delta - \beta g_{m1}C_1C_L \tag{30}$$

$$N_1 = \frac{kT\gamma g_{m2}\Delta}{\beta C_cD} \tag{31}$$

$$N_2 = \frac{kT\gamma g_{m2}\left[C_L(C_1 + C_c)^2 + C_1C_c^2\right]}{C_cC_LD} \tag{32}$$

$$N_3 = \frac{kT\gamma g_{m2}C_c(C_1 + C_L)}{C_LD}. \tag{33}$$

It is seen from (30) that the noise expressions will go negative if $\beta g_{m1}C_1C_L$ becomes larger than $g_{m2}\Delta$. Clearly a negative result cannot be true since we have calculated the total noise power which is greater than zero. In fact, the negative sign stems from the potential instability of the circuit and is the case with every noise expression in feedback circuits of orders greater than one. Whenever the total phase shift around the loop reaches 0 and the loop gain is larger than 1, the noise at that frequency builds up and makes the circuit unstable. For the case of Miller-compensated OTA, this happens when $D = 0$, which makes the noise power infinite. Beyond that, the circuit is unstable and the equation does not hold. Therefore, the denominator of every noise expression represents a stability condition for the circuit. The same condition can also be derived by applying the Routh-Hurwitz stability criterion to the characteristic equation of the circuit.

In the Miller-compensated OTA the first stage often exploits a cascode transistor to boost the gain and improve the frequency response. At low frequencies (compared to the device transit frequency) the cascode transistor is degenerated by the input stage and has very low gain and therefore negligible noise contribution. At high frequencies the parasitic capacitances at the source of the cascode device reduce the degeneration but the dominant pole at the output of the first stage filters the noise. Hence the cascode noise at the output is typically low across the whole frequency range and the results from Fig. 3 apply to the cascoded architecture as well.

B. Cascode-Compensated OTA

The cascode-compensated architecture utilizes a common gate transistor to mitigate the impact of the RHP zero [8]. This transistor blocks the feed-forward path to the output and creates a unilateral feedback through the compensation capacitor.

There is no need to use an explicit common gate stage to do the task because it can be superimposed on the cascode transistor already embedded in the first stage [9], as illustrated in Fig. 5. The compensation capacitor provides a direct path from the input to the output and unless the cascode transistor has infinite transconductance, some of the input signal flows to the output via C_c and forms a zero. However, a closer inspection reveals that the circuit actually has two symmetric zeros at high frequencies that cancel the phase of one another and therefore do not degrade the stability. The circuit also has a real dominant

$$N_1 = \int_0^\infty \left| \frac{4kT\gamma g_{m1}\left[(g_{m2}R - 1)C_cs + g_{m2}\right]}{RC_cC_LC_1s^3 + (C_LC_1 + C_cC_L + C_cC_1)\,s^2 + (g_{m2}C_c - \beta g_{m1}C_c + \beta g_{m1}g_{m2}RC_c)\,s + \beta g_{m1}g_{m2}} \right|_{s=j2\pi f}^2 df. \tag{25}$$

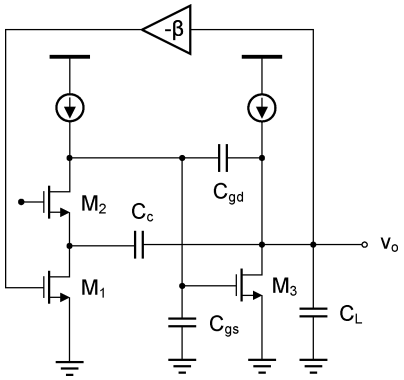

Fig. 5. Two-stage cascode-compensated OTA with feedback factor β.

pole as well as a pair of complex conjugate poles, as shown in Fig. 4(b). This circuit is usually designed in the time domain where the position of the poles are directly determined from the settling requirements [10]. It has one noise source less than the cascoded Miller-compensated architecture. However the noise of the cascode transistor is not negligible as in the Miller circuit.

The choice of the parasitics to include in the model, depends on the relative magnitude of circuit elements and the accuracy we wish to achieve. Here, the parasitic capacitances at the output of the first stage and the gate-drain capacitance of M_3 are included. The capacitance at the drain of M_1 is neglected because C_c is usually much larger and will dominate the conductance at that node. The circuit has four capacitances three of which form a loop; thereby constituting a third-order system. The total noise power of the three transistors are presented below in (34)–(38).

$$\Delta \triangleq C_{gs}C_L + C_{gs}C_{gd} + C_L C_{gd} \tag{34}$$

$$D \triangleq \beta\Delta\Big\{C_{gd}(g_{m3}-\beta g_{m1})\Big[C_c\big[C_{gd}(g_{m3}-\beta g_{m1})+g_{m3}C_c\big] + \beta g_{m1}\Delta\Big] + (g_{m2}-\beta g_{m1})(\Delta + C_{gs}C_c)\big[\beta g_{m1}C_c + (g_{m3}-\beta g_{m1})(C_{gd}+C_c)\big]\Big\} \tag{35}$$

$$N_1 = \frac{kT\gamma}{D}\Big\{C_c\Big\{(C_{gd}+C_{gs})\Big[\beta g_{m1}g_{m3}\big[\Delta + C_{gd}(C_c+C_{gs}+C_{gd}) + C_cC_{gs}\big] - g_{m1}^2(\beta^2C_{gd}^2+\beta^2C_{gd}C_{gs}) + g_{m3}^2C_{gd}C_L + g_{m2}g_{m3}C_{gs}C_L\Big] + g_{m3}C_{gs}C_{gd}(g_{m3}C_{gd}+g_{m2}C_{gs})\Big\} + g_{m2}\Delta(g_{m3}\Delta + \beta g_{m1}C_{gd}^2)\Big\} \tag{36}$$

$$N_2 = \frac{kT\gamma\beta C_c}{D}\Big[g_{m2}C_{gs}^2\big[(g_{m3}-\beta g_{m1})C_{gd}+g_{m3}C_c\big]+g_{m3}^2C_c\Delta\Big] \tag{37}$$

$$N_3 = \frac{kT\gamma\beta g_{m3}}{D}(C_{gd}+C_{gs})^2\Big[C_c\big[C_{gd}(g_{m3}-\beta g_{m1})+g_{m3}C_c\big] + g_{m2}\Delta\Big]. \tag{38}$$

C. Noise Analysis Example

The derived expressions are applied in a numerical example using BSIM3v3 models. The transistors in the first stage have a current of 1 mA and an aspect ratio of 1000 μm/0.35 μm. The transistor in the second stage has a current of 2 *mA* and an aspect ratio of 2000 μm/0.35 μm. The resistor in the Miller-compensated OTA is taken to be $1/g_{m2} \approx 25\ \Omega$. Also $C_L = 1$ pF, $C_c = 5$ pF and $\beta = 0.25$ are used. For simplicity, an ideal VCVS is used to implement the feedback network. The results from SPICE simulations and hand calculations are summarized in Table I. Output noise running integrals for individual noise sources are shown in Fig. 6(a) and (b). The total integrated noise is the terminal value of the curves as f tends to infinity. For comparison, the total integrated noise obtained by calculation is also shown with straight lines. It is seen that the derived equations are in good agreement with simulation results. The most significant discrepancy is a 26% error in N_2 for the cascode-compensated circuit. We may improve the accuracy by including the junction capacitance at the drain of M_1, its gate-drain capacitance and finally the finite output resistances of the transistors. However the difference constitutes a small part of the overall noise and the improved accuracy is not worth the extra work.

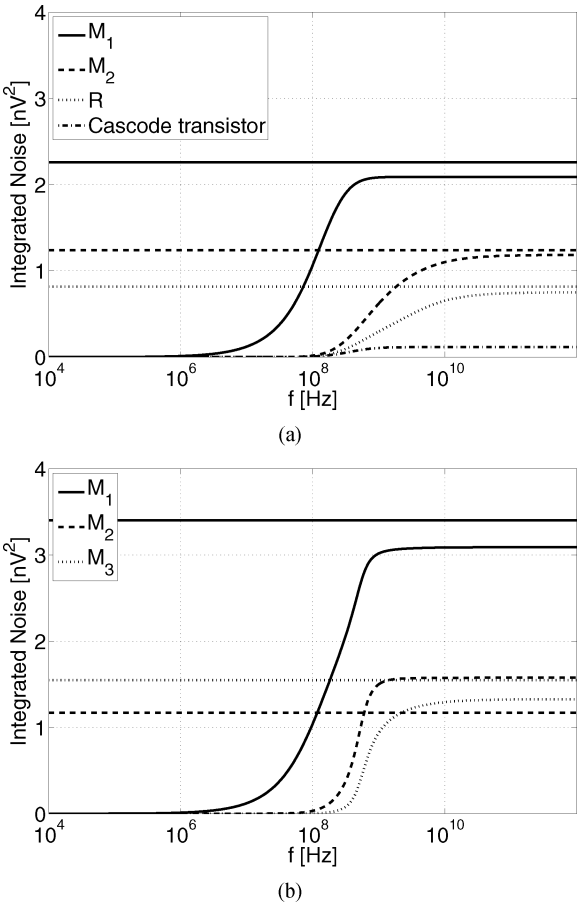

Fig. 6. Curves show the simulated output noise running integrals and the lines show the calculated total integrated noise values. (a) Miller-compensated OTA noise plot. (b) Cascode-compensated OTA noise plot.

IV. Conclusion

Accurate calculation of various circuit specifications can aid in more intelligent and efficient designs. One of the least polished equations in circuits is the one for the total integrated noise that is needed for example in SC circuits. Noise calculations even in the most widely used and recognized amplifiers involve complicated algebra. In this paper the required formulae

TABLE I
TWO-STAGE OTA NOISE EXAMPLE (NUMBERS ARE IN nV^2).

	Element	M1	M2	M3	R
Miller-Compensated	SPICE	2.09	1.18	–	0.751
	Calculation	2.26	1.24	–	0.815
Cascode-Compensated	SPICE	3.09	1.58	1.33	–
	Calculation	3.40	1.17	1.55	–

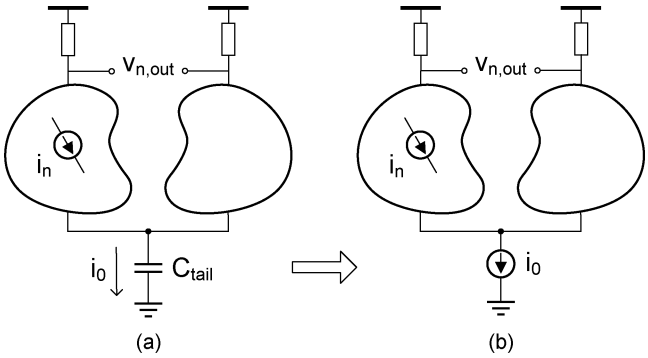

Fig. 7. Validity of half-circuit method in noise analysis.

for a general circuit were derived. Obtained results for two circuit examples are found to closely match the results from SPICE simulations.

APPENDIX
NOISE ANALYSIS OF DIFFERENTIAL CIRCUITS

It seems quite natural to apply the half-circuit concept to calculate various noise transfer functions in differential circuits. However the validity of this approach deserves a careful look. Since the noise sources in each half are uncorrelated their effects on the tail node are not cancelled out and the assumption of virtual ground is no longer true. However as shown below if the circuit is symmetric and is sensed differentially, then a half-circuit analysis yields correct results.

Consider Fig. 7(a) where we want to find the differential output voltage due to a single source i_n (the dc tail current source is not shown). Suppose a current i_0 goes to ground at the tail node, for instance due to the capacitance at that node. From the substitution theorem [11] we know that the circuit essentially remains the same if we substitute the path to ground with a current source i_0, as shown in Fig. 7(b). Now there are two sources in the circuit: The original source i_n and a controlled source i_0 that depends on i_n as well as the circuit topology. If the circuit is linear, we can use the superposition theorem and find the output voltage by adding up their individual effects. However, since i_0 is common mode, it will not produce any differential output. Therefore the value of i_0 or the impedance at the tail node do not affect the differential output voltage. A larger tail capacitance drains more current into ground and reduces the output voltage at the right branch, but it also increases the output voltage at the left branch such that the total differential voltage remains the same. In the limit when $C_{tail} \rightarrow \infty$ we may directly connect the tail node to ground. In this case the circuit is divided into two half-circuits and the differential output follows from the single-ended output. This proof only uses the linearity and the symmetry of the circuit and is otherwise general. For example i_n can be a noise source, a deterministic input, an equivalent source representing offset, etc. In general, to use the concept of half-circuits for calculating the differential output voltage it is not necessary to have a virtual ground at the tail node.

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