High slew rate two stage A/AB and AB/AB op-amps with phase lead compensation at output node and local common mode feedback

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***Abstract*—Class A/AB and class AB/AB two stage op-amps with very high and symmetrical slew rate are introduced. They use output dominant pole with phase lead compensation. Resistive local common mode feedback is used to achieve a class AB output stage. One of the architectures uses also a class AB pseudo-differential pair to achieve class AB operation in the input stage. Experimental results verify slew rate enhancement factors of 12 and 50 for the A/AB and AB/AB circuits respectively. This is achieved with same bandwidth and noise and very small additional quiescent power dissipation or hardware complexity.**

I. INTRODUCTION

In some applications like in Low Dropout (LDO) regulators [1] two stage op-amps with a dominant output pole are used as shown in Fig. 1a,b. The dominant pole is given in this case by $\omega_{pout}=1/[C_L(r_{o5}||r_{o6})]$. Phase lead compensation by means of a series resistor R_c is commonly used to create a left half plane zero at a frequency $\omega_{pz}=1/(R_cC_L)$. The zero compensates (partially) for the phase shift of the internal non dominant pole of the op-amp that has a value $\omega_{px}=1/[C_x(r_{o3,4}||r_{o1,2})]$.Where C_x is the parasitic capacitance at nodes x, x'. Phase lead compensation is required since these nodes are high impedance nodes and have poles ω_{px} that could cause unstable behavior. The conventional class A two stage op-amp (Fig. 1b) is characterized by a highly asymmetrical slew rate with the negative slew rate given by $SR=2I_B/C_L$ where I_B is the bias current. Slew rate can only be increased in class A op-amps by increasing the I_B (and consequently the static power dissipation) of the output stage. Many two stage op-amps with class AB output stage have been reported that are characterized by relatively modest effective slew rate improvement factors [2]-[4]. They require additional complex circuitry, and/or non-negligible additional static power dissipation, or increased supply voltages and/or PSRR degradation [5]. Local common mode feedback (LCMFB) consists of introducing resistors R connected between the drain and gate terminals of the load transistors as shown in Fig. 1c [6]. It provides class AB behavior to the shell formed by M5-M8 in one stage op-amps (OTAs). It enhances slew rate by increasing significantly the maximum swing at internal nodes x,x' of the OTA. It has the added advantage that it reduces the parasitic capacitance of the internal nodes of the op-amp [7] and increases for this reason the phase margin. This is due to the fact that with LCMFB the common gate node of the load transistors M3-M4 is signal grounded so that their gate-source capacitances do not contribute to C_x. The gain in the first stage is given by $A_I=g_{m1,2}(R||r_{o3,4})$ while the gain of the second stage is given by $A_{II}=g_{mout}\ (r_{o5}||r_{o6})$. In an one stage op-amp the local common mode feedback resistors R has a low value so that the first stage has close to unity gain $A_I\sim g_{m1,2}R\sim1$ The internal pole $\omega_{px}=1/(C_xR)$ is in this case a very high frequency pole and most of the open loop gain is achieved in the output node $A_{ol}=A_{II}=g_{m1,2}R_{out}$. A drawback of one stage op-amps based on this technique is that only relatively low open loop gains are possible since inclusion of output cascoding transistors to increase R_{out} (and A_{ol}) limits also seriously the maximum output current and with this the slew rate enhancement factor. This circuit is not capable of

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driving resistive loads due to the gain degradation caused by them. In this paper we discuss a two stage op-amp counterpart to the "super" OTA reported in [8] which has the same architecture of an OTA using resistive LCMFB. The main difference being that the value of R is selected so that gain is also provided in the first stage. This leads to high open loop gain, with very high and symmetrical slew rate, high output swing, low supply requirements and capability to drive resistive loads. We show that in spite of the fact that inclusion of a large resistor R to boost the open loop gain the op-amp decreases the internal pole f_{px} the op-amp can still have a stable behavior for moderate capacitive loads if phase lead compensation is used.

II. SUPER CLASS AB TWO STAGE OP-AMP

Fig. 1b shows the architecture of the first proposed two stage op-amp denoted here A/AB op-amp. It has the same architecture of the one stage op-amp with LCMFB reported in [7]. The difference is that in this case high values are selected for resistors R comparable to the output resistance of an MOS transistor $R \sim r_o$ This is done to increase the open loop gain of the op-amp so that it performs as a two stage op-amp. This as opposed to the op-amp of [7] where the values of $R \sim 1/g_m$ lead to close to unity gain in the first stage so that it performs as a one stage op-amp. The drawback is that the internal non-dominant pole f_{px} reduces its value causing potential instability but on the other hand given that LCMFB also reduces the effective parasitic capacitance at nodes x, x' and that phase lead compensation is used, the op-amp can remain stable even with relatively low load capacitances A simple analysis follows:

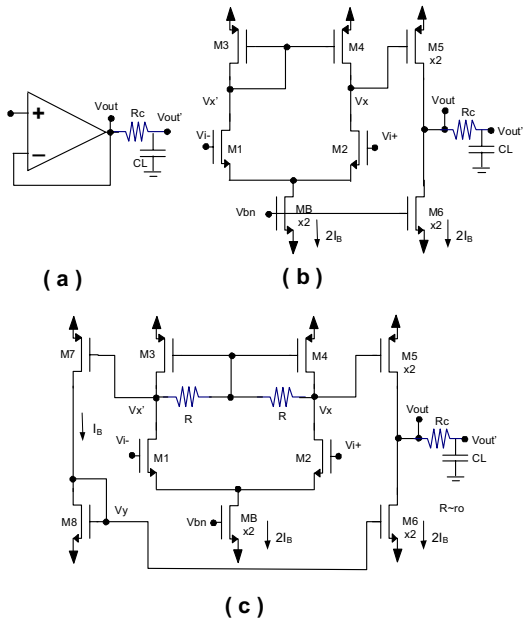

Fig. 1 (a) Op-amp with output dominant pole and phase lead compensation connected as voltage follower, (b) Conventional class A/A two stage op-amp (c) proposed class A/AB two stage op-amp with resistive local common mode feedback in input stage

The open loop gain of the op-amp is given by

$$A_{ol}=g_{m1,2}Rg_{m5,6}(r_{o5}||r_{o6}) \quad (1)$$

The dominant output pole is

$$\omega_{pout}=1/[C_L(r_{o5}||r_{o6})] \quad (2)$$

The gain bandwidth product (in rad/s) is

$$GB= g_{m1,2}Rg_{m5,6}/C_L \sim g_{m1,2}r_o g_{m5,6}/C_L \quad (3)$$

The non-dominant pole ω_{px} and half plane zero ω_z are given by

$$\omega_z=1/R_cC_L \text{ and } \omega_{px}=1/(C_xR||r_{o3,4}). =2/(C_xr_o) \quad (4)$$

The condition for pole zero cancellation is to select following value for R_c

$$R_c= r_oC_x/(2C_L) \quad (5)$$

This condition can only be satisfied approximately given that all parameters are uncorrelated but in practice even if a relatively large mismatch (say 20%) between ω_{px} and ω_z exists partial cancellation allows to achieve high phase margin with large gain bandwidth products.

The quiescent voltage drop across resistors R is zero and the voltage at nodes x,x' sets accurately the quiescent current in M7-M8 to a value I_B (or $2I_B$ in M5-M6, this assumes matched transistors). The selection of a large value for $R \sim r_o$ leads to large swing at nodes x,x' so that under dynamic conditions the currents in the shell formed by M5-M8 can be essentially larger than the quiescent current I_B.

Fig 2a shows a modification of the circuit of Fig. 1b denoted here AB/AB op-amp that uses a pseudo class AB differential pair and. In this circuit the source node V_z has very low impedance node ($R_z=1/[g_m(g_mr_o)^2] \sim 1\Omega$) . The voltage at V_z follows the common mode input voltage variations. This is achieved by means of a circuit denoted cascoded flipped voltage follower (CASFVF) [9]-[10] formed by MFVF, MB and MCS. The input common mode voltage V_{iCM} is sensed using a continuous-time capacitive averaging network formed by two capacitors with value C (shown in Fig. 2a). V_{iCM} is applied to the gate of MFVF. This causes gate source variations in M1 and M2 with equal and opposite values $V_{GS1,2}=V_{GSQ} \pm V_d/2$ and lead to class AB operation with currents

$$I_{d1,2}=(\beta/2)[(V_{GSQ}-V_T)^2 \pm V_d(V_{GSQ}-V_T) +(V_d/2)^2] \quad (6)$$

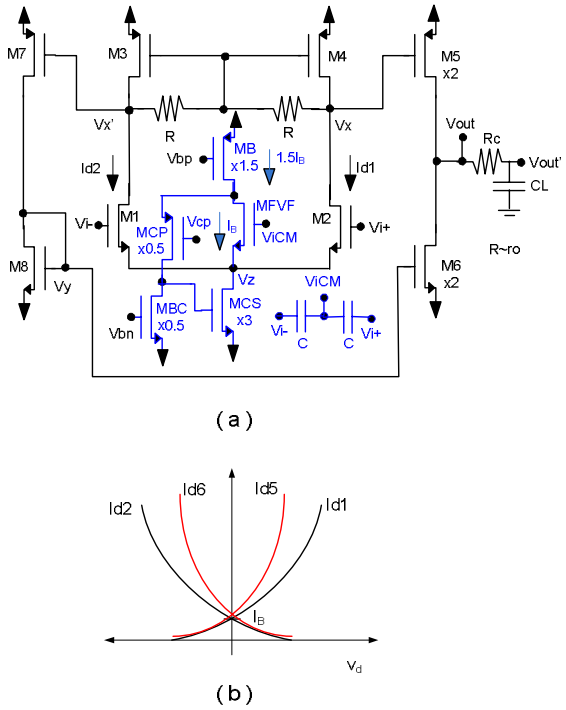

Fig. 2 (a) Two stage uncompensated op-amp with local common mode feedback and class AB input differential stage (b) DC transfer characteristic of input and output stages.

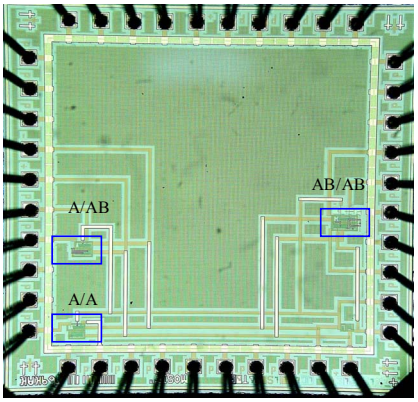

Fig. 3 Micrograph of fabricated test chip

Where $I_{d1,2}$ can take values much higher than the quiescent current I_B as shown in Fig. 2b. Besides providing Class AB operation to the input stage the CASFVF does not degrade the common mode rejection as it is the case for pseudo differential class AB input stages where the common source node is tied directly to a low impedance node. In this case common mode input voltage variations lead to large variations

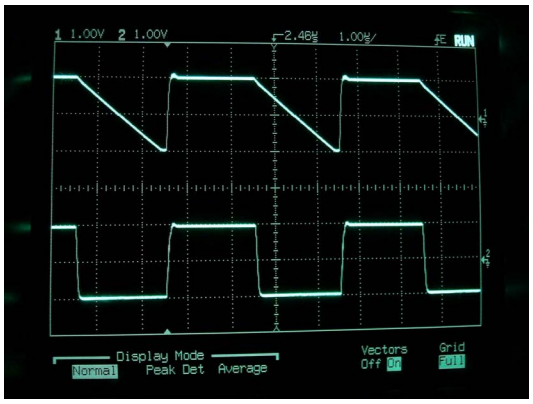

Fig. 4 Experimental pulse response of circuits of Figs 1a and 1b with CL=80pF: Top Trace: Conventional two stage op-amp of Fig. 1a. Bottom trace Proposed class A/AB two stage op-amp of Fig. 1b with R=50kΩ. Horizontal axis:1µs/div, vertical axis: 1V/div.

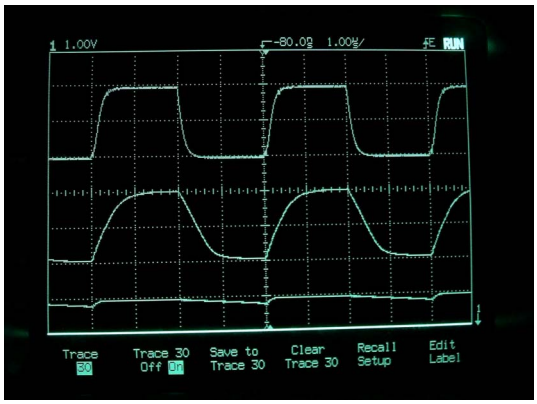

Fig. 5 Experimental response of circuits of Figs. 1a (bottom trace), 1b (middle trace) and 2 (top trace) with C_L=500pF and 250kHz $2V_{pp}$ input pulse

in I_{d1},I_{d2}. This does not take place in the input stage of Fig. 2b given that node V_z follows input common mode voltage variations. For this reason the CMRR of the input stage of Fig. 2b is similar to the CMRR of a conventional differential input stage. The output stage currents $I_{d5,6}$ of the circuit of Fig. 2a are further enhanced with respect to $I_{d1,2}$ by the large signal swing caused by the resistive LCMFB at nodes V_x, $V_{x'}$. The combined effect of class AB operation of the input differential stage and LCMFB in the AB/AB circuit of Fig. 2a leads to output currents $I_{out}=I_{d5}-I_{d6}$ that are much larger than in the A/AB circuit of Fig. 1b and essentially larger than the class A/A circuit of Fig. 1a as shown by the experimental results of following section. The total quiescent currents of the circuits of Fig1a, 1b and 2a are $4I_B$, $5I_B$ and $6.5I_B$ respectively.

III. Experimental Results

A test chip prototype of the A, A/AB and AB/AB circuits of Fig. 1b, 1c and 2a respectively was fabricated in 0.5μm CMOS technology (see micrograph in Fig. 3). Resistors R=50kΩ, Rc=330Ω (on chip) and unit transistor sizes were W/L=25/1 and 60/1 for PMOS and NMOS transistors respectively. The circuits were tested with I_B=50μA in voltage follower configuration with V_{out} connected directly on chip to the negative input terminal while V'_{out} was made available off chip as shown in Fig. 1a. A 250kHz, 2Vpp input pulse signal and supply voltages V_{DD}=2.2V, V_{SS}=-2.2V were used. Fig. 4 shows the experimental pulse response of the circuits of Fig. 1a and 1b with C_L=80pF. They have slew rates SR=1V/μs for the conventional circuit Fig. 1a and SR=16V/μS for proposed class A/AB of Fig. 1b. Bandwidth was BW=15MHz. In simulations circuits showed stable behavior down to capacitive loads C_L=10pF, noise was 10nV/√Hz for all circuits. Fig. 5 compares the pulse response of the circuits of Fig. 1a, 1b and 2a with C_L=500pF. In this case slew rates had values SR=10V/μs for the AB/AB op-amp of Fig. 2a, SR=2.5V/μs for the A/AB circuit of Fig. 1b and SR=0.2V/μs for the A/A circuit of Fig. 1a. This corresponds to maximum output currents with values 5mA, 1.1mA and 100μA respectively. These experimental results validate the efficient class AB behavior of the proposed structures.

IV. Conclusion

Two class AB two stage op-amps were introduced. One of them uses LCMFB to implement an output stage with class AB behavior, the second one has in addition to LCMFB a class AB input stage. The A/AB and AB/AB circuits showed large experimental slew rate enhancement factors of 12.5 and 50 respectively. These are achieved with only 25% and 62% additional static power dissipation.

Acknowledgments

Authors would like to acknowledge financial support from the Spanish CICYT under projects TEC2007-67460-C03 and TIC2005-08091-C03-03.

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