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# An Enhanced Fully Differential Recyclic Folded Cascode OTA

Pravanjan Patra, S.Kumaravel
Research scholar, ECE
Tiruchirappalli, INDIA
pravanjanpatra80@gmail.com, kumaravel@nitt.edu

Dr. B.Venkatramani
Professor, ECE
Tiruchirappalli, INDIA
bvenki@nitt.edu

*Abstract* - **In the literature, Recyclic Folded Cascode (RFC) and Improved RFC (IRFC) Operational Transconductance Amplifiers (OTAs) are proposed for enhancing the DC gain and the Unity Gain Bandwidth (UGB) of the Folded Cascode (FC) OTA. In this paper, an enhanced RFC (ERFC) OTA which uses positive feedback at the cascode node is proposed for increasing the DC gain without changing the unity gain bandwidth (UGB). This also has an additional advantage of decreasing the Common–Mode (CM) gain of the OTA. For the purpose of comparison, RFC, IRFC and ERFC OTAs are implemented using UMC90nm technology and studied through simulation. From the simulation, it is found that the DC gain of ERFC OTA is higher by 6dB, 1dB compared to that of RFC and IRFC OTAs respectively. The CM gain of ERFC OTA is lower by 31dB, 34dB compared to that of RFC and IRFC OTAs respectively for the same power and area. The Slew rate of ERFC OTA is higher by a factor of 1.14, 1.08 compared to RFC and IRFC OTAs.**

## I. INTRODUCTION

High performance A/D converters and switched capacitor filters require Operational Transconductance Amplifiers (OTAs) that has both high DC gain and a high unity gain bandwidth (UGB). The advents of deep sub-micron technologies enable increasingly high speed circuits. As the technology scales down, the intrinsic gain $g_m r_o$ of the transistor decreases which makes it difficult to design OTAs with high DC gain. In low voltage CMOS process, Folded Cascode (FC) amplifier is one of the most preferred architectures for both single stage and the multi stage amplifiers (in the first stage) due to its high gain and reasonably large output signal swing. Moreover, the FC with PMOS input pair is preferred over its NMOS counterpart due to its higher non-dominant poles, lower flicker noise, and lower input common mode range [1].

A number of techniques have been proposed in the literature to enhance the gain of the FC OTA. One of these techniques presented in [2], [3] enhances the DC gain by providing an additional current path at the cascode node. This converts the current source into active current mirror which raises the output current to be above its quiescent value during slewing. Another technique proposed in [4], enhances the DC gain and UGB by modifying the bias current sources of the conventional FC. In the conventional FC these current sources don't contribute to DC gain. A recycling technique is proposed to overcome this disadvantage. This OTA is referred to as Recyclic Folded Cascode (RFC).

In [5] further enhancement in the DC gain and UGB of the RFC OTA is obtained using improved Recyclic structure and is termed as IRFC OTA. In this paper, an enhanced RFC (ERFC) OTA is proposed, by adopting the technique proposed in [2] for the FC OTA. The performance of all the three OTAs (RFC, IRFC, and ERFC) are evaluated through simulation and compared.

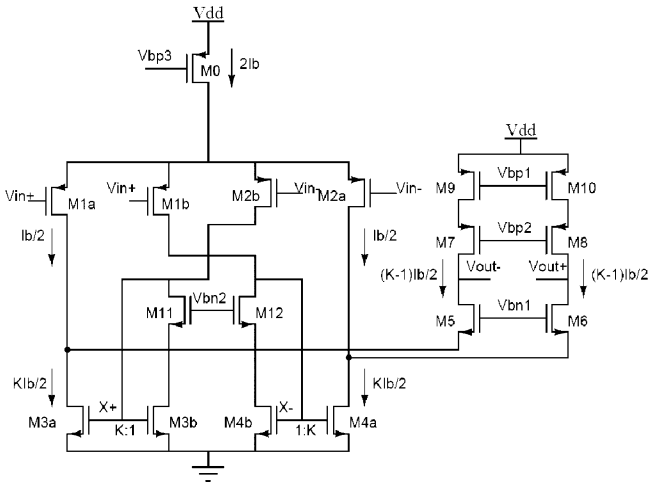


Figure1. Recyclic Folded Cascode OTA

The paper is organized as follows. Section II presents an overview of the conventional RFC OTA. Section III describes about the enhanced RFC OTA proposed in this paper. Section IV and V present the simulation results and the conclusion respectively.

## II. RECYCLIC FOLDED CASCODE OTA

The bias current sources in the conventional FC [1] consume high current, and have large transconductance. However, these current sources don't contribute to the DC gain. In [4], the input transistors of FC are split into two parts (M1a, M1b, M2a, M2b) which conduct fixed and equal currents of $I_b/2$. Next the current source transistor in the FC is replaced by current mirrors M3a:M3b and M4a:M4b at a ratio of K: 1. This architecture is called as the RFC OTA and is shown in Fig.1.

### *A. DC Gain*

The DC gain $A_v$ of the RFC [4] is given by

$$A_v = G_{mRFC} * R_{outRFC} \quad (1)$$

where $G_{mRFC}$ is the transconductance and $R_{outRFC}$ is the output impedance.

The transconductance $G_m$ is given by

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$$G_{mRFC} = I_{out}/V_{i+} \quad (2)$$

where the output current $I_{out}$ is given by

$$I_{out} \approx g_{m1a}V_{i+} + g_{m3a}V_{x+} \quad (3)$$

From Fig.1, it can be seen that transistors M2b and the diode connected transistors M11 and M3b act as a common source amplifier with a voltage gain of approximately -1. Since, the input applied to M2b is in opposite direction, the node $X_+$ (or $X_-$) is in the same phase of $V_{i+}$ (or $V_{i-}$)

where

$$V_{x+} \approx -g_{m2b}R_xV_{i-}$$

and

$$R_x = {}^1/_{g_{m3b}}$$

Hence

$$V_{x+} \approx V_{i+}$$

Substituting $V_{x+}$ in (3)

$$I_{out} = g_{m1a}V_{i+} + g_{m3a}V_{i+} \quad (4)$$

Substituting (4) in (2) gives the small signal transconductance $G_m$.

$$G_{mRFC} = g_{m1a} + g_{m3a} \quad (5)$$

where

$$g_{m3a} \approx K.g_{m1a}$$

The output impedance $R_{out}$ of the RFC OTA is given by

$$R_{outRFC} = g_{m5}r_{05}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09} \quad (6)$$

*B. Frequency Response Analysis:*

From Fig.1, it is observed that there are three poles and one zero. For practical purposes, we need to consider only the poles occurring at the output node and cascode node as the other pole and zero lie far away from origin.

*1.Dominant Pole*: Because of high impedance ($R_{out}$) and large capacitance ($C_{out}$) at the output node, the dominant pole occurs in this node.

The dominant pole frequency $\omega_{p1}$ ($f_{-3db}$) is given by

$$\omega_{p1} = 1/R_{outRFC}C_{out} \quad (7)$$

Where

$$R_{outRFC} \approx g_{m5}r_{o5}(r_{01a}||r_{03a})||g_{m7}r_{07}r_{09}$$

And

$$C_{out} = C_l + C_{DB8} + C_{GD8} + C_{GD6} + C_{DB6}$$

*2. Non-Dominant Pole:* It occurs in the cascode node C at a very high frequency compared to the dominant pole. Since the output capacitance bypasses the effect of output impedance, an equivalent impedance $R_C$ at the cascode node is approximately $1/g_{m5}$. Hence, the non-dominant pole frequency $\omega_{p2}$ is given by

$$\omega_{p2} \approx 1/R_cC_c \quad (8)$$

Where

$$C_C \approx C_{GD3a} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{SB5}$$

The UGB of the OTA is given by

$$UGB = Av * f_{-3db} \quad (9)$$

Using (7) & (8)

$$UGB \approx g_{m1a}(K+1)/C_{out} \quad (10)$$

From (5) & (10), it is observed that the $A_V$ and UGB are enhanced by a factor of 2 (for K = 3 and $g_{m1}$ of FC = $2g_{m1a}$), compared to the FC for the same power and area.

## III. ENHANCED RFC OTA

In Fig.1, the input impedance $Z_C$ at the cascode node C of the RFC OTA is given by (11)

$$Z_c = \frac{1}{g_{m5}}\left(1 + \frac{g_{m7}r_{07}r_{09}}{r_{05}}\right) \cong \frac{g_{m7}r_{07}r_{09}}{g_{m5}r_{05}} \quad (11)$$

In [3], the cascode node of the FC OTA is modified and the current sources are replaced with an active inverting current mirror. The same approach is adopted for the RFC OTA at the cascode node. The modified half circuit of RFC OTA is shown in Fig.2. The active load of the conventional RFC OTA comprising (M7, M9) is modified into an active inverting current mirror comprising (M7, M9, M14, M16, and the inverters). A normal current mirror creates a copy of a current of equal magnitude and in the same direction. The inverting current mirror creates a copy of any incremental currents that is equal in magnitude, but opposite in direction. The inverting incremental currents for M7 and M9 can be obtained from M2a and hence the inverters shown in Fig.2 are not required. Therefore, M12, M14 and M16 are attached to the drain of *M2a.* The fully differential enhanced RFC OTA is shown in Fig.3. The gain from the cascode node to the output node is given by (12). Thus the modified input impedance $Z_C$ at the cascode node is given by (13),

$$\frac{v_{out}}{v_c} \cong (g_{m5} + g_{m12})r_{o5} \quad (12)$$

$$Z_c \cong \frac{g_{m7}r_{07}\,r_{o9}}{2g_{m5}r_{o5}} \quad (13)$$

*A. Description of ERFC*

Next, the operation of the fully differential ERFC is described. Considering a half circuit shown in fig.2 of the differential amplifier, an input voltage of $Vin^+$ is applied to the M1a and $Vin^-$ is applied to the M2b. M2b acts as a

common source amplifier with a diode connected load whose impedance looking into the drain of M2b is given by $1/g_{m3b}$. The voltage at the gate of M3b is now given to M3a which is used for the current mirror action. It copies K times of the current in M3b to M3a. Both the input at the M1a and M3a are in phase. The current produced by M1a and M3a is now given to the cascode node C. At the cascode node, i.e. at the drain of the M1a and M3a, the current sees multiple current paths formed by the cascode transistors M5 and M11. The impedance looking into the source of M5 is of the order of output impedances exhibited by transistor M7 and M9 which is $\approx g_{m7}r_{07}r_{09}$.

The impedance looking into the source of M11 has two diode connected transistors M13 and M15 in series as a load whose impedance is approximately $1/g_{m15}$. Therefore, the path into M11 has significantly lower impedance compared to the other competing paths attached to the cascode node C. Hence, majority of the input current flows into the source of M11 at low frequencies. By the current mirror action of M13, M15, M8 and M10, nearly all the input current is effectively mirrored onto the non-inverting output of the amplifier.

In order to carry out positive current feedback, the current at the non-inverting output is fed directly back to the input section (without inversion). The current at the non-inverting output flows to the other cascode node through transistor M6. The impedance looking into the source of M12 is negligible compared to the impedance as exhibited by other competing current paths at this cascode node Hence, majority of the current flows into the source of M12.

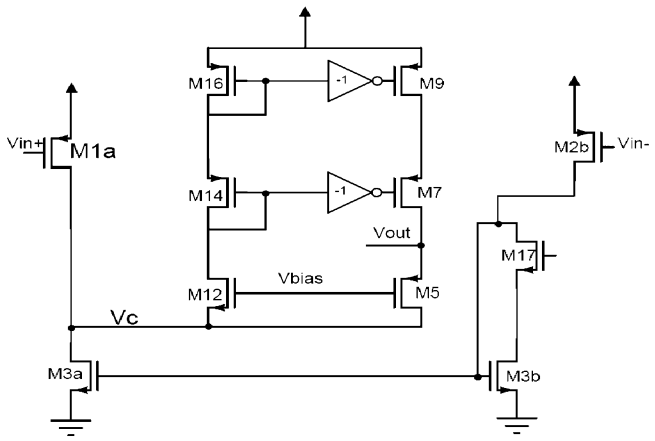


Figure2. Half circuit of ERFC

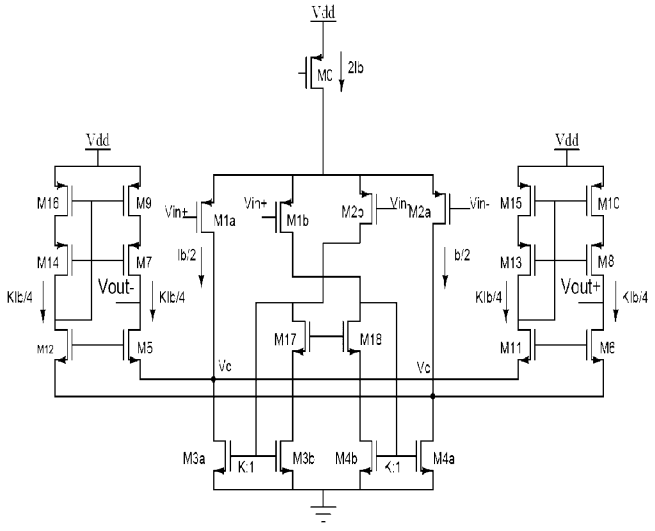


Figure3. Proposed Enhanced RFC OTA

By the current mirror action of M14, M16, M7 and M9, this current is effectively mirrored onto the inverting output. The resulting current at the inverting output flows back into the original cascode node through M5. Similar operation occurs in the other half of the signal at the gate of M2a.Thus the current at the non inverting node is effectively fed back to the starting node. This positive feedback operation gives a higher output resistance (14) and hence a higher gain (15). If $g_{m5}$ and $g_{m11}$ are equal, then the output resistance increases by two times and the gain of the ERFC amplifier is also increased by two times as compared to the RFC.

*B. DC Gain*

$$R_{out} = (1 + {}^{g_{m5}}/_{g_{m11}})R_{outRFC} \tag{14}$$

$$G_m \approx g_{m1a}(1 + k)$$

$$A_0 \approx \quad G_m R_{out} \tag{15}$$

*C. Frequency Response*

The proposed op amp has three poles: the dominant pole at the output node and the non dominant poles at the cascode node (at the drain node of the input transistor (M1, M2) and a pole at current mirror node. Frequency response of the op amp can be analyzed using the differential half-circuit shown in Fig. 3.

*Dominant Pole*: Because of high impedance ($R_{out}$) and large capacitance ($C_{out}$) at the output node, the dominant pole occurs in this node.

The dominant pole frequency $\omega_{p1}$ is given by

$$\omega_{p1} = \frac{1}{R_{out}C_{out}} \tag{16}$$

Where $C_{out}$ denotes the equivalent load capacitance that includes the external capacitance $c_l$, as well as all the parasitic junction capacitances associated with the output node.

$$R_{out} \approx (2g_{m5}r_{05} + 1)(r_{01a} || r_{03a} || \frac{g_{m7}r_{07}r_{09}}{2g_{m5}r_{05}}) \tag{17}$$

and

$$C_{out} \approx C_L + C_{DB8} + C_{GD8} + C_{GD12} + C_{DB12}$$

*Non-Dominant Pole:* The non-dominant pole is determined by the intrinsic capacitances existing at the cascode node C and the effective cascode input impedance $R_C$ at high frequencies. Although the impedance at the cascode node for dc is high, at high frequencies, the drain of M5 is short circuited to ground by $Z_C$. Hence, the impedance at the source of both M5 and M8 is approximately $1/g_{m5}$. Hence, the non-dominant pole $wp_2$ is given by

$$\omega_{p2}=1/R_C.C_C \tag{18}$$

$$R_C = 1/2g_{m5}$$

Where

$$C_C = C_{GD3A} + C_{GS5} + C_{GD1a} + C_{DB3a} + C_{DB1a} + C_{SB5}$$

$C_c$ includes all the intrinsic capacitances at the cascode node.

*4Common Mode Gain*

The difficulties posed by common mode operation of fully differential circuits have been addressed in numerous papers e.g.[6],[7]. In most fully differential amplifiers, the common mode and differential mode signals share the same signal, path resulting in equal and large common mode and differential impedance. The common mode operation of RFC is described next. For common mode input, the signal at the gate of M1a and M3a are out of phase. So as the common mode input decreases the current in M1a increases and the current in M3a also increases because of out of phase. So, if the small signal current coming from the M1a is $\Delta I_d$ then current going through M3a is $K\Delta I_d$ . Hence (K-1)$\Delta I_d$ is now coming from the output node to the cascode node. Hence, the transconductance and output resistance may be shown to be given by (19) and (20).

$$G_m = \frac{I_{out}}{V_{in}} \approx 2g_{m1a}(K-1) \quad (19)$$

$$R_{out} = \left(\frac{g_{m9}r_{09}r_{013}}{2}\right)||g_{m5}r_{05}(r_{01a}||r_{03a}) \quad (20)$$

Hence, the common mode gain is given by (21)

$$A_{cm} = G_m * R_{out} \quad (21)$$

In the half circuit of ERFC OTA shown in Fig.3, the common mode signal sees a lower gain to the source of M5 as the positive feedback loop is not seen by the common mode input. The positive feedback is achieved by the inverting current mirror for differential signals. However in case of common mode signals, the current mirror is non-inverting because instead of using actual inverters, the signal from the other half of the OTA is used, assuming it is inverted. In the common mode circuit, the current in both the halves are identical so that the currents M5 and M11 add up. As a result the common mode output impedance is significantly lower than differential mode output impedance. Hence, the CM gain is reduced by the factor of $g_m r_0$. compared to the conventional RFC. This in turn improves the common mode rejection ratio.

It can be shown that the CM gain $A_{cm}$ is given by

$$A_{cm} = 2g_{m1a}(K-1)\left(\frac{r_{05}}{4}\right) \quad (22)$$

## IV. SIMULATION RESULTS

The ERFC OTA and RFC OTAs, IRFC OTAs reported in the literature [4][5] are simulated using the UMC 90nm CMOS process with a supply voltage of 1.2 volts. The load capacitance $C_L$ for all the OTAs is 5.6pF. For all three OTAs, the parameter K in the bias current source is assumed to be three. The OTAs discussed are implemented and simulated using Cadence SPECTRE Simulator. The area required is the same for all the three OTAs as the transistor widths of M5, M7, and M9 are divided into pairs of M5/M11, M7/M13, M9 and M15. It can be verified from the Table.1 that the size of M5/M7/M9 are 2 times that of the M5/M11/M7/M13/M9/M15. The improvement in common mode rejection ratio can also be analyzed from the Fig.5. Designing a CMFB circuit is difficult for fully differential RFC [4] but that need is eliminated in ERFC. The various parameters of the OTAs such as DC Gain, UGB, Phase Margin CMRR, slew rate, settling time are given in Table.2. The Figure of Merit [FoM] given by (23) is also computed and given in Table.2.

$$Fom = Slewrate * C_l/I_{bias}\left(\left(\frac{V}{us}\right)p_f\right)/mA \quad (23)$$

From Fig.8 and Table.2 the following observations may be made:

- The gain of the ERFC OTA is higher by 6dB, 1dB respectively compared to conventional RFC and IRFC OTAs.
- The CM gain of ERFC OTA is lower by 30dB, 34dB compared to that of RFC and IRFC OTAs respectively. This also implies that the CMRR of ERFC OTA is higher by 49dB compared to that of RFC and IRFC OTAs respectively.
- The Slew rate and Figure of Merit of ERFC OTA are higher by a factor of 1.14 and 1.08 compared to RFC and IRFC OTAs.

## V. CONCLUSION

The fully differential enhanced RFC OTA proposed in this paper and RFC as well as IRFC OTAs reported in the literature have been designed and simulated in UMC 90nm CMOS technology. The increase in the low frequency DC gain is achieved by positive current feedback technique. This in turn results in symmetric slew rate and high common mode rejection ratio. The fully differential Enhanced RFC OTA achieves a higher DC Gain and lower CM gain compared to the other two OTAs. The need for CMFB circuit is also avoided.

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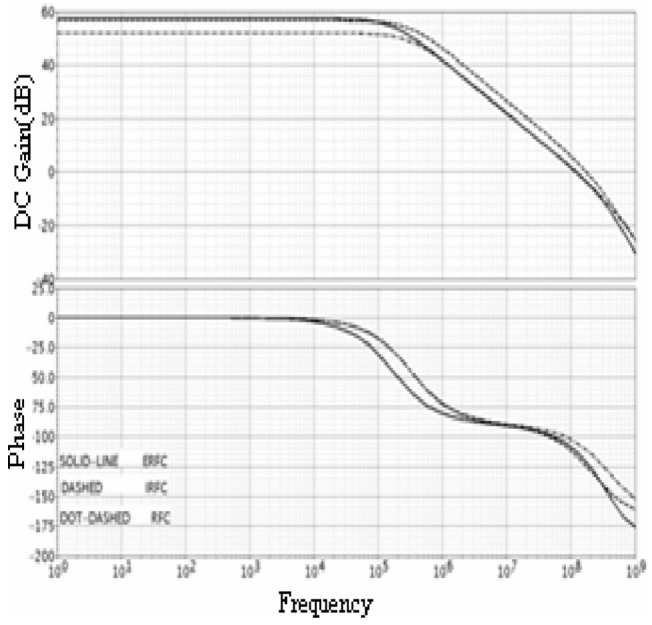


Figure4. Gain and Phase Margin for ERFC and RFC and IRFC

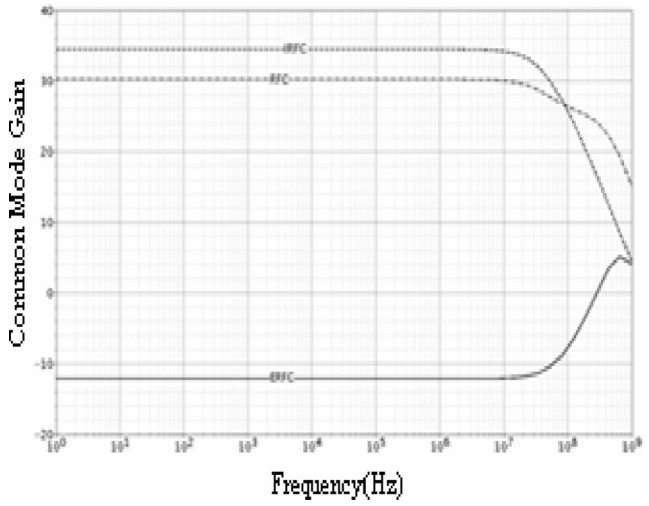


Figure5. Common Mode gain of OTAs

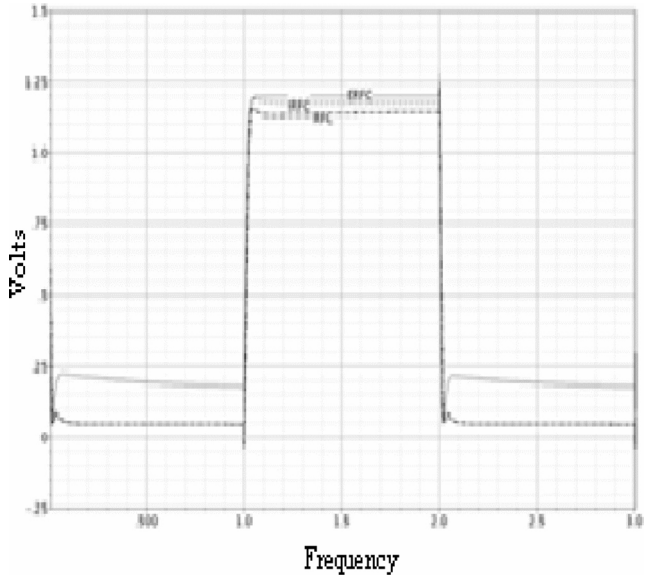


Figure6. Slew rate of RFC, ERFC and IRFC

TABLE1. Device Sizes of ERFC, RFC and IRFC

| DEVICE | ERFC | RFC | IRFC |
|---|---|---|---|
| M0 | 276/0.35 | 276/0.35 | 276/0.35 |
| M1a/M1b/M2a/M2b | 67.636/0.35 | 67.636/0.35 | 67.636/0.35 |
| M3a/M4a | 71/0.5 | 71/0.5 | 71/0.5 |
| M3b/M4b | 24.204/0.5 | 24.204/0.5 | 12.102/0.5 |
| M3c/M4c | - | - | 12.102/0.5 |
| M5 | 10.477/0.18 | 20.954/0.18 | 20.954/0.18 |
| M11 | 10.477/0.18 | - | - |
| M7 | 8.045/0.18 | 16.089/0.18 | 16.089/0.18 |
| M13 | 8.045/0.18 | - | - |
| M9 | 22.0426/0.5 | 44.0853/0.5 | 44.0853/0.5 |
| M15 | 22..0426/0.5 | - | - |
| M11a/M12a | 9.078/0.18 | 9.078/0.18 | 4.539/0.18 |
| M11b/M12b | - | - | 4.539/0.18 |

TABLE2. Device parameters of ERFC, RFC and IRFC

| Parameter | ERFC | RFC | IRFC |
|---|---|---|---|
| Power Consumption | 672uW | 672uW | 672uW |
| DC Gain | 57dB | 51dB | 56dB |
| Load Capacitance | 5.6pf | 5.6pf | 5.6pf |
| Open loop Phase Margin | 68 | 68 | 65 |
| GBW[MHz] | 117 | 117 | 164 |
| Average Slew Rate (V/uS) | 40 | 35 | 37 |
| CMRR(dB) | 70 | 21 | 21 |
| Figure of Merit ((V/us)pF/mA) | 400 | 350 | 370 |