Low-Voltage Super Class AB CMOS OTA Cells With Very High Slew Rate and Power Efficiency

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***Abstract*—A simple technique to achieve low-voltage power-efficient class AB operational transconductance amplifiers (OTAs) is presented. It is based on the combination of class AB differential input stages and local common-mode feedback (LCMFB) which provides additional dynamic current boosting, increased gain-bandwidth product (GBW), and near-optimal current efficiency. LCMFB is applied to various class AB differential input stages, leading to different class AB OTA topologies. Three OTA realizations based on this technique have been fabricated in a 0.5-μm CMOS technology. For an 80-pF load they show enhancement factors of slew rate and GBW of up to 280 and 3.6, respectively, compared to a conventional class A OTA with the same 10-μA quiescent currents and $\pm$1-V supply voltages. In addition, the overhead in terms of common-mode input range, output swing, silicon area, noise, and static power consumption, is minimal.**

***Index Terms*—Adaptive biasing, analog CMOS circuits, class AB amplifiers, low-voltage CMOS circuits, operational transconductance amplifier (OTA).**

I. Introduction

LOW-VOLTAGE operation and optimized power-to-performance ratio are required by modern wireless and portable electronics in order to decrease battery weight and size and to extend battery lifetime. In these and other applications, operational transconductance amplifiers (OTAs) are widely employed as active elements in switched-capacitor filters, data converters, sample and hold circuits, or as buffer amplifiers for driving large capacitive loads [1]. Besides low-voltage and power-efficient operation, these OTAs should have a fast settling response, not limited by slew rate. Conciliating all these requirements is difficult with conventional (class A) OTA topologies, since the bias current limits the maximum output current. Hence, a tradeoff between slew rate and power consumption exists [1]. In order to overcome this issue, adaptive bias circuits are often employed. These circuits provide well-controlled quiescent currents, which can be made very low in order to reduce drastically static power dissipation. However, they automatically boost dynamic currents when a large differential input signal is applied, yielding maximum current levels well above the quiescent currents. Therefore, the amplifier operates in class AB. This current boosting ability is often quantitatively expressed by the current boosting factor (CBF), defined as the ratio of the maximum load current to the differential pair bias current, i.e., $\mathrm{CBF} = I_{\mathrm{out}}^{\mathrm{MAX}}/I_{\mathrm{BIAS}}$.

Several class AB amplifiers have been proposed. Most of them are based on including additional circuitry to increase the tail current when large input signals are applied [2]–[7]. However, the extra circuitry increases both the power consumption and active area of the amplifier, and often adds extra parasitic capacitances to the internal nodes [2]. This degrades small-signal performance, which was already poor due to the low quiescent currents employed. Moreover, positive feedback is frequently employed to achieve boosting of the tail current, by feeding a scaled copy of the input stage differential current back to the tail current. This procedure makes it difficult to enforce unconditionally stable circuits considering variations of process and environmental parameters [3], [6]. Although other topologies are based on negative feedback [7], additional operational amplifiers are required to implement the feedback loops, leading to a complex design. Another shortcoming is that tail current boosting topologies are often not well suited to low-voltage operation, such as earlier approaches based on source-coupled nMOS and pMOS transistors [4] due to the stacking of gate-source voltages. Other topologies suffer from quiescent currents that depend on supply voltage and process parameters [5] leading to unstable performance characteristics.

Another aspect that deserves mention is power efficiency. This involves not only very low static power dissipation, but also high current utilization [7], also named current efficiency (CE) and defined as the ratio of the load current to the supply current, i.e., $\mathrm{CE} = I_{\mathrm{out}}/I_{\mathrm{supply}}$. This parameter is essential for optimum power management. CE is typically below 0.5 for previously reported class AB amplifiers with output current mirror ratio B equal to 1 [7], which means that at least half of the supply current is wasted in internal replicas of the differential pair current. In these approaches, the only way to improve current efficiency is to scale the output currents by increasing B. However, parasitic capacitances at the internal nodes increase for large B, reducing phase margin. Moreover, quiescent currents at the output branches are also scaled by B.

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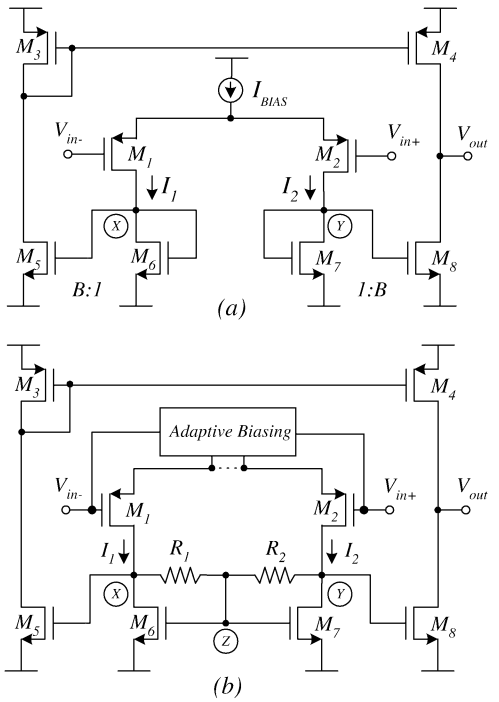

Fig. 1. (a) Class A OTA. (b) Super class AB OTA.

A new class AB design principle is presented here that solves the issues mentioned, and combines excellent performance with simplicity of design and suitability for low-voltage operation. With a few modifications on a conventional OTA, it allows not only to avoid limitation of settling time by slew rate, but also to improve small-signal characteristics like gain-bandwidth product (GBW) and to achieve near-optimal current efficiency without sacrificing static power consumption and with output current mirror ratio B equal to 1. In Section II, the basic principle is presented and its main characteristics are derived. In Section III, different OTA topologies based on this design principle are described. Measurement results for a 0.5-μm CMOS implementation of these OTAs are presented in Section IV, and their performance is compared to that of a conventional OTA. Finally, some concluding remarks are given in Section V.

II. Principle of Operation

Fig. 1(a) shows a conventional OTA. It is assumed that the aspect ratio of transistors M_5 and M_8 is B times that of M_6 and M_7. The well-known expressions for the dc open-loop gain and dominant pole are $A_{\rm OL} = Bg_{m1,2}R_{\rm out}$ and $f_{\rm Pout} = 1/(2\pi R_{\rm out}C_L)$, respectively, where $g_{m1,2}$ is the small-signal transconductance of M_1 and M_2, and $R_{\rm out}$ and C_L are the equivalent resistance and capacitance at the output node. Therefore, the gain-bandwidth product is ${\rm GBW} = Bg_{m1,2}/(2\pi C_L)$. The internal poles at nodes X and Y are $f_{PX} \approx g_{m6}/(2\pi C_X)$ and $f_{PY} \approx g_{m7}/(2\pi C_Y)$, where $C_X \approx C_{\rm GS5} + C_{\rm GS6}$ and $C_Y \approx C_{\rm GS7} + C_{\rm GS8}$ are the parasitic capacitances at nodes X and Y, respectively. Typically the condition $2{\rm GBW} < f_{PX,Y}$ is used in practice to enforce enough phase margin.

The quiescent current flowing through transistors M_1, M_2, M_6, and M_7 is $I_{\rm BIAS}/2$, and $BI_{\rm BIAS}/2$ in M_3, M_4, M_5, and M_8. The maximum current delivered to the load is $BI_{\rm BIAS}$ and the slew rate is therefore ${\rm SR} = BI_{\rm BIAS}/C_L$. Hence, for a given C_L, to avoid limitation of settling time by slew rate B and/or $I_{\rm BIAS}$ should be large. An increase in $I_{\rm BIAS}$ leads to the same increase in static power dissipation. Larger B values not only increase slew rate, but also GBW and current efficiency, which for the conventional OTA of Fig. 1(a) is given by $B/(B+1)$ [7]. These arguments suggest that B should be maximized. Unfortunately, assuming operation in strong inversion of the current mirrors static current consumption is $I^Q = {\rm SR}\cdot C_L\cdot(1+1/B)$, so even for very large B slew rate can only increase proportionally to the static power consumption. This is because quiescent currents experience the same multiplication by B as dynamic currents do. Therefore, it is difficult to achieve high slew rate with low static power consumption using a conventional class A OTA. Moreover, an increase in B leads to larger parasitic capacitances at nodes X and Y, reducing the phase margin.

A typical solution is to replace the constant bias current source $I_{\rm BIAS}$ of Fig. 1(a) by an adaptive bias circuit which provides very small quiescent currents to M_1 and M_2. When such adaptive circuit senses a large differential input signal, it automatically boosts the bias current provided. However, typically in CMOS technologies current boosting is just proportional to the square of the differential input voltage, and current efficiency is still 0.5 in the best case for $B = 1$ [7]. Moreover, small-signal characteristics like GBW are often degraded by the additional circuitry added.

Fig. 1(b) shows the solution that we propose. In addition to the use of an adaptive bias circuit at the input differential pair, the active load of the differential pair is rearranged including local feedback loops via matched resistors R_1 and R_2. The common mode of the drain voltages of M_6 and M_7 is thus fed back to their common gate. This latter technique was formerly coined as local common-mode feedback (LCMFB) [8]–[10], and provides additional current boosting, near-optimal current efficiency, and increased GBW to our class AB amplifiers.

A. Small-Signal Analysis

When an ac small-signal differential voltage v_{id} appears at the input of the OTA in Fig. 1(b), the class AB input stage behaves similar to a conventional class A differential pair, and complementary small-signal currents $i_1 = -i_2 = kg_{m1,2}v_{id}/2$ are generated. Typically k is equal to 1, but in some cases (see Section III-A) it can be 2. Assuming that $R_{1,2} \ll r_{o6,7}$, where $r_{o6,7}$ is the small-signal drain-source resistance of M_6 and M_7, a small-signal current $i_R = i_1 = -i_2$ flows through the resistors, generating complementary ac voltage variations at nodes X and Y given by $v_X = -v_Y = R_{1,2}i_R = R_{1,2}kg_{m1,2}v_{id}/2$. Therefore, $v_Z = 0$ V and node Z becomes an ac virtual ground, thus eliminating the influence of $C_{\rm GS6}$ and $C_{\rm GS7}$ in the capacitances at nodes X and Y. This effect tends to increase the high-frequency poles f_X and f_Y. However, the small-signal resistance of these nodes is also increased by R_1 and R_2, i.e., $R_{X,Y} \approx R_{1,2}\|r_{o6,7}\|r_{o1,2}$. Thus, stability reasons impose an upper limit on the value of $R_{1,2}$. The gain-bandwidth product is

$$ {\rm GBW} = \frac{kg_{m1,2}g_{m5,8}R_{X,Y}}{2\pi C_L} \qquad (1) $$

so an increase of $kg_{m5,8}R_{X,Y}$ is achieved compared to the OTA of Fig. 1(a) with $B = 1$. The phase margin PM as a function of $R_{1,2}$ is given by

$$\begin{aligned}\mathrm{PM} &\approx 90^\circ - \mathrm{arctg}\left(\frac{\mathrm{GBW}}{f_{X,Y}}\right)\\ &\approx 90^\circ - \mathrm{arctg}\Bigg[kg_{m1,2}g_{m5,8}\\ &\qquad\cdot (R_{1,2}\|r_{o6,7}\|r_{o1,2})^2\,\frac{C_{\mathrm{GS5,8}}}{C_L}\Bigg]. \quad (2)\end{aligned}$$

This formula allows estimation of the maximum value for $R_{1,2}$ that can be employed for a given phase margin PM and load capacitance C_L. If $R_{1,2}$ is too large ($\approx r_{o6,7}\|r_{o1,2}$) the OTA of Fig. 1(b) behaves like a two-stage topology and Miller compensation is required. Fortunately, it is not necessary to use large values of $R_{1,2}$ to achieve very high slew rates in our proposed OTAs, as will be illustrated in Section II-B, thus enforcing enough phase margin.

B. Large-Signal Analysis

When no differential input is present in the OTA of Fig. 1(b), currents I_1 and I_2 generated by the input differential pair are identical and equal to the very small quiescent current I_B provided by the adaptive bias circuit, and no current flows through R_1 and R_2. Assuming operation in strong inversion and saturation, voltages at nodes X, Y, and Z are given in this case by

$$V_X = V_Y = V_Z = V_{\mathrm{TH}} + \sqrt{\frac{2I_B}{\beta_{6,7}}} \quad (3)$$

where V_{TH} and $\beta_{6,7} = \mu_n C_{\mathrm{ox}}(W/L)_{M6,7}$ are the threshold voltage and transconductance factor, respectively, of transistors M_6 and M_7. However, upon application of a differential input signal $V_{id} = V_{i+} - V_{i-}$, a differential current $I_d = I_1 - I_2$ is created, which neglecting channel-length modulation in M_6 and M_7 leads to a current in the resistors $I_R = I_d/2 = (I_1 - I_2)/2$. Current through M_6 and M_7 will be the common-mode current $I_{\mathrm{cm}} = (I_1 + I_2)/2$. Therefore, nodal voltages will be

$$\begin{aligned}V_Z &= V_{\mathrm{TH}} + \sqrt{\frac{2I_{\mathrm{cm}}}{\beta_{6,7}}}\\ V_X &= V_Z + \frac{R_1 I_d}{2}\\ V_Y &= V_Z - \frac{R_2 I_d}{2}. \quad (4)\end{aligned}$$

Hence, a large positive voltage swing takes place at node X for $V_{id} > 0$ V. Assuming operation in strong inversion and saturation for M_5, it leads to a current in M_5

$$I_5 = \frac{\beta_5}{2}\left(V_Z + \frac{R_1 I_d}{2} - V_{\mathrm{TH}}\right)^2 = \frac{\beta_5}{2}\left(\sqrt{\frac{2I_{\mathrm{cm}}}{\beta_{6,7}}} + \frac{R_1 I_d}{2}\right)^2 \quad (5)$$

whereas the large negative swing at node Y strongly decreases current through transistor M_8 below quiescent current I_B. Thus, the output current is $I_{\mathrm{out}} = I_5 - I_8 \approx I_5$. In a similar manner, for $V_{id} < 0$ V $I_d = I_1 - I_2$ is negative, and the large positive swing at node Y yields a large current in M_8, given by

$$I_8 = \frac{\beta_8}{2}\left(V_Z - \frac{R_2 I_d}{2} - V_{\mathrm{TH}}\right)^2 = \frac{\beta_8}{2}\left(\sqrt{\frac{2I_{\mathrm{cm}}}{\beta_{6,7}}} - \frac{R_2 I_d}{2}\right)^2 \quad (6)$$

whereas current in M_5 is lower than I_B and negligible. In this case $I_{\mathrm{out}} = I_5 - I_8 \approx -I_8$. Thus, a general expression for the output current when $V_{id} \neq 0$ V is

$$\begin{aligned}I_{\mathrm{out}} = I_5 - I_8 &\approx \pm\frac{\beta_{5,8}}{2}\left(V_Z + \frac{R_{1,2}\,|I_d|}{2} - V_{\mathrm{TH}}\right)^2\\ &\approx \pm\,\frac{\beta_{5,8}}{2}\left(\sqrt{\frac{2I_{\mathrm{cm}}}{\beta_{6,7}}} + \frac{R_{1,2}\,|I_d|}{2}\right)^2 \quad (7)\end{aligned}$$

where $I_{\mathrm{out}} > 0$ when $V_{id} > 0$ and $I_{\mathrm{out}} < 0$ when $V_{id} < 0$.

Current efficiency is approximately given by $|I_{\mathrm{out}}|/(|I_{\mathrm{out}}| + 2I_{\mathrm{cm}}) = 1/(1 + 2I_{\mathrm{cm}}/|I_{\mathrm{out}}|)$, where I_{out} is given by (7). Since under dynamic conditions $|I_{\mathrm{out}}| \gg I_{\mathrm{cm}}$, current efficiency approaches the ideal value of 1, whereas in the conventional OTA of Fig. 1(a) and in previous class AB OTAs with $B = 1$ it is 0.5 or less [7]. This is because using LCMFB the large dynamic currents are generated directly in the output branches, without internal replication.

A drawback of LCMFB is that independence of current multiplication with absolute process variations, typical of current mirrors, is lost as the expressions above reflect. This is not critical since the exact maximum output current obtained is not very important provided it is high enough to achieve a given settling time. However, process tolerances must be considered at the design stage in order to reach specifications within reasonable safety margins.

LCMFB has been employed in the past combined with conventional class A differential pairs to achieve class AB amplifiers [8]. In this case the maximum differential current I_d of the input pair is twice the quiescent current, i.e., $I_d^{\mathrm{MAX}} = 2I_B = I_{\mathrm{BIAS}}$ where the tail current I_{BIAS} is chosen very small to achieve low static power dissipation. From (7), this implies that large feedback resistors $R_{1,2}$ should be utilized to achieve enough current boosting, which is incompatible with large phase margin. Thus limited current boosting is provided as low enough values for $R_{1,2}$ must be chosen to enforce stability. This limitation explains why the reported slew rate increase factor in [8] versus the conventional OTA is just 3. Potentials of the LCMFB technique for design of class AB amplifiers can only be fully exploited using a class AB differential input stage, as we propose here and show in Fig. 1(b). In this case, current boosting at the input stage may lead to a differential current I_d in (7) much larger than the quiescent current I_B, and therefore a very large current boosting can be achieved in the output current for low values of $R_{1,2}$, simultaneously preserving phase margin and static power dissipation. Dynamic current boosting takes place not only in the differential pair, but also in its active load due to the LCMFB technique. For typical class AB CMOS input stages, the differential current I_d generated is proportional to V_{id}^2 and so is the output current [4], [7]. From (7), including LCMFB the output current will be proportional to I_d^2 and therefore to V_{id}^4, clearly outperforming previously reported CMOS

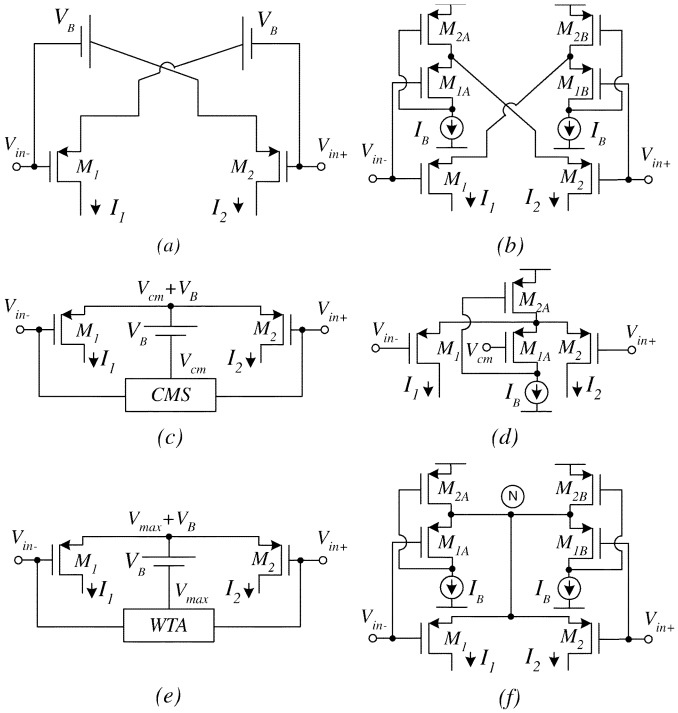

Fig. 2. Adaptive biasing topologies. Using two level shifters: (a) diagram; (b) circuit. Using CMS: (c) diagram; (d) circuit. Using WTA: (e) diagram; (f) circuit.

class AB OTA topologies. Hence, the resulting circuits can be coined as "super" class AB OTAs [10].

III. Super Class AB OTAS

Different super class AB OTA topologies can be obtained using different adaptive biasing techniques for the input differential pair in the general diagram of Fig. 1(b). Fig. 2 shows three alternatives to implement these input stages, suited to low-voltage operation. The resulting OTAs are shown in Fig. 3.

A. Super Class AB OTA With Cross-Coupled Floating Batteries

The scheme of Fig. 2(a) [10], [11] consists of two matched transistors M_1 and M_2 cross-coupled by two dc level shifters. Under quiescent conditions $V_{\rm SG1}^Q = V_{\rm SG2}^Q = V_B$, so transistors M_1 and M_2 carry equal quiescent currents controlled by V_B. If V_B is slightly larger than $|V_{\rm TH}|$, very low standby currents can be achieved. However, for instance when $V_{\rm in+}$ decreases voltage at the source of M_1 decreases by the same amount whereas the source voltage of M_2 stays constant. Therefore, current through M_2 increases whereas current through M_1 decreases. The maximum value of these currents can be much larger than the quiescent current. Very low output impedance dc level shifters are required in order to drive the low-impedance source terminals of transistors M_1 and M_2. The dc level shifters must also be able to source large currents when the circuit is charging or discharging a large load capacitance. Moreover, they should be simple due to noise, speed, and supply restrictions. A very good choice is shown in Fig. 2(b) [10], [11]. Each level shifter is built using two transistors (M_{1A}, M_{2A} and M_{1B}, M_{2B}) and a current source I_B. We name these level shifters Flipped Voltage Followers (FVFs) [12]. They have a very low output resistance (typically in the range 20–100 Ω), and fulfill the aforementioned requirements. Quiescent current in M_1 and M_2 is the well-controlled bias current I_B of the FVFs assuming that transistors M_1, M_2, M_{1A} and M_{1B} are matched. In this case, for large V_{id} currents I_1 and I_2 are

$$I_1 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} + V_{id}\right)^2 \quad I_2 < I_B \quad V_{id} > 0$$
$$I_2 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} - V_{id}\right)^2 \quad I_1 < I_B \quad V_{id} < 0. \quad (8)$$

Although $I_d = I_1 - I_2 \approx \sqrt{8\beta_{1,2}I_B}V_{id}$ when both M_1 and M_2 operate in strong inversion and saturation (i.e., for low $|V_{id}|$ values), due to the small value of $V_B - |V_{\rm TH}| = (2I_B/\beta_{1,2})^{1/2}$ chosen the input transistor with the lowest $V_{\rm SG}$ is soon driven out of strong inversion for not very large V_{id}, and dependence of I_d on V_{id} becomes quadratic. In this case the differential current $I_d = I_1 - I_2$ and common-mode current $I_{\rm cm} = (I_1 + I_2)/2$ are $I_d \approx I_1$ and $I_{\rm cm} \approx I_1/2$ for large positive V_{id} whereas $I_d \approx -I_2$ and $I_{\rm cm} \approx I_2/2$ for large negative V_{id}. From (8), currents I_1 and I_2 are not bounded by I_B, showing the class AB operation of the circuit. The common-mode output current $I_{\rm cm}$ is signal-dependent, another characteristic of class AB topologies.

The ac small-signal differential current of the input stage is

$$i_d = i_1 - i_2 \approx \left(1 + \frac{g_{m2A,B}r_{o1A,B} - 1}{g_{m2A,B}r_{o1A,B} + 1}\right) g_{m1}v_{id} \approx 2g_{m1}v_{id}. \quad (9)$$

Since the ac input signal is applied to both the gate and the source terminals of M_1 and M_2, the transconductance of this input stage is twice that of a conventional differential pair.

Fig. 3(a) shows the super class AB OTA obtained using the adaptive bias circuit of Fig. 2(b) in the scheme of Fig. 1(b). For large and positive V_{id}, from (8) $I_d \approx I_1 \approx (\beta_{1,2}/2)V_{id}^2$ and $I_{\rm cm} \approx I_1/2$. For large negative V_{id}, $I_d \approx -I_2 \approx -(\beta_{1,2}/2)V_{id}^2$, and $I_{\rm cm} \approx I_2/2$. Using (7), the output current in Fig. 3(a) is given by

$$I_{\rm out} \approx \pm\frac{\beta_{5,8}}{2}\left(\sqrt{\frac{\beta_{1,2}}{2\beta_{6,7}}}\,|V_{id}| + \frac{R_{1,2}\beta_{1,2}}{4}V_{id}^2\right)^2 \quad (10)$$

where the sign of $I_{\rm out}$ corresponds to the polarity of V_{id}. It is clear that for a large V_{id} the output current increases with V_{id}^4, enhancing quadratically the current boosting provided by the class AB input stage. The GBW of the OTA is given by (1) with $k = 2$. An increase factor $2g_{m5,8}R_{X,Y}$ appears in the dc gain compared to the conventional OTA of Fig. 1(a), which translates to the same increase in GBW. The factor $g_{m5,8}R_{X,Y}$ is due to the LCMFB technique, and the additional factor 2 is due to the doubled transconductance of the input stage.

The minimum supply voltage of the circuit is $|V_{\rm TH}| + 3|V_{\rm DS,sat}|$ where $|V_{\rm DS,sat}|$ is the minimum $|V_{\rm DS}|$ for operation in saturation. For $|V_{\rm TH}| = 0.7$ V and $|V_{\rm DS,sat}| = 0.2$ V it yields 1.3 V. The common-mode input voltage is similar to that of the conventional class A OTA of Fig. 1(a). Therefore the circuit is suitable for low-voltage operation. Other approaches based on

source-coupled nMOS and pMOS transistors [4] require a minimum supply voltage of $2|V_{\rm TH}| + 3|V_{\rm DS,sat}|$. Note, however, that the FVF cell is suited to low supply voltages only, as the drain voltage of $M_{1A,B}$ is $V_{\rm DD} - V_{\rm SG2A,B}$, which can make $M_{1A,B}$ enter triode region if $V_{\rm DD}$ is large enough. For high supply voltages, a source follower can be included in the FVF loop acting as a dc level shifter to solve this issue [12].

Transistors M_{2A} and M_{2B} in the FVF cells provide shunt feedback, and the FVF cell forms a two-pole negative feedback loop. Stability of the FVF cell can be readily enforced by proper sizing of transistors to ensure the condition $g_{m1A,B}/(4g_{m2A,B}) > C_{p1}/C_{p2}$, where C_{p1} and C_{p2} are the parasitic capacitances at the source and drain, respectively, of $M_{1A,B}$. FVF load capacitance is included in C_{p1}. For large FVF capacitive loads the inclusion of a grounded compensation capacitor at the drains of M_{1A} and M_{1B} could be necessary to increase C_{p2}.

B. Super Class AB OTA With Pseudodifferential Pair

An alternative class AB input stage is shown in Fig. 2(c)[13], [14]. Voltage at the common-source node of the input differential pair is set to the input common-mode voltage ($V_{\rm cm}$) shifted by V_B. Under quiescent conditions, $V^Q_{\rm SG1} = V^Q_{\rm SG2} = V_B$ and voltage V_B controls the quiescent currents like in Fig. 2(a). When a differential input is applied, an unbalance in the drain current is produced that is not limited by the quiescent current. A very efficient implementation of the dc level shifter is again the FVF, and the resulting circuit is shown in Fig. 2(d). In this case $V_B = V_{\rm SG,1A}$ and the FVF bias current I_B is the quiescent current of the input differential pair, assuming matched transistors M_1, M_2, and M_{1A}. Currents I_1 and I_2 are given by

$$I_1 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} + \frac{V_{id}}{2}\right)^2 \quad I_2 < I_B \quad V_{id} > 0$$
$$I_2 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} - \frac{V_{id}}{2}\right)^2 \quad I_1 < I_B \quad V_{id} < 0. \quad (11)$$

As in Fig. 2(b), output currents increase quadratically with V_{id} and are not limited by I_B. A circuit, labeled CMS in Fig. 2(c), is required to sense the common-mode input voltage $V_{\rm cm}$ and to apply it to the gate of transistor M_{1A}, in order to make quiescent currents independent of the input common-mode voltage, and thus to obtain a high common-mode rejection ratio (CMRR).

Fig. 3(c) and (d) shows two implementations of Fig. 1(b) using the circuit of Fig. 2(d) with different common-mode sensing techniques. In both cases the common-mode voltage $V_{\rm cm}$ is sensed by applying the input voltage to a resistive divider through two FVF buffers, thus exploiting the benefits already mentioned of the FVF cell. Voltage at node A is $V_{\rm cm} + V_{\rm SG9,11}$. In Fig. 3(c), a down-shifting $-V_{\rm SG15} = -V_{\rm SG9,11}$ is applied to obtain $V_{\rm cm}$ at the gate of M_{1A}. Noting that M_{15} and M_{1A} lead to complementary dc level shifts, an alternative approach is shown in Fig. 3(d) where these transistors are removed, and a simple buffer is employed. The amplifier used in Fig. 3(d) is a simple nMOS differential pair with active load. An alternative and very compact approach not discussed here for sensing of input common-mode level is based on the use of floating-gate transistors [15].

Both in Fig. 3(c) and (d), differential and common-mode currents flowing out of the input pair are $I_d \approx I_1 \approx (\beta_{1,2}/8)V_{id}^2$ and $I_{\rm cm} \approx I_1/2$ for large positive V_{id}, and $I_d \approx -I_2 \approx -(\beta_{1,2}/8)V_{id}^2$ and $I_{\rm cm} \approx I_2/2$ for large negative V_{id}. Therefore, using (11) and (7) the output current is

$$I_{\rm out} \approx \pm\frac{\beta_{5,8}}{2}\left(\sqrt{\frac{\beta_{1,2}}{2\beta_{6,7}}}\frac{|V_{id}|}{2} + \frac{R_{1,2}\beta_{1,2}}{16}V_{id}^2\right)^2 \quad (12)$$

where the sign of $I_{\rm out}$ corresponds to the polarity of V_{id}. Like for the OTA of Fig. 3(a), the output current increases with V_{id}^4, enhancing quadratically the current boosting provided by the class AB input stage. However, comparing (12) and (10) a lower current boosting is predicted for the topologies of Fig. 3(c) and (d) compared to Fig. 3(a) for identical transistor dimensions and quiescent currents, due to the factor 2 that divides V_{id} in (11). The small-signal transconductance of the input stage is also half that of Fig. 3(a), i.e., like the conventional class A OTA, since the ac input signal is only applied to the gate of the input transistors and their source is an ac virtual ground. Thus for fully differential inputs the ac small-signal v_{gs} of the input transistors is half the differential ac input swing. Therefore, the GBW of the OTA is given by (1) with $k = 1$. Only the increase factor $g_{m5,8}R_{X,Y}$ in the dc gain due to the use of LCMFB appears compared to the conventional OTA of Fig. 1(a), which translates to the same increase in GBW. Supply voltage requirements and common-mode input range are the same as for Fig. 3(a), allowing low-voltage operation.

C. Super Class AB OTA With WTA Input Stage

Fig. 2(e) shows a modification proposed here of the idea in Fig. 2(c), where a Winner-Take-All (WTA) circuit replaces the common-mode sensing circuit. The output of the WTA circuit is the maximum (the "winner") of the input voltages. Therefore, voltage at the common-source node of the differential pair is the maximum input voltage $V_{\rm max}$ shifted by the constant voltage V_B. Under quiescent conditions, input voltages are equal, and their maximum value corresponds to the common-mode input voltage. Thus $V^Q_{\rm SG1} = V^Q_{\rm SG2} = V_B$, and quiescent currents are well controlled and determined by V_B like in the circuits of Fig. 2(a) and (c). The difference arises under dynamic conditions. If for instance the input voltage $V_{\rm in+}$ decreases so that it is lower that $V_{\rm in-}$, the common-source node tracks the maximum input voltage, i.e., $V_{\rm in-}$, and not the common-mode voltage of the inputs. Therefore, the resulting $V_{\rm SG2}$ is larger than that obtained for the same input in Fig. 2(c), and a larger dynamic current boosting is achieved. A related strategy which uses a Minimum circuit was reported in [7]. However, two additional amplifiers in negative feedback configuration are required, complicating the design. Here only four transistors are utilized to achieve the Maximum operator.

Fig. 2(f) shows a very efficient implementation of the WTA circuit. The basic cell employed is once more a FVF cell thus benefiting from its large sourcing capability, low output impedance and low-voltage operation. It will be assumed that transistors M_1, M_2, M_{1A} and M_{1B} are matched. In this case,

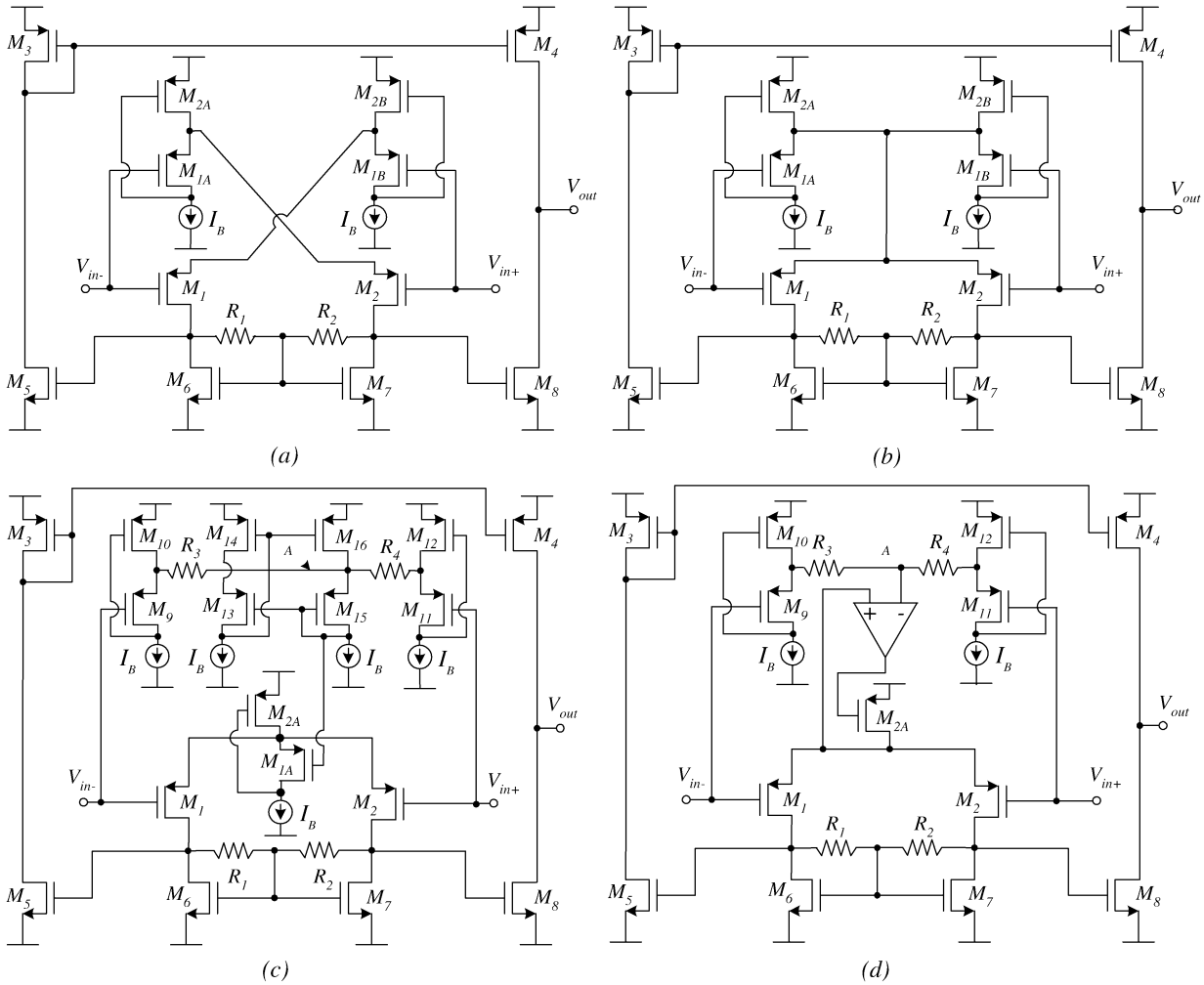

Fig. 3. Super class AB OTAs. (a) Based on Fig. 2(b). (b) Based on Fig. 2(f). (c), (d) Based on Fig. 2(d).

under quiescent conditions $V_{\text{in}+} = V_{\text{in}-} = V_{\text{cm}}$, and voltage at node N is $V_N = V_{\text{cm}} + V_B = V_{\text{cm}} + V_{\text{SG},1A-B}$, yielding again a quiescent current I_B. If for instance $V_{\text{in}-}$ decreases, $V_{\text{SG},1A}$ increases so the drain voltage of M_{1A} increases, driving M_{1A} into triode region. In this situation voltage at node N is set by $V_{\text{in}+}$, the dimensions of M_{1B}, and current I_B, i.e., $V_N = V_{\text{in}+} + V_{\text{SG},1B}$. Accordingly, when $V_{\text{in}+}$ decreases below $V_{\text{in}-}$, M_{1B} enters triode region and $V_N = V_{\text{in}-} + V_{\text{SG},1A}$.

Hence, for $V_{id} > 0$ V, $V_{\text{in}+} > V_{\text{in}-}$, $V_N = V_{\text{in}+} + V_{\text{SG},1B}$ and currents I_1 and I_2 are

$$I_1 = \frac{\beta_{1,2}}{2}\left(-V_{\text{in}-} + V_N - |V_{\text{TH}}|\right)^2 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} + V_{id}\right)^2 \quad I_2 = I_B. \tag{13a}$$

In a similar way, when $V_{id} < 0$ V, $V_{\text{in}+} < V_{\text{in}-}$, $V_N = V_{\text{in}-} + V_{\text{SG},1A}$, and currents I_1 and I_2 are

$$I_2 = \frac{\beta_{1,2}}{2}\left(-V_{\text{in}+} + V_N - |V_{\text{TH}}|\right)^2 = \frac{\beta_{1,2}}{2}\left(\sqrt{\frac{2I_B}{\beta_{1,2}}} - V_{id}\right)^2 \quad I_1 = I_B. \tag{13b}$$

Therefore, the same maximum currents as in (8) are generated. Again I_1 and I_2 may be significantly larger than I_B.

The ac small-signal differential current of the input stage is $i_d = i_1 - i_2 = g_{m1,2}v_{id}$, like for the OTAs of Figs. 1(a) and 3(c) and (d). This is because, although under large-signal conditions the largest V_{SG} of the input transistors is $|V_{id}| + V_{\text{SG},1A}$ due the WTA circuit, for a fully balanced ac small-signal input the node N is an ac virtual ground and $v_{gs1,2} = \pm v_{id}/2$.

Fig. 3(b) shows the super class AB OTAs obtained employing the adaptive bias circuit of Fig. 2(f) in the scheme of Fig. 1(b). The maximum output current is the same as for the OTA of Fig. 3(a), given by (10). Since $i_d = g_{m1,2}v_{id}$, the predicted dc gain is like for the OTAs of Section III-B, and also GBW is given by (1) with $k = 1$. The requirements in terms of supply voltage and the input common-mode range are identical than for the OTA of Fig. 3(a) and the conventional class A OTA of Fig. 1(a).

D. Comparison of the Super Class AB OTAS

The differences among the OTAs of Fig. 3 are due to the different class AB input stages employed. All the OTAs achieve a current boosting proportional to V_{id}^4, clearly outperforming previous approaches. However, the topologies of Fig. 3(a) and (b) achieve the maximum output current for a certain V_{id}, given by (10) and identical in both cases. The OTAs of Fig. 3(c) and (d) yield a lower output current for the same V_{id}, as can be de-

duced from (12). This difference is due to the fact that under dynamic conditions signal is injected both at the gate and the source terminals of the input transistor that generates the maximum current in the circuits of Fig. 2(b) and (f), but in Fig. 2(d) the source terminal is a signal ground in such transistor. For instance, for a large positive V_{id}, the $V_{\rm SG}$ of M_1 in Fig. 2(b) and (f) is $V_{id}+V_{{\rm SG},1B}$, but only $V_{id}/2+V_{{\rm SG},1A}$ in Fig. 2(d). Another disadvantage of the OTAs of Fig. 3(c) and (d) is the need for a common-mode sensing circuit.

Finally, although both OTAs in Fig. 3(a) and (b) achieve the same maximum current, an advantage of the circuit of Fig. 3(b) is that the lowest current in the differential pair is never less than I_B, as reflected in (13a) and (13b), and none of the input transistors is in cutoff. The reason is that for instance, for a large positive V_{id}, in Fig. 2(f) $V_N = V_{\rm in+}+V_{{\rm SG},1B}$ and the $V_{\rm SG}$ of M_2 is constant and equal to $V_{{\rm SG},1B}$. However for the same V_{id} in Fig. 2(b), the $V_{\rm SG}$ of M_2 is $V_{\rm in-}+V_{{\rm SG},1A}-V_{\rm in+}=V_{{\rm SG},1A}-V_{id}$, and soon it makes M_2 enter cutoff.

E. Operation in Weak and Moderate Inversion

The analysis carried out to achieve simple expressions for the maximum output current in the OTAs of Fig. 3 has been based on the assumption that transistors operate in strong inversion and saturation. However, the OTAs proposed can also operate in weak and moderate inversion regions. If a small enough I_B is chosen to operate the transistors of the OTAs of Fig. 3 in weak inversion and saturation under quiescent conditions, upon application of a small differential input voltage V_{id} currents I_1 and I_2 in the input pair become

$$\begin{aligned}
&I_1 = I_B e^{(V_{id}/nU_T)} \quad I_2 = I_B e^{-(V_{id}/nU_T)} \quad \text{Fig. 3(a)}\\
&I_1 = I_B e^{(V_{id}/2nU_T)} \quad I_2 = I_B e^{-(V_{id}/2nU_T)} \quad \text{Fig. 3(c),(d)}\\
&I_1 = \max\left(I_B e^{(V_{id}/nU_T)}, I_B\right)\\
&I_2 = \max\left(I_B e^{-(V_{id}/nU_T)}, I_B\right) \quad \text{Fig. 3(b)} \qquad (14)
\end{aligned}$$

where n is the subthreshold slope and $U_T = kT/q$ is the thermal voltage. Therefore an exponential current boosting is achieved at the input pair as opposed to the quadratic boosting obtained in strong inversion, although it is again lower in Fig. 3(c) and (d). When V_{id} reaches a large enough value the input pair transistor with largest current will enter strong inversion and the quadratic boosting in the input stage appears. During such transition this transistor operates in moderate inversion and the situation is intermediate. The additional current boosting due to LCMFB is quadratic in any case for practical purposes, since the gate voltage of the transistor with the largest current (M_5 or M_8) increases exponentially with $|V_{id}|$ when the input pair operates in weak inversion, and makes such transistor enter strong inversion even for very small values of $|V_{id}|$. In fact, even if the circuits are designed to operate in weak or moderate inversion under quiescent conditions to save static power, the dynamic behavior for large transient signals is similar to that observed with circuits designed for quiescent operation in strong inversion. This is due to the large dynamic currents present in both cases.

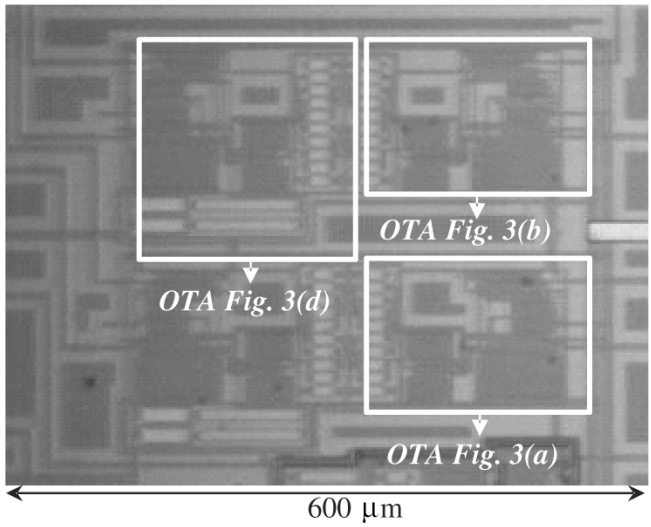

Fig. 4. Test chip microphotograph.

IV. Measurement Results

A test chip prototype containing the OTAs of Fig. 3(a), (b), and (d) was fabricated in an AMI 0.5-μm CMOS n-well process, with nominal nMOS and pMOS threshold voltages of about 0.67 V and -0.96 V, respectively. The aspect ratios (in μm) of transistors M_1, M_2, M_{1A}, M_{1B}, M_9, and M_{11} were 50/1, and those of transistors M_3, M_4, M_{2A}, M_{2B} were 240/1. Transistors M_5–M_8 were 120/1, and M_{10}, M_{12} were 24/1. Resistors had values of 10 kΩ, and were implemented using interdigitized polysilicon strips. However, linearity is not critical for the resistors. They can be implemented by MOS transistors in triode region, saving active area and with the additional advantage that the resistance value can be readily programmed using a bias voltage [8]. This way, the resistance value can be adjusted to compensate for process variations and to achieve a certain phase margin for a given C_L, as (2) reflects. Supply voltages were ± 1 V, and bias current I_B was set to 10 μA. Fig. 4 shows a microphotograph of the chip, where the location and relative area of the three OTAs can be observed.

Fig. 5 shows the measured dc output transconductance characteristics (short circuit output current versus differential input voltage) of the three OTAs, and that of a conventional class A OTA, fabricated in the same prototype for comparison. Supply voltages and quiescent currents were the same for the conventional OTA. Note that only the conventional OTA has a maximum current limited by the quiescent current, showing the class AB operation of the proposed OTAs. The measured output currents are in agreement with expressions (10) and (12). The maximum current boosting factor is achieved by the OTAs of Fig. 3(a) and (b), as predicted in Section III. In Fig. 6, the measured dc output current of the OTA of Fig. 3(b) is compared with an ideal quadratic current boosting, for negative differential input voltages. Note that the current boosting obtained is larger than this quadratic function, in agreement with (10). This additional current boosting is due to the LCMFB technique employed. In the same figure the measured supply currents are shown. Note that most of the supply current is delivered to the load of the OTA, so current efficiency is nearly

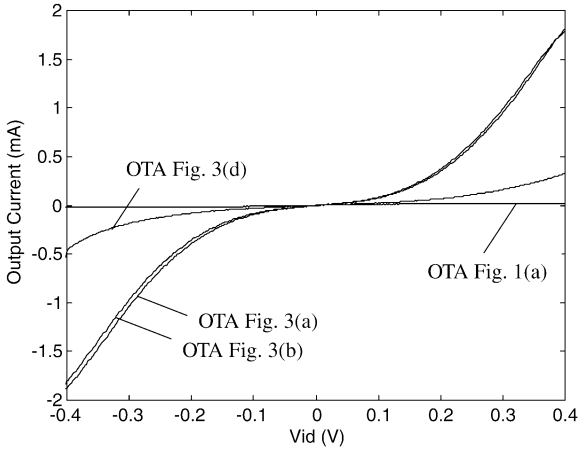

Fig. 5. Measured dc output characteristics of the OTAs.

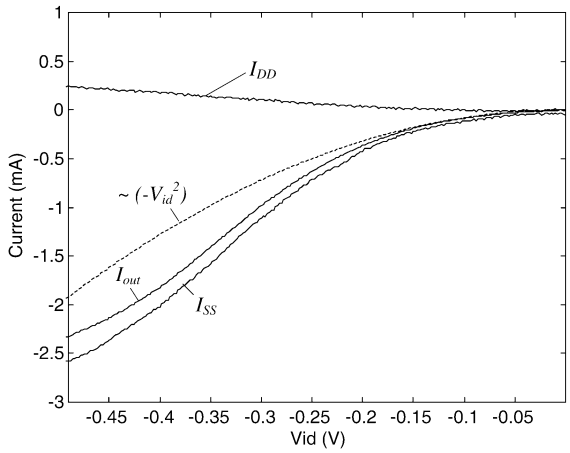

Fig. 6. Measured load and supply currents for a negative dc input swing.

optimal as predicted in Section III. Similar results are obtained for the other Super Class AB OTAs.

The transient response of the OTAs was measured connecting them in unity-gain configuration, and using a 1-MHz square wave at the input. The output terminal was connected directly to a bonding pad and no external buffer was employed, so the load capacitance corresponds to the pad, breadboard, and test probe capacitance. It is of approximately 80 pF. Fig. 7 shows in solid line the output of the proposed OTAs and the output of the conventional class A OTA. The input is the dotted waveform, almost undistinguishable from the output of the proposed OTAs. Supply voltage, load, and quiescent currents were identical for all the OTAs. Table I shows the main measured parameters of the OTAs. Note the increase in slew rate obtained using the super class AB OTAs, of more than two orders of magnitude, and the increase in GBW. In agreement with the comparison of Section III-D, measurements show a similar slew rate for the OTAs of Fig. 3(a) and (b), more than 200 times that of the class A OTA for the same load and quiescent current, and larger than that of the OTA of Fig. 3(d). The LCMFB also leads to an increase of about 7 dB in dc gain for the super class AB OTAs, as predicted in Section II-A, which is also responsible for the higher GBW. Moreover, as expected from Section III-A, an additional increase of about 6 dB in the OTA of Fig. 3(a) takes

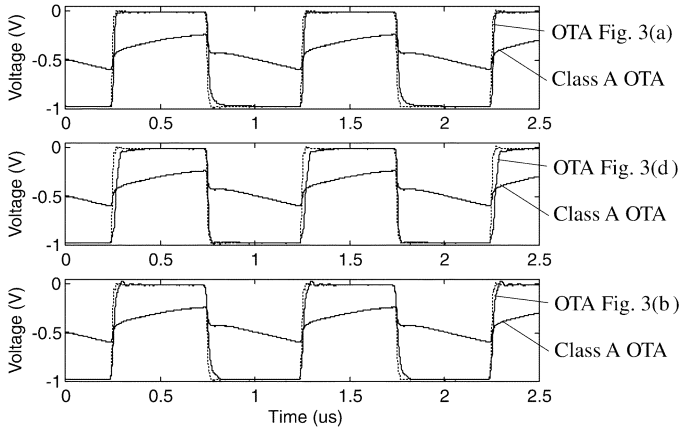

Fig. 7. Transient response of the OTAs of Fig. 3(a) (upper graph), Fig. 3(d) (middle graph), and Fig. 3(b) (lower graph).

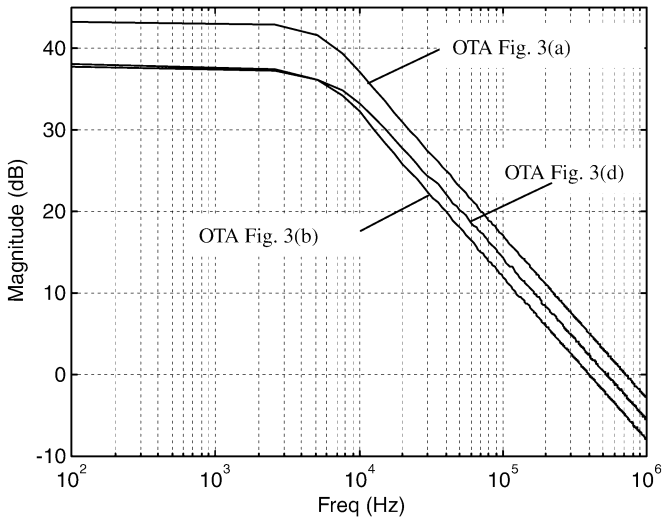

Fig. 8. Measured open-loop frequency response of the OTAs.

place, also producing an additional increase in GBW, compared with the OTAs of Fig. 3(b) and (d).

Fig. 8 shows the measured open-loop frequency response of the OTAs. The dc gain is around 40 dB. It can be readily extended to about 80 dB by using a cascode output stage, at the expense of a reduced output range. The phase margin is around 90° in all cases for this load capacitance. The small-signal characteristics of the proposed OTAs are not only maintained compared to the conventional OTA, but even improved in some parameters like dc gain and GBW. Therefore, the proposed technique improves both small-signal and large-signal characteristics, in agreement with the theoretical results of Section II. This is in contrast with other class AB amplifier topologies, which improve large-signal behavior at the expense of small-signal performance. Noise performance is not seriously degraded as compared with the conventional OTA, as Table I reflects.

Measurements for supply voltages down to ± 0.65 V were also performed, showing correct operation, but the input range available decreases by the same amount as the supply voltage does.

TABLE I
MEASURED PERFORMANCE PARAMETERS OF THE OTAS

PARAMETER	Class A OTA	OTA Fig. 3(a)	OTA Fig. 3(b)	OTA Fig. 3(d)
Slew Rate (positive)	0.35 V/μs	100 V/μs	92 V/μs	42 V/μs
Slew Rate (negative)	-0.4 V/μs	-78 V/μs	-76 V/μs	-80 V/μs
Pos. settling (1%)	3.1 μs	29 ns	66 ns	100 ns
Neg. settling (1%)	3.6 μs	57 ns	62 ns	33 ns
GBW	200 kHz	725 kHz	410 kHz	470 kHz
Phase margin	90º	89.5º	90º	90º
Output Noise (1-MHz band)	223 μV_{rms}	230 μV_{rms}	230 μV_{rms}	252 μV_{rms}
THD @ 100 kHz, 0.9V_{pp}	-40 dB	-56 dB	-43 dB	-41 dB
Dynamic range	63 dB	66 dB	63.7 dB	62.5 dB
DC gain	30 dB	43 dB	37.5 dB	37.5 dB
CMRR	54 dB	68 dB	70 dB	69 dB
PSRR+ (dc)	48 dB	55 dB	50 dB	57 dB
PSRR- (dc)	44 dB	58 dB	53 dB	46 dB
Static power consumption	80 μW	120 μW	120 μW	140 μW
Die area	0.011 mm^2	0.024 mm^2	0.024 mm^2	0.042 mm^2

V. CONCLUSION

A novel family of CMOS class AB OTAs, based on the combined use of adaptive biasing and local common-mode feedback, has been fabricated and tested. The technique employed leads to a significant increase in slew rate and fast settling, improving current efficiency and maintaining low noise and very low static power consumption. The principle proposed is completely general and can be extended to virtually any class AB input stage by properly including LCMFB. Various topologies have been presented and implemented in a 0.5-μm CMOS technology, achieving near-optimal current efficiency, increasing slew rate by more than two orders of magnitude, and increasing GBW up to a factor 3.6 compared to the conventional OTA with the same dimensions and quiescent currents. Among them, as theoretically predicted in Section III-D and experimentally verified from Table I, the circuit of Fig. 3(a) shows the best overall performance, in terms of slew rate, GBW, and settling time. The circuits proposed can find application in low-voltage low-power switched-capacitor circuits and in buffers for testing mixed-signal circuits.

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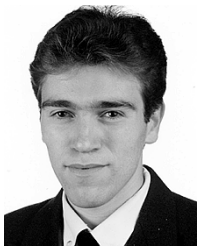

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