A High-Performance Micropower Switched-Capacitor Filter

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Abstract—**MOS technology scaling requires the use of lower supply voltages. Analog circuits operating from a low supply and achieving a sufficiently large dynamic range must be designed if analog/digital interfaces are to be implemented in scaled technologies. This paper describes a high-performance fifth-order low-pass switched-capacitor filter operating from a single 5-V supply. The filter uses a fully differential topology combined with input-to-output class *AB* amplifier design, dynamic biasing, and switched-capacitor common-mode feedback (CMFB). An experimental prototype fabricated in a 5-μm CMOS technology requires only 350 μW of power to meet the PCM channel filter requirements. Typical measured results are: a dynamic range of 92 dB, a supply rejection (PSRR) of 40 dB over the entire Nyquist range, and a total harmonic distortion (THD) of −73 dB for a 2-V rms differential output signal. The chip active area is about 3900 mil^2.**

I. Introduction

THE PERFORMANCE of switched-capacitor filters has steadily improved during the last several years, primarily as a result of improvements in the performance of CMOS operational amplifiers. This improvement has been particularly evident in the PCM channel filter application [1]–[6]. However, the most recent commercial PCM filter implementations still require a power-per-pole of about 1 mW and operate from a ±5 V supply. It has recently been shown [20], [21] that, from a fundamental standpoint, the absolute minimum achievable power dissipation in a voice-band filter with a dynamic range of 90 dB in a 3-μm technology operated from a ±5 V supply is less than 1 μW per pole. A large margin for improvement in power consumption over existing filter designs is therefore possible in principle. The realization of such a reduction, while maintaining high-performance levels, would have important implications in the realization of battery-operated analog/digital interfaces.

A second important consideration in the realization of switched-capacitor filters is the fact that the technological scaling of the mainstream MOS technologies dictates the use of lower power-supply voltages [7]. This fact, and the need for an analog/digital compatible technology, create a strong motivation for developing new analog circuit techniques suitable for low-voltage operation.

Recently several circuit approaches to the implementation of low-power MOS switched-capacitor filters have been described [8]–[14], some of them operating off a low power-supply voltage. These, however, have been intended for applications requiring limited dynamic range and power-supply rejection, and are not suitable for high-performance applications such as PCM telephony. This paper describes a fifth-order CMOS PCM channel filter operated from a single 5-V supply and dissipating about 70-μW per pole which embodies a combination of circuit techniques including input-to-output class *AB* amplifier design, fully differential topology, dynamic biasing, and switched-capacitor common-mode feedback. These techniques provide performance comparable or improved with respect to current 10-V commercial realizations, while dissipating much less power and operating on a 5-V power supply.

The paper is organized as follows. In Section II the fundamental limit to the achievable power dissipation for a low-pass switched-capacitor filter of given dynamic range is computed and compared with the actual value in commercially available devices. In Section III a new class AB operational amplifier, which represents the core of the filter reported in this paper, is described in detail. Section IV discusses the structure of the fifth-order switched-capacitor low-pass filter prototype which has been used to test the level of performance achievable with the new design. Finally, Section V presents some experimental results for both the filter and the op amp which demonstrates that high performance in analog circuits can be preserved when the supply voltage is reduced.

II. Limits to Power Dissipation and Dynamic Range

Power consumption reduction is always a major issue in VLSI systems. Present commercial switched-capacitor filters consume far more power than the theoretical minimum required. For this reason, this section examines some fundamental limitations to the achievable minimum power dissipation for a low-pass switched-capacitor filter of given dynamic range. This analysis has been carried out in detail in a previous paper [20], [21], and in this section only the main results are summarized stressing their intuitive interpretation.

In present day switched-capacitor filters, the quiescent dc bias power drawn by the operational amplifiers is normally much larger than the dynamic power drawn from

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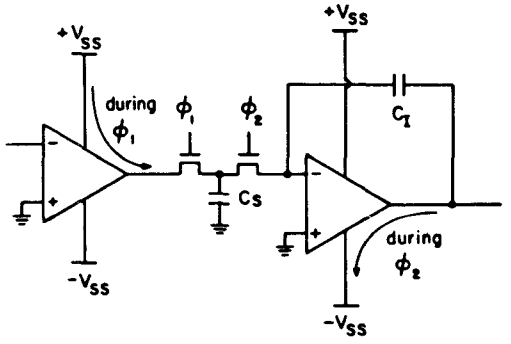


Fig. 1. Minimum power dissipation for a switched-capacitor integrator.

the supply in order to charge and discharge the sampling and integrating capacitor within the filter. We assume for this analysis, however, that, through improved circuit techniques, the op amp static power dissipation can eventually be reduced to the point of being negligible with respect to the dynamic power. This condition can be approached, in principle, by appropriate use of class B amplifier architectures. The situation is then analogous to that of a CMOS logic gate. Fig. 1 shows the flow of power from the supplies during one clock period for a switched-capacitor integrator. During phase 1 the positive supply charges the sampling capacitor via the previous switched-capacitor integrator, and during phase 2 the energy stored on the sampling capacitor is discharged by the feedback action of the second op amp through the integrating capacitor to the negative supply. Assuming that a full swing sinusoid of frequency f is present at the output of the integrator, the minimum power dissipation is proportional to the maximum energy that can be stored on the integrating capacitor times the frequency of the signal. Here it is important to emphasize that the power dissipation is proportional to the frequency of the signal and not to the frequency of the clock as in a CMOS gate. As an example this power is on the order of 1–2 μW per integrator for a typical switched-capacitor voice-band filter.

In order to reduce the power consumption, for a given frequency band of interest, the size of the integrating capacitor should then be reduced. The integrating capacitor is, however, constrained to be larger than some minimum value in order to achieve the required dynamic range due to the kT/C noise contribution. This should appear intuitively correct if it is noticed that, since in a switched-capacitor filter signals are represented as energy stored on capacitors, increasing the maximum energy that can be stored is equivalent to increasing the maximum signal energy level that the filter can process and therefore is equivalent to increasing the filter dynamic range. In fact, the dynamic range is related to the ratio of maximum stored energy to thermal energy, kT dictating a minimum capacitor size for a given supply voltage to achieve the required filter dynamic range.

By combining these two results, and applying them to the case of a low-pass filter implemented using switched-capacitor integrators, a plot of achievable signal-to-noise ratio versus minimum power dissipation for a low-pass

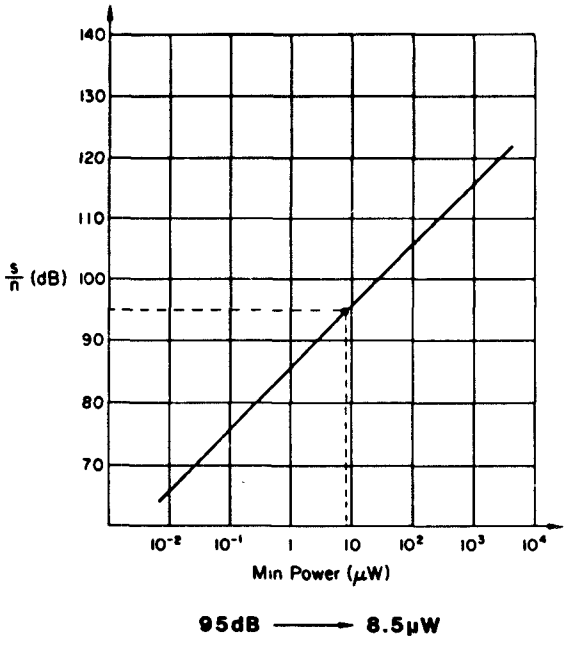


Fig. 2. Minimum power dissipation versus dynamic range for a 3.4-kHz fifth-order low-pass switched-capacitor filter

filter can be obtained given the value of the filter band edge. In Fig. 2 the case of a fifth-order filter with a 3.4-kHz bandwidth is shown. A dynamic range of 95 dB requires only 8.5 μW of power. Commercially available switched-capacitor PCM filters of similar performance use almost three orders of magnitude more power. Part of the discrepancy between theoretical and actual results is due to the fact that the above analysis neglects the noise contribution associated with the op amp (white and $1/f$ noise). This, however, can only account for a factor of two or so. A very large improvement is therefore feasible if op amps which are more efficient and achieve a signal swing closer to the supply voltage are designed.

III. Operational Amplifier Architecture

As just illustrated, op amp power consumption tends to dominate in typical filters. Next the design of a low power class AB op amp is described.

The new circuit configuration is based on four main concepts. The first is fully differential architecture which results in better swing and supply rejection. A class AB structure is used for low power dissipation. A single-stage topology with dynamically biased cascode is used for optimum current drive capability and output swing. A switched-capacitor common-mode feedback is used for minimum power. These feature will be discussed in detail in the following sections.

A. Fully Differential Topology

A fully differential switched-capacitor integrator is shown in Fig. 3. The two input voltages V_{in}^{+} and V_{in}^{-} are symmetrical with respect to the common-mode input voltage V_{cm}, and the two output voltages V_o^{+} and V_o^{-} are symmetrical

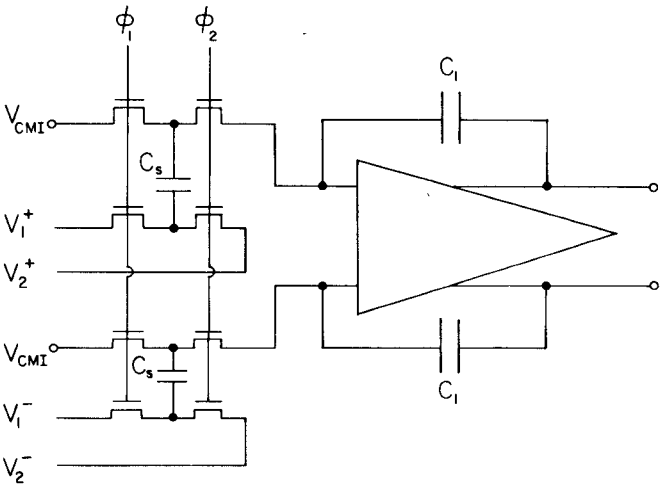


Fig. 3. Fully differential switched-capacitor integrator.

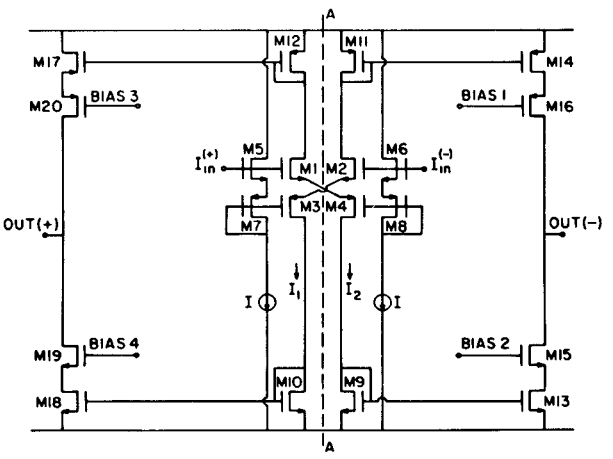


Fig. 4. Simplified schematic of the class AB amplifier.

with respect to the common-mode output voltage V_{cmo}. This structure doubles the output swing, which is of paramount importance for low-voltage applications, and provides a reduction on the sensitivity to supply and clock noise so that good PSRR can be obtained without having to decouple the input summing nodes from the supplies as it is instead required in the single-ended case. This results in a simplified input structure much more suitable for low-voltage design. Furthermore, a fully differential approach allows the designer to independently choose the value of the input and output common-mode voltages (V_{cmi} and V_{cmo}) for optimum performance. Although for maximum swing V_{cmo} should be equal to half of the total supply voltage, the same may not be the case for V_{cmi}. In the present design, in fact, V_{cmi} is higher than V_{cmo} by an n-channel threshold voltage.

The main disadvantage of the fully differential approach is the increased power and area requirement; however, in this design an efficient common-mode feedback (CMFB) circuit limits the power consumption increase to approximately 40 percent, while the total area increase is about 60–70 percent, with respect to a corresponding single-ended realization.

B. Class AB Single-Stage Configuration

Reduction of the quiescent power consumed by the op amp while retaining sufficient speed can be obtained by using a class AB configuration. Fig. 4 shows a simplified schematic of the class AB amplifier used in the filter without CMFB circuit. This circuit is a modified version of a previously proposed structure [18]. The circuit is perfectly symmetric about the axis $A-A$. For zero applied differential input signal, the two matched current sources I uniquely define the circuit quiescent current level. In fact, if for simplicity it is assumed that the four NMOS input devices are identical, and the same is true for the four PMOS devices, then $I_1 = I_2 = I$. Furthermore, since all current mirrors have a gain of 1, the quiescent current in the output branches is also equal to I. It follows, therefore that the quiescent power consumption in the circuit is precisely controlled by the two matched current sources in the input stage. The dynamic behavior of the circuit is shown in Fig. 5.

In response to a large positive differential input signal, current I_1 goes practically to zero. As a consequence, half of the devices in the circuit become cut off and have not been shown on Fig. 5(a). Current I_2, on the other hand, increases to a peak value which, in principle, is only limited by the value of the input voltage applied. The same current is mirrored to the outputs and can quickly charge and discharge the load capacitance. The comparison between the current–voltage characteristic of a class A and a class AB amplifier can be seen from Fig. 5(b). Notice that, in the example shown, for an input voltage of 300 mV the current in the class AB circuit is already several times larger than the current in the class A circuit. These values are representative of the actual behavior of the circuit reported in this paper.

Although in the above consideration it was assumed that the peak value for current I_2 in the class AB circuit of Fig. 5 is only a function of the applied input voltage, in practice another limiting factor is the total supply voltage. In fact as the current level increases, the sum of the voltage drops across devices $M1$, $M4$, $M9$, and $M14$ in Fig. 5 also increases, until it is equal to the total supply voltage. At this point, some of the devices ($M1$ or $M4$ or both) enter the linear region of operation, and the current level becomes practically constant independently of the value of the input voltage. This problem becomes more and more severe as the supply voltage is reduced, and represents the limiting factor to the maximum achievable peak current for a 5-V total supply voltage. The achievable value for the peak current is also strongly dependent on the value of the input common-mode voltage V_{cmi}. An optimum choice of the value of V_{cmi} is important in order to obtain the best possible performance in the op amp. In fact, increasing V_{cmi} by one n-channel threshold voltage above the middle point between the two supplies, as allowed by the fully differential configuration, gives more than a threefold increase on the achievable peak current level.

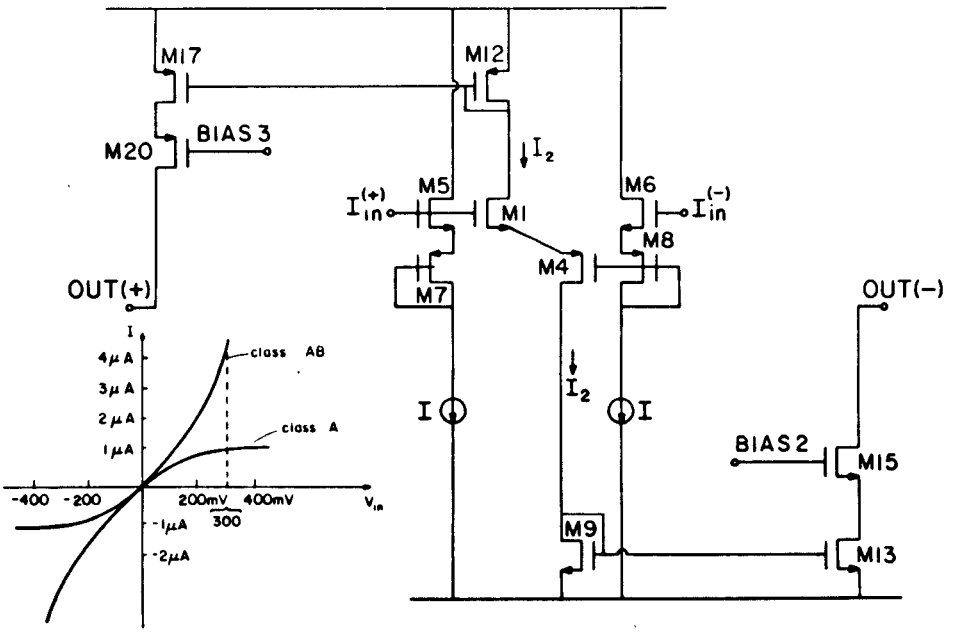


Fig. 5. Active portion of the amplifier for a positive input signal.

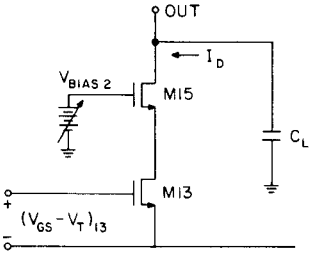
By utilizing a class *AB* configuration, a saving on the quiescent power dissipation for a given speed can therefore be achieved. Furthermore, the low quiescent current level on the output devices improves the voltage swing, and gives a larger dc gain. The class *AB* structure, however, has also some disadvantages. In particular it tends to be more complicated, and makes the problem of designing the CMFB circuit more difficult.

A single-stage configuration is particularly suitable for class *AB* operation. Also it has good power-supply rejection at high frequencies (beyond the dominant pole) and gives no high-frequency second-stage noise contribution, an effect which can greatly reduce the dynamic range of a sampled data system due to aliasing effects. Furthermore, in the present design the load capacitance is enough to guarantee stable closed-loop response, so that no extra compensation is required. The main drawback of the single-stage topology, particularly for low-voltage applications, is the reduced output swing due to the cascode devices. However, as shown below, the significance of this problem can be reduced by careful design.

In order to take full advantage of the class *AB* structure the amplifier must be able to deliver all of the peak input current to the load, without unacceptably compromising the output voltage swing. This requires use of a novel biasing scheme for the cascode devices as explained in the following section.

C. Dynamic Biasing

The necessity of adaptively biasing the cascode current mirrors in the amplifier is illustrated by the circuit of Fig. 6. Fig. 6(a) shows the two output devices of the NMOS cascode current mirror, which is active for a positive input signal. Fig. 6(b) is a table of value for the $V_{GS} - V_T$ of the two devices together with the minimum value of V_{BIAS2} required to keep both devices in saturation for two different conditions of operation. In the first column the current through the two devices is equal to the quiescent value. In the second column the current through the two devices is equal to the peak value that occurs during the transient resulting from applying a full swing signal at the input of the circuit. The numbers on the table are representative of the actual values for the amplifier reported in this paper.



(a)

	Quiescent	Max
$(V_{GS} - V_T)_{13}$	180mV	1.2Volts
$(V_{GS} - V_T)_{15}$	100mV	700mV
Required $V_{BIAS\,2}$	V_T + 280mV	V_T + 1.9Volts

(b)

Fig. 6. Output devices of an NMOS current mirror.

To obtain a large output swing V_{BIAS2} must be as small as possible, and the minimum possible value that guarantees proper operation of the circuit is, from the first column of Fig. 6(b), equal to 280 mV more than the value of the threshold voltage of device *M*13. This is because to obtain the full gain of the circuit it is necessary to insure

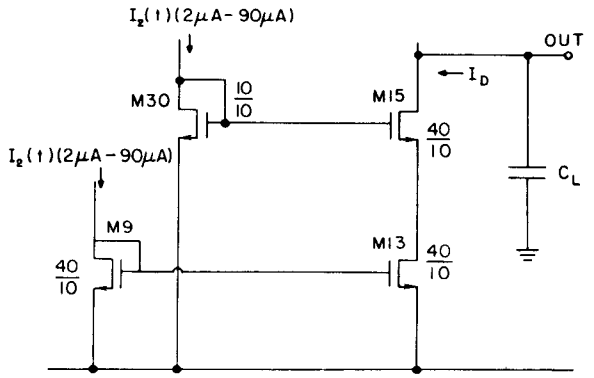


Fig. 7. Complete schematic of NMOS dynamically biased current mirror.

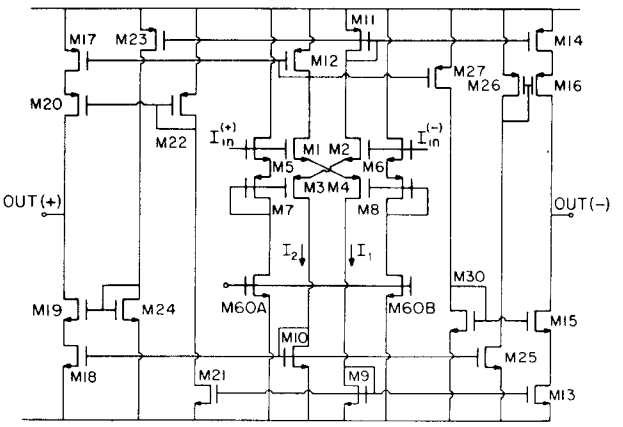


Fig. 8. Detailed schematic of the entire amplifier without CMFB

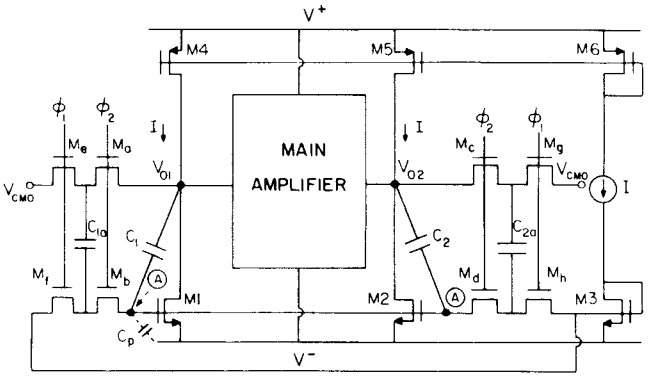


Fig. 9. Simplified dynamic common-mode feedback circuit.

that both $M13$ and $M15$ are in saturation at least in the quiescent state, i.e., when all transients have died away. For this value of V_{BIAS2}, however, as the output current increases $M13$ quickly enters the linear region of operation and the current limits to a value much smaller than the peak current in the input stage.

To guarantee full current driving capability to the load, $M13$ must be kept in the saturation region of operation during the entire transient. This require a value of V_{BIAS2} greater than or equal to the value shown in the second column of Fig. 6(b), i.e., 1.9 V more than the value of the threshold voltage of $M13$. Notice that V_{BIAS2} in the two cases differs by more than 1.6 V. In a fixed bias condition, therefore, there is a basic conflict between maximum current driving and maximum swing and whichever value of the bias voltage V_{BIAS2} is used between the two extreme cases shown on the table will result in a severe degradation of the overall performance of the circuit.

The solution to the problem is to vary V_{BIAS2} during the transient to simultaneously obtain optimum swing and full current drive capability. A simple way to achieve such a variable bias scheme is shown in Fig. 7. The input current $I_2(t)$ during the transient is assumed to varies from 2 μA to a peak value of 90 μA as an example. $M9$, $M13$, and $M15$ make up the NMOS current mirror and for simplicity are shown to have the same size. $M30$ has an aspect ratio 4 times smaller than the other devices. Assuming that the current on $M30$ and $M9$ is the same, a high swing cascode [17] current mirror results where $M13$ is biased at the edge of the linear region with its drain one threshold voltage lower than its gate. This bias condition gives the maximum possible output swing while, at the same time, guarantees a current gain of 1 in the mirror and a very large output resistance at the output node. By forcing $M30$ and $M9$ to carry the same current during the all transient, the full 90-μA current driving capability is achieved together with the same output swing of a fixed bias cascode biased to carry only 2 μA of current. Since the voltage at the gate of the cascode device varies during transients, such a biasing scheme is called "dynamic biasing." Notice that, in actuality, the aspect ratio of $M30$ must be smaller than shown in the above example due to body effects and to guarantee some margin of safety in the V_{DS} of $M13$ even in the presence of process variations.

Fig. 8 shows the entire amplifier schematic without common-mode feedback and illustrates how the two tracking currents, that are necessary for the proper operation of the dynamic biased current mirrors, can be easily generated. There are two p-type and two n-type dynamically biased cascode current mirrors at the top and bottom of the figure. As an example, consider the bottom right one. The current in $M30$ is forced to track the current in $M9$ by mirroring I_2 from the top via current mirror $M12$, $M27$.

D. Dynamic Common-Mode Feedback

The main drawback associated with the fully differential approach is the need for a CMFB circuit. Besides requiring extra area and power, the CMFB circuit limits the output swing, increases the noise, and slows down the op. amp. These are particularly undesirable effects in a low-voltage low-power system. The design reported here uses a switched-capacitor CMFB circuit similar to one proposed by Senderowicz *et al.* [3]. A simplified schematic of the circuit architecture used in this design is shown in Fig. 9. Capacitors $C1$ and $C2$ provide an ac feedback path from the two outputs of the op amp V_{o1} and V_{o2} to the feedback node A. The common-mode gain from node A to the output is very large and negative, while the differential gain

from node A to the output is ideally zero. This implies that the common-mode output voltage is kept at an almost constant value while, at the same time, the op amp differential gain is almost uneffected by the CMFB circuit. The dc value of the common-mode output voltage is, however, not well defined. It depends on the initial voltages across capacitors C_1 and C_2. The purpose of C_{1a} and C_{2a} is to establish the voltage drops across C_1 and C_2 that gives the desired common-mode output, and to periodically restore these voltages to compensate for leakages. In a switched-capacitor integrator C_{1a} and C_{2a} are switched-in on the phase opposite to that associated with the input signal.

This CMFB circuit is particularly suited for low-voltage low-power applications for two main reasons. First, it does not require any extra power consumption, with the exception of the replica circuit that defines the proper value of V_A ($M3$, I, and $M6$) which is, however, shared by all the op amps. Second, it does not degrade the differential output swing since the level shift operation performed by the capacitor C_1 and C_2 is not limited by the voltage supplies.

Although the maximum current that the CMFB circuit can supply is quite large for a positive signal, for a negative signal it is limited to $2I$ (about 2 μA). This makes the CMFB circuit unacceptably slow for the case of a negative common-mode output transient. However, by chosing the device sizes in such a way that the p-type current mirrors are faster than the n-type current mirrors, all common-mode output transients are guaranteed to have a positive polarity and the CMFB circuit is guaranteed to always work at its maximum speed. It turns out that the above choice of device channel lengths is also desirable from noise and speed considerations, as explained in the next section.

TABLE I
AMPLIFIER DEVICE SIZES

DEVICE	Z(μm)	L(μm)
M 1	180	6
M 2	180	6
M 3	140	6
M 4	140	6
M 5	150	6
M 6	150	6
M 7	200	6
M 8	200	6
M 9	22	10
M10	22	10
M11	29	7
M12	29	7
M13	22	10
M14	29	7
M15	22	6
M16	29	6
M17	29	7
M18	22	10
M19	22	6
M20	29	6
M21	20	9
M22	6	12
M23	28	6
M24	6	14
M25	20	9
M26	6	12
M27	28	6
M30	6	14

TABLE II
AMPLIFIER SPECIFICATIONS

CORE AMPLIFIER SPECIFICATIONS (0-5 Volts Supply) 100μW Quiescent Power Dissipation	
DIFFERENTIAL GAIN	> 10 000 *
UNITY GAIN FREQUENCY	2 MHz *
NOISE	140 nV/$\sqrt{Hz}$ 1KHz 50 nV/$\sqrt{Hz}$ white
OUTPUT SWING	0 5 Volts from Supply *
AREA	300 mils²

* Inferred from filter measurement

E. Noise Considerations

The noise performance of the amplifier is of particular concern since both low voltage supply and low power consumption tend to degrade the dynamic range. For optimum noise performance the input devices should be as large as possible. Furthermore, the input structure should be as simple as possible, and the input referred noise due to all the devices, other than the input ones, should be made as small as possible (ideally negligible).

In this design, the input structure ($M1-M8$) is much more complicated than the classical source-coupled pair (eight devices instead of two). However, the noise power associated with each one of the eight input devices should be divided by 4, when referred back to the input node, since their noise propagates only through one of the two signal paths while the input signal propagates through both. The overall input referred noise produced by $M1-M8$ is, therefore, equivalent to that of one n plus one p device which is comparable to that of a source-coupled pair.

The noise contribution of all the devices, other than the input ones, is next considered. First notice that, as in the case of the input devices, they only affect one signal path and therefore their noise power contribution should be divided by 4 when referred back to the input. Notice that this would not be the case if the amplifier was operated single ended. Furthermore the ratio of the noise power contributed by one of these devices over that of an input transistor is inversely proportional to the ratio of their transconductances for the white component and inversely proportional to the ratio of the square of the channel lengths for the $1/f$ component [19].

In order to simultaneously reduce both kinds of noise, the channel length of the current-mirror devices should be made as long as possible. This increases the amplifier voltage gain but reduces the frequency of the first non-dominant pole. However, because of the fact that p-type devices are slower but less noisy than n-type devices [14], it is possible to use devices close to minimum size in the p-type current mirrors (while the devices in the n-type

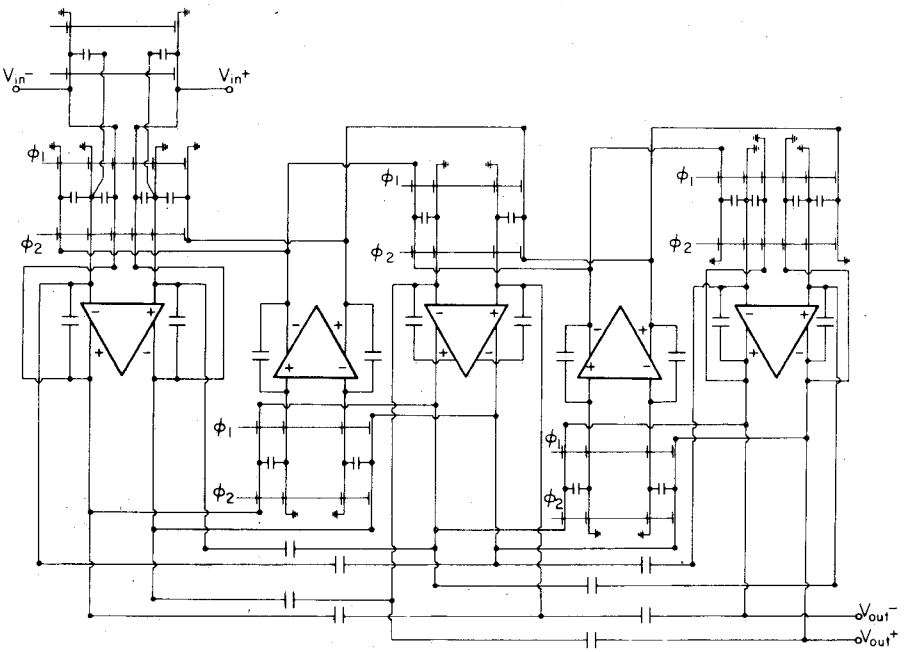


Fig. 10. Full schematic of the low-pass filter prototype.

current mirrors are longer). This achieves good speed in the circuit without appreciably degrading the overall noise performance. In this design the noise contributed by all devices other than the input ones is only about 15 percent of the total for both $1/f$ and white components while at the same time the frequency of the second pole is kept within 40 percent of the value achievable by using all minimum channel length devices. It is interesting to note that, to achieve this result, the device length is such that the n-type current mirrors are slower than the p-type ones.

As a final point notice that since the cascode devices $M15$, $M16$ give a negligible noise contribution, their channel length can be made very short (consistent with the gain requirement) thereby improving the frequency response.

F. Op Amp Summary

The device sizes for the circuit of Fig. 8 are shown in Table I, and the main amplifier performance for a total supply of 5 V and 100-μA power dissipation is shown in Table II. Some of the entries on the table where not measured directly but inferred from the filter results. Notice the very good output swing particularly for a cascoded output. The relatively large area is due to the fully differential topology. In fact, the dynamic common-mode feedback circuit alone takes more than one-third of the total amplifier area.

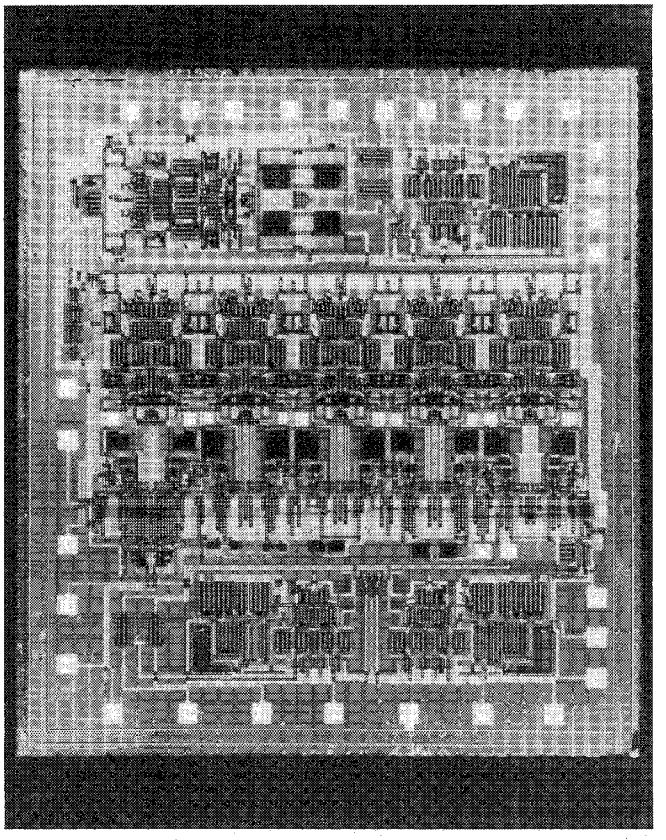


Fig. 11. Chip microphotograph.

IV. Prototype Filter Description

In order to test the performance achievable with the new op amp, a low-pass switched-capacitor filter prototype was built and will be described next.

A full schematic for the realized low-pass switched-capacitor filter is shown in Fig. 10. It is a fifth-order elliptic filter with four transmission zeros that requires a total of five op amps. The filter uses the standard active ladder architecture, for its low sensitivity to parameter variations, [15] and utilizes parasitic-free bottom-plate switched-capacitor integrators [4]. The 6-dB signal loss associated with the ladder structure is compensated by

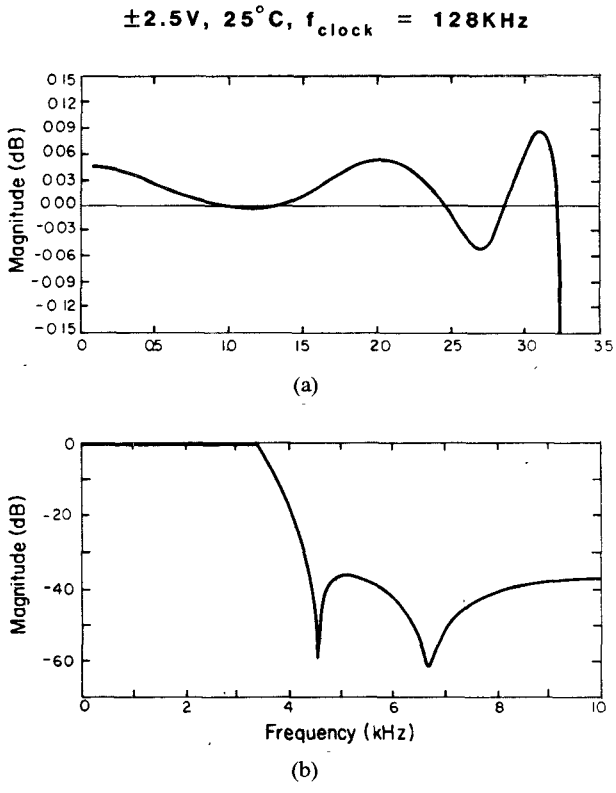


Fig. 12. (a) Detailed passband response. (b) Coarse frequency response of the filter.

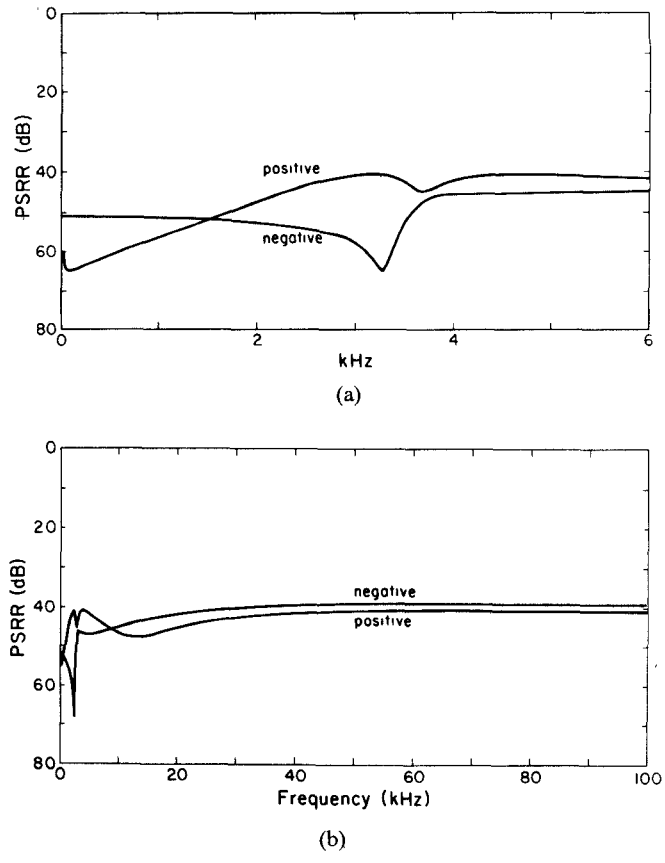


Fig. 13. Positive and negative PSRR: (a) in the 0–6 kHz range, and (b) in the 1–100 kHz range.

adding an extra sampling capacitor at the input which gives a gain close to 0 dB in the passband. This causes some peaking (less than 6 dB) at the internal nodes near the bandedge which degrades the filter linearity for large inputs at frequencies close to the band edge. On the other hand, no extra amplification is needed at the output and the overall noise is reduced.

The two-phase clock is externally supplied with two on-chip inverters providing the two-clock complements necessary to drive CMOS transmission gates which are implemented at all output node due to the large swing. The input is supplied differentially to the chip, and the differential to single-ended conversion is done off chip.

In order to be able to provide the output signal off-chip, a new low-voltage low-power buffer amplifier was designed and integrated on the chip prototype. The amplifier was designed to drive a capacitive load of up to 100 pF and/or a resistive load of 10 kΩ or more with a power dissipation from a 5-V supply of only 350 μW, and a settling time to an accuracy of 0.1 percent for a 2.5-V step of less than 3 μS.

A microphotograph of the experimental chip is shown in Fig. 11. A p-well 5-μm CMOS process was used. The process allows for a single level of metal and has a minimum channel length of 5 μm, device oxide thickness of 400 Å, and capacitor oxide thickness of 1000 Å. The chip layout is almost perfectly symmetrical to maximize cancellation of the spurious signals coupled into the system. Some small asymmetries were impossible to avoid (cross-coupled devices), but they were all limited to the metal layer. The power level in both the filter and the amplifier can be externally controlled.

The central part of the picture is the fifth-order filter which has an active area of 3500 mil^2. In the bottom part of the picture are visible the two amplifiers designed to buffer the output of the filter from outside the chip. Two circuits are necessary because the signal is taken off-chip differentially. The top portion of the chip shows some test structure. Although the test buffer amplifier was functional and showed performance corresponding to the design values [16], due to some layout errors in the interconnections of the buffers at the filter output these circuits had to be bypassed and all the measurements reported were taken using some source followers externally biased as output buffers.

V. Experimental Results

Both detailed and coarse filter response are shown on Fig. 12 for a total power consumption of 350 μW. The supply used is ±2.5 V, the clock frequency is 128 kHz. The total in-band ripple is 0.13 dB. The transmission zeros are at 4.5 and 6.7 kHz and the attenuation in the stopband is more than 35 dB. This agrees well with the simulation results obtained from the DIANA program [22]. The power supply rejection ratio for both supplies is shown in Fig. 13(a) for the frequency interval 0–6 kHz and in Fig. 13(b) for the interval 1–100 kHz. At 1 kHz the PSRR is well

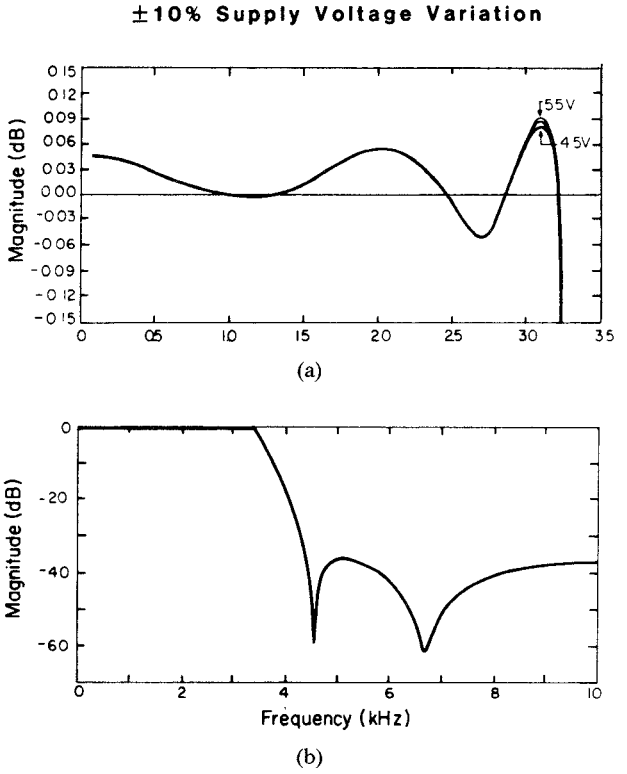


Fig. 14. Changes in the (a) passband response and (b) overall filter response for ±10 percent variation in the supply voltage.

above 50 dB for both supplies and stays close to 40 dB up to 100 kHz.

The effect of a ±10 percent variation in the total supply voltage is shown in Fig. 14. The only variation that can be detected is in the detail passband plot and it occurs at the bandedge; however, it is only about ±0.01 dB. No appreciable change can be seen on a coarse scale. The position of the zeros is essentially unaffected by the change in supply voltage. The total *C*-message weighted integrated noise is 70 μV.

The total harmonic distortion for a 2-V rms differential output at 1 kHz is about −73 dB. The good linearity of the filter is further shown in Fig. 15 where the total harmonic distortion (THD) at the output for the nominal supply voltage of 5 V and a 1-kHz input signal is plotted versus the output signal amplitude. The THD stays below −40 dB up to a differential output of approximately 4.6-V peak (3.3 V rms), i.e., 200 mV from both supply rails. The large output swing is primarily due to the use of dynamic biasing for the cascode devices and to the fact that the CMFB circuit behaves linearly even for signals which are larger than the supplies. The linearity of the CMFB circuit also helps produce the low distortion achieved in the filter.

A summary of the achieved filter performance is shown in Table III. The operating conditions are a total supply voltage of 5 V, a clock rate of 128 kHz, and a power dissipation of 350 μW. The total measured *C*-message weighted noise of 70-μV rms combined with the maximum differential output swing that gives less than 1-percent THD for a 1-kHz signal of 3.3-V rms gives a dynamic range of 93 dB, which is comparable with the value achieved

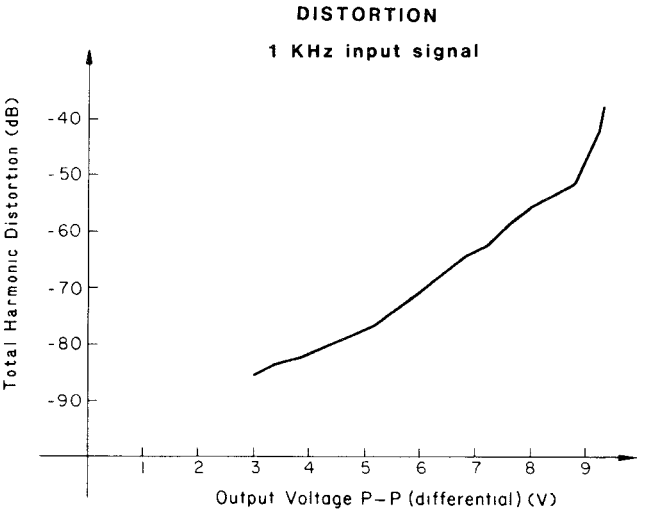


Fig. 15. Total harmonic distortion as a function of the output voltage for a 1-kHz signal

TABLE III
SUMMARY OF THE FILTER PERFORMANCE

25°C ±2.5 V f_{clk} = 128KHz		
PARAMETER	CONDITION	VALUE
MINIMUM POWER DISSIPATION	—	350μW
P S R R	1KHz +SUPPLY 1KHz −SUPPLY	56 dB 52 dB
TOTAL HARMONIC DISTORTION	2V rms differential output 1KHz	73 dB
IDLE NOISE	CMESSAGE WEIGHTED	70 μV
OUTPUT SWING DIFFERENTIAL	<1% THD	3 1(RMS)V
DYNAMIC RANGE	—	93 dB

by typical commercially manufactured filters operated from ± 5-V supplies and requiring 10–15 times more power than this device. Another point of interest is the low distortion achieved in the filter −73 dB for a 2-V rms differential output signal. One reason for this is the use of the fully differential topology as demonstrated by the results of Fig. 16, which shows the output spectrum for a 1-kHz pure sinusoidal input that gives a 4.4-V peak-to-peak differential output. This plot is obtained by feeding one of the two filter outputs directly to the spectrum analyzer without passing through the differential to single-ended converter. As can be seen, the only appreciable harmonic is the second one. On this plot the harmonic content of the differential output is depicted. The second harmonic is totally canceled out because of the symmetry of the struc-

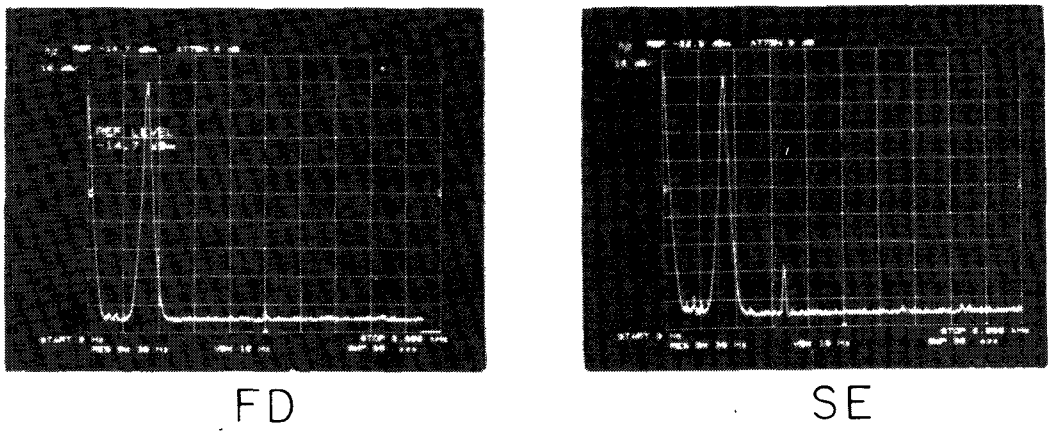


Fig. 16 Comparison between the harmonic distortion for a fully differential and a single-ended output for a differential output voltage of 4 4 p-p V.

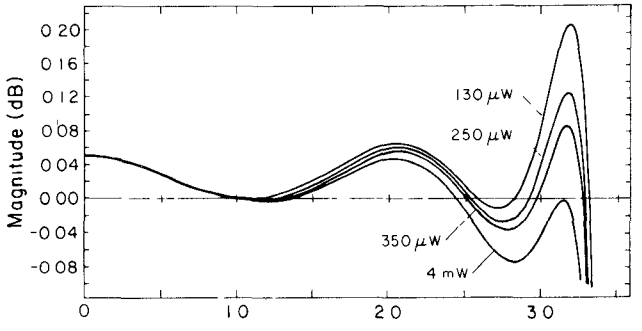


Fig. 17. Variation of the passband response for different power levels.

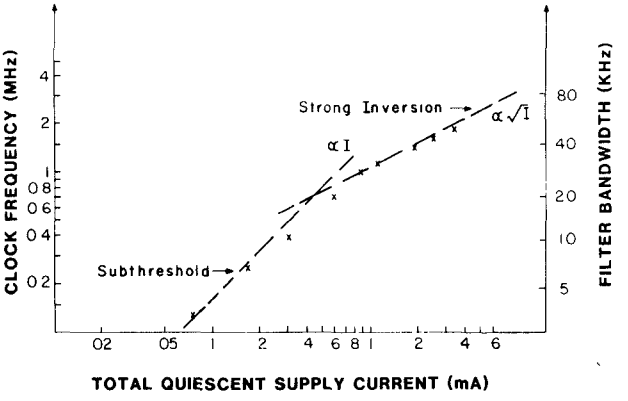


Fig 18. Maximum clock frequency versus required supply current.

ture. On the other hand, a small amount of third harmonic is now present. The total improvement in THD from right to left is more than 12 dB. The clock feedthrough for the two cases was also compared. For grounded inputs, which gives matched signal paths, the clock feedthrough in the fully differential case is 30 dB less than in the single-ended case.

Fig. 17 shows the change in the shape of the passband for different values of the total power dissipation. For very low power the filter is still functional but the op amp is not capable to settling very accurately within one phase of the clock and peaking occurs. However, channel filter requirement are met over a change in the power level of more than 40 to 1. Here the power level was varied by varying the bias current to the op amps with an external resistor.

The minimum value of the total supply voltage required for proper operation is approximately 3 V. A smaller value could be used if a low threshold process had been used instead of the conventional (not scaled) process featuring approximately ± 0.8-V thresholds.

Finally, Fig. 18 shows the total amount of supply quiescent current that is necessary for the filter to operate properly when the clock rate is increased. This experiment was carried out by chosing a value of the clock rate and then increasing the current level in the filter until the required ripple in the passband was obtained. The last point to the right shows that with a total supply quiescent current of about 3 mA, a 50-kHz filter could be obtained. At this clock rate (almost 2 MHz) the op amp must be able to accurately settle in about 200 ns. The change on the slope of the curve indicates that the input devices of the op amp move from the subthreshold to strong inversion as the current is increased from 60 μA to 3 mA.

VI. Conclusions

An experimental switched-capacitor filter has been described which shows that a dynamic range adequate for communications applications can be achieved when a total supply voltage of 5 V is used. Good PSRR up to high frequency and low power dissipation make this approach very suitable for operation as a part of a large digital/analog chip where noise immunity and power consumption reduction are of paramount importance. This circuit was implemented using 5-μm technology and requires 700 mil^2/pole. It is, however, projected that by using a 3-μm technology an area per pole of less than 200 mil^2 can be achieved without compromising the level of performance.

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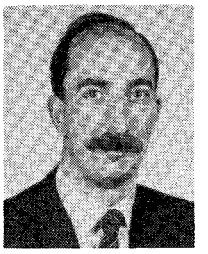

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