FAST-SETTLING CMOS TWO-STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS AND THEIR SYSTEMATIC DESIGN

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ABSTRACT

Comparing to single-stage OTAs, two-stage OTAs have higher gain and output swing, but more poles and zeros and thus have more complex settling behavior. Two structures of two-stage OTA that have good settling performance are introduced. By analyzing the settling behavior of the third order system, a set of poles and zeros parameters are extracted. A design procedure for minimum settling time of these two OTAs is described. Finally two design examples for minimum settling time are presented. These high-speed OTAs are suitable for high-speed switched-capacitor applications.

1. INTRODUCTION

Speed and accuracy are two of the most essential properties of analog circuits. In operational transconductance amplifiers (OTAs), settling time and DC gain are direct reflections of speed and accuracy. While pursuing the high specifications of analog circuits, fast settling and high DC gain of OTAs are often demanded at the same time. Especially in switched-capacitor circuits, settling performance is the most concerned parameter as the settling time determines the maximum clock frequency while the DC gain of the OTA determines the output accuracy [1].

For settling performance of a system, the single-pole system has the simplest settling behavior. Therefore, the single-stage OTA, which can be regarded as a first-order system in approximation, is the simplest OTA structure comparing to the multi-stage OTA in term of settling performance. The GBW of the amplifier determines the settling time solely. However, the DC gain that one stage can reach is limited. To achieve high DC gain with a single amplifier stage, some techniques are adopted, such as cascoding, gain-boosting and negative conductance compensation. However, gain-boosting technique suffers from the degrading of high-frequency performance and has the potential to be unstable. The negative conductance compensation is heavily relies on transistor matching. Of all these techniques, cascoding is widely used as it doesn't degrade the settling performance.

With the semiconductor processing development, the size of the transistor is continuously shrinking, making it possible to reach even higher unit-gain frequencies of the transistor. However, the intrinsic gain of the transistor, gm*ro, is also degrading. This makes the single-stage amplifier gain even lower. At the same time, the power-supply voltage is decreasing, making the output swing lower [2]. For widely used cascode structure, the output swing is limited as at least 4 transistors are in stack. These problems force the analog designer switching to multi-stage OTAs.

The main drawback of the multi-stage OTA is that the compensation is needed to avoid instability. Thus more poles and zeros are introduced and the settling time no longer depends on one pole frequency. This makes the design of the high-speed multi-stage OTA more difficult.

In this paper, the settling behavior of the third-order system is analyzed and an optimized set of system parameters is obtained. According to the obtained system parameters, a design method of optimizing the settling time is proposed. Finally, a design example is reported.

2. SETTLING BEHAVIOR ANALYSIS OF TWO TWO-STAGE OTAS

2.1. Ahuja style compensated OTA

The most popular two-stage OTA is the Miller compensated OTA. Moving the compensation capacitance to the source of the cascading transistor, the so-called Ahuja style compensated two-stage OTA is obtained, shown in Fig.1 [3]. The first stage is a telescopic cascode stage that provides high voltage gain, and the second stage is a common-source stage that provides high output swing. Of all the nodes, only node N_2 and output nodes are high impedance nodes. The poles and zeros formed by these two nodes are much smaller than the other nodes. To simplify the analysis, only the parasitic capacitances of these two nodes are taken into consideration. In real situations, the OTAs always operate in closed loop

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configurations, so the following analysis is based on a closed-loop configuration.

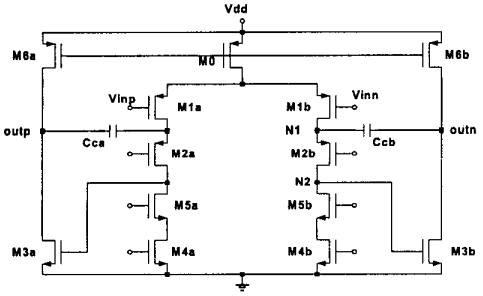

Fig. 1 The Ahuja style compensated two-stage OTA

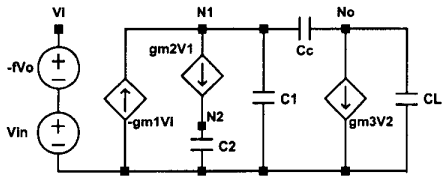

Fig. 2 Small-signal equivalent circuits of the Ahuja style compensated two-stage OTA

Fig.2 shows the small-signal equivalent circuit for pole and zero analysis. In the schematic, C_2 represents the parasitic capacitance of node N_2, C_1 represents the parasitic capacitance of node N_1 and C_L represents the parasitic capacitance of node N_o and the load capacitance. gm_1, gm_2 and gm_3 represent the transconductance of transistor M1, M2 and M3 respectively; V_1, V_2 and V_o represent the voltage of node N_1, N_2 and N_o. To simplify the expression, the bulk transconductance and Gds of all transistors are considered as zero. The node equations and the transfer function are:

$$\begin{cases} V_o sC_L + gm_3 V_2 + (V_o - V_1)sC_C = 0 \\ (V_o - V_1)sC_C + gm_2 V_1 + gm_1(V_{in} - fV_o) + V_1 sC_1 = 0 \\ V_2 sC_2 - gm_2 V_1 = 0 \end{cases} \quad (1)$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{\frac{gm_1}{C_2 C_T}(s^2 C_C C_2 - gm_2 gm_3)}{s^3 + \frac{[gm_2(C_L + C_C) - fgm_1 C_C]}{C_T^2}s^2 + \frac{gm_2 gm_3 C_C}{C_2 C_T^2}s + \frac{fgm_1 gm_2 gm_3}{C_2 C_T^2}} \quad (2)$$

Where $C_T^2 = C_1 C_L + C_1 C_C + C_L C_C$

2.2. Settling behavior of Ahuja style compensated OTA

In order to investigate the settling behavior, we convert the transfer function of the Ahuja style OTA to the following standard third-order system transfer function:

$$H(s) = \frac{k(z^2 - s^2)}{(s + \omega_{CL})(s^2 + 2\zeta\omega_n s + \omega_n^2)} = \frac{k(\gamma^2\zeta^2\omega_n^2 - s^2)}{(s + \alpha\zeta\omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (3)$$

Where $z = \gamma\zeta\omega_n$ and $\omega_{CL} = \alpha\zeta\omega_n$

There are four system parameters, α, γ, ζ and ω_n in the transfer function. ω_n is called natural frequency and ζ is called damping factor. The physical explanation of these four parameters can be found in Fig. 3.

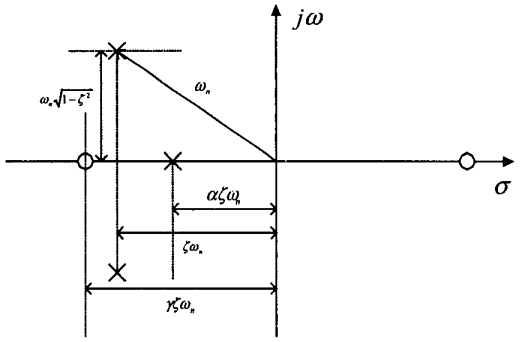

Fig. 3. Poles and zeros plot of a third order system

Now we try to find the relationship between the settling time and these four parameters. If we apply a step signal to this system, which is equivalent to multiply the transfer function by 1/s, the Laplace transform of the unit step, we obtain the response of this system in frequency domain. After taking the reverse Laplace transform, we obtain the time domain step response of the system [4]:

$$R(t) = A_{CL}\left\{1 - \frac{(\gamma^2 - \alpha^2)}{\gamma^2(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)}e^{-\alpha\zeta\omega_n t} - \frac{\alpha e^{-\zeta\omega_n t}}{\gamma^2(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)} \left[(\alpha - 2\zeta^2\gamma^2 + \alpha\zeta^2\gamma^2)\cos(\omega_n t\sqrt{1-\zeta^2}) + \frac{(1 - \alpha\zeta^2 + \zeta^2\gamma^2 - 2\zeta^4\gamma^2 + \alpha\zeta^4\gamma^2)}{\zeta\sqrt{1-\zeta^2}}\sin(\omega_n t\sqrt{1-\zeta^2})\right]\right\} \quad (4)$$

Where A_{CL} denotes the closed-loop gain.

$E(t) = \frac{R(\infty) - R(t)}{R(\infty)}$ is the settling error of time t to the final value.

$$E(t) = \left\{\frac{(\gamma^2 - \alpha^2)}{\gamma^2(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)}e^{-\alpha\zeta\omega_n t} + \frac{\alpha e^{-\zeta\omega_n t}}{\gamma^2(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)} \left[(\alpha - 2\zeta^2\gamma^2 + \alpha\zeta^2\gamma^2)\cos(\omega_n t\sqrt{1-\zeta^2}) + \frac{(1 - \alpha\zeta^2 + \zeta^2\gamma^2 - 2\zeta^4\gamma^2 + \alpha\zeta^4\gamma^2)}{\zeta\sqrt{1-\zeta^2}}\sin(\omega_n t\sqrt{1-\zeta^2})\right]\right\} \quad (5)$$

The analytical equation of settling error and system parameters has been found. However, this equation is too complex to see the relationship clearly. So it is explored

by numerical calculations. With the help of mathematics tools software, the settling error curves with different system parameter values can be drawn. For given settling error and time, the parameters can be found easily. All the figures are drawn versus time normalized to $\omega_n t$.

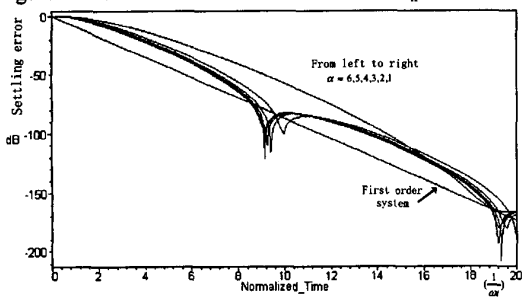

Fig. 4 Normalized settling time of the Ahuja style OTA for different α value (ζ=0.95 and γ=4)

Fig. 4 shows the settling error curves of the Ahuja style OTA for different parameters. The minimum settling time is achieved when α>2, ζ=0.95 and γ>4. From the curves one can clearly see that for –80 dB settling error, the settling time of the Ahuja style OTA is about 9 times of $1/\omega_n$, which is comparable to the first order system with the same ω_n.

2.3. Improved Ahuja style compensated OTA

If we move the compensation capacitance to the source of the load transistor, a new structure is formed, shown in Fig.5. The small signal equivalent circuits are shown in Fig. 6.

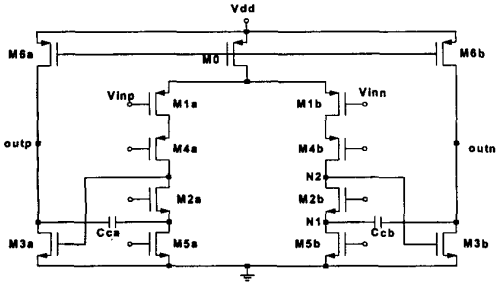

Fig. 5 The improved Ahuja style compensated two-stage OTA

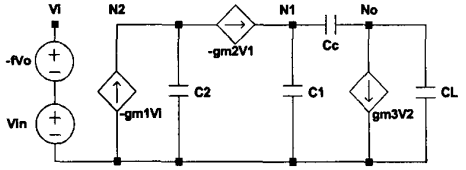

Fig. 6 Small signal equivalent circuits of the improved Ahuja style compensated two-stage OTA

Again, we have the node equations and the transfer function:

$$\begin{cases} V_o sC_L + gm_2 V_2 + (V_o - V_1) sC_C = 0 \\ (V_1 - V_o) sC_C + gm_2 V_1 + V_1 sC_1 = 0 \\ V_2 sC_2 - gm_2 V_1 + gm_1 (V_{in} - fV_o) = 0 \end{cases} \quad (6)$$

$$\frac{V_o(s)}{V_{in}(s)} = \frac{gm_1 gm_3 \frac{C_c + C_1}{C_1 C_T^2}\left(s + \frac{gm_2}{C_c + C_1}\right)}{s^3 + s^2 \frac{gm_3}{C_1 C_T^2}(C_2 C_1 + C_2 C_c) + s\frac{1}{C_1 C_T^2}[fgm_1 gm_3 (C_c + C_1) + gm_3 gm_2 C_c] + \frac{f}{C_1 C_T^2} gm_1 gm_2 gm_3} \quad (7)$$

Where $C_T^{\ 2} = C_1 C_L + C_1 C_C + C_L C_C$

We can see that there is only one zero in the transfer function of improved Ahuja style OTA.

2.4. Settling performance of the improved Ahuja style compensated OTA

The transfer function of the improved Ahuja style compensated OTA can be simplified as follows:

$$H(s) = \frac{k(s+z)}{(s+\omega_{CL})(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (8)$$

Based on this equation, using the same method, the step response of the improved Ahuja style compensated OTA can be calculated, shown bellow:

$$R_2(t) = A_{CL}\left\{1 - \frac{(\gamma-\alpha)}{\gamma(1-2\alpha\zeta^2+\alpha^2\zeta^2)} e^{-\alpha\zeta\omega_n t} + \frac{\alpha e^{-\zeta\omega_n t}}{\gamma(1-2\alpha\zeta^2+\alpha^2\zeta^2)}\right.$$
$$\left[\frac{2\gamma\zeta^3 - \alpha\gamma\zeta^3 + \alpha\zeta - \zeta - \gamma\zeta}{\sqrt{1-\zeta^2}} \sin(\omega_n t\sqrt{1-\zeta^2})\right. \quad (9)$$
$$\left.\left. -(1 + \alpha\gamma\zeta^2 - 2\gamma\zeta^2)\cos(\omega_n t\sqrt{1-\zeta^2})\right]\right\}$$

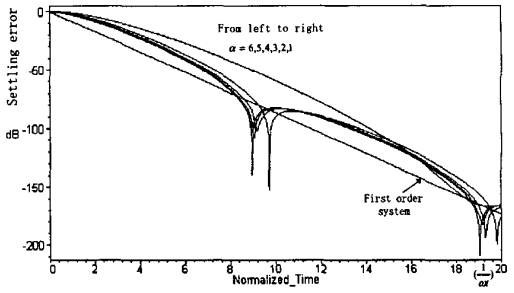

Fig. 7. Normalized settling time of the improved Ahuja style OTA for different α value (ζ=0.95 and γ=4)

Fig. 7 shows the settling error curves of the improved Ahuja style OTA for different parameters. The parameters to achieve the minimum settling time are the same with the Ahuja style OTA.

3. OPTIMIZATION FOR MINIMUM SETTLING TIME

From the previous analysis, we already have the system parameters for desired settling time and settling error. Now the problem is how to design the physical sizes of the transistors and the biasing currents.

3.1. Optimization procedure of the Ahuja style OTA

The optimization of the Ahuja style two-stage OTA can be start from the design equations extracted by matching the transfer function of the OTA with Eq. 3.

$$\begin{cases} (2+\alpha)\zeta\omega_n = \dfrac{gm_2(C_L+C_C)-fgm_1C_C}{C_1C_L+C_1C_C+C_LC_C} \\ \omega_n^2(1+2\alpha\zeta^2) = \dfrac{gm_2gm_3C_C}{C_2(C_1C_L+C_1C_C+C_LC_C)} \\ \alpha\zeta\omega_n^3 = \dfrac{fgm_1gm_2gm_3}{C_2(C_1C_L+C_1C_C+C_LC_C)} \end{cases} \quad (10)$$

These equations reveal the relationship between the device parameters and the system parameters. Among all the parameters, the system parameters, α, γ, ζ and ω_n are known. The load capacitance C_L is known too. The compensation capacitance C_C can also be determined before hand. The capacitances C_1 and C_2 are parasitic capacitances of the node N_1 and N_2 respectively and they can be related to the transistor sizes. So C_1, C_2 and all the transconductances can be expressed by transistor sizes. Theoretically, these equations can be solved and the sizes of the transistors can be obtained. However, practically, these equations are too complex to be solved. Again, numerical solution is taken to find the right sizes of the transistors.

3.2. Optimization procedure of the improved Ahuja style OTA

The design equations of the improved Ahuja style OTA can be found bellow:

$$\begin{cases} (2+\alpha)\zeta\omega_n = \dfrac{gm_2(C_2C_1+C_2C_C)}{C_2(C_1C_L+C_1C_C+C_LC_C)} \\ \omega_n^2(1+2\alpha\zeta^2) = \dfrac{fgm_1gm_3(C_C+C_1)+gm_2gm_3C_C}{C_2(C_1C_L+C_1C_C+C_LC_C)} \\ \alpha\zeta\omega_n^3 = \dfrac{fgm_1gm_2gm_3}{C_2(C_1C_L+C_1C_C+C_LC_C)} \end{cases} \quad (11)$$

The design procedure is the same with the Ahuja style OTA.

4. COMPARISON OF TWO TYPE OF OTAS

The poles and zeros parameters for these two OTA types achieving certain settling performance are almost the same. The difference takes place in the implementation of the circuits. To design a fast settling OTA, the large transconductance value is inevitable for transistor M2, as it drives the compensation capacitance, which is a relatively large capacitance. In the Ahuja style OTA, M2 are PMOS transistors, which need larger current and size to achieve the wanted transconductance, resulting into more power consumption. However, in the improved Ahuja style OTA, M2 are NMOS transistors, making things easier. This is the main difference between these two types of OTAs.

5. SIMULATION RESULTS

A simulation results using 0.25 micron CMOS process model are given in Table 1. To ensure high slew rate, the biasing current of the output stage must be high enough. The OTAs were designed with α=5, ζ=0.95 and γ=5.

Table 1 Simulation results
(Vdd=2.5V, Cload=3pF, f=0.75)

	Ahuja OTA	Improved Ahuja OTA
DC gain (dB)	66	72
Power consumption (mW)	30	25
GBW (MHz)	710	963
Settling time + slew time (ns) (0.6V step)	2.1	2.1

6. CONCLUSION

Considering gain and output swing performances, two-stage structures are good choices of OTA structures in deep sub-micron CMOS technology. By proper optimization, the settling performances of two-stage OTAs can be as good as the single-stage ones. Simulation results using 0.25 micron model show that these OTAs achieve good settling performances with reasonable power consumption. The design procedures are proved to be effective to design high-speed two-stage OTAs.

9. REFERENCES

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