Electrical Engineering (2006) 88: 509–517
DOI 10.1007/s00202-005-0306-2

ORIGINAL PAPER

S. M. Rezaul Hasan · Nazmul Ula

A novel feed-forward compensation technique for single-stage fully-differential CMOS folded cascode rail-to-rail amplifier

Received: 14 January 2005 / Accepted: 21 March 2005 / Published online: 20 December 2005

Abstract This paper presents a novel active and passive mixed feed-forward compensation technique for single-stage CMOS folded-cascode rail-to-rail operational trans-conductance amplifiers (OTA). Simulations using 0.5 μm Agilent CMOS process parameters indicate a phase margin of around 82° with an unity gain bandwidth of 320 MHz (@1.17 pF capacitive load including the device parasitics). Also, the compensated OTA provided over 60 dB DC-gain with rail-to-rail output voltage swing as well as wide input common-mode range. This ensures optimum step response (fast and accurate settling without ringing) for the feedback amplifier in switched-capacitor signal processing applications. An improved "fast sensing" common-mode feedback circuit with high common-mode gain is also used for the single-stage cascode OTA.

Keywords Single-stage rail-to-rail OTA · Phase margin · CMOS · Folded cascode · compensation

1 Introduction

Single-stage CMOS amplifiers (operational trans-condutance amplifiers, OTA's) are an integral part of today's numerous precision continuous-time and discrete-time analog signal processing integrated circuits. Although multi-stage (in particular two-stage) amplifiers are increasingly being considered in low-voltage applications, bandwidth considerations still make single-stage amplifiers more suitable for many high-speed wide-band applications [8]. The single-stage folded-cascode CMOS OTA is being used in many low-voltage high bandwidth applications. Although the single-stage OTA is inherently less prone to instability, most applications use the OTA in an "integrator" type feed-back configuration which can result in instability. This possible instability is likely to manifest under high-frequency operation. Although a fully differential folded-cascode amplifier does not suffer from "mirror pole" limitations, the folding node contributes a non-dominant parasitic pole [10] in addition to the dominant pole due to the RC time-constant at the output node due to the output load capacitance and the output impedance of the cascode. One of the "textbook style" technique for ensuring sufficient phase margin for feedback stability of this folded cascode is the use of additional load capacitance [10] to push the dominant pole towards the imaginary axis, thereby ensuring a smaller phase lag at the gain crossover point. Stability is thus achieved by sacrificing bandwidth. Many compensation techniques are well-known for double and multi-stage amplifiers based on the well-known miller compensation and its variations [1–4]. In addition, feed-forward compensation techniques for multi-stage amplifier [5] has also been recently reported. However, many of these topologies are not quite suitable for a single-stage cascode amplifier. The authors in [6] presented a feed-forward compensation technique for single-ended folded cascode using a feed-forward capacitor and active biasing, while, capacitive cross-coupled feed-forward compensation of fully differential folded-cascode was reported in [7], both requiring considerable compensation capacitor overhead. In this paper we discuss a simple feed-forward compensation technique using a combination of active and passive feed-forward components for the single-stage fully-differential folded-cascode rail-to-rail transconductor amplifier stage [13]. This technique does not involve the use of any pole splitting miller compensation and hence bandwidth is not sacrificed for increasing stability via increased phase margin. Instead, this technique involves the creation of LHP zeros to approximately cancel the phase-lag caused by the non-dominant parasitic poles at the folding nodes of the transconductor utilizing the inherent flexibility of the rail-to-rail OTA structure [13, 14] and appropriate

S. M. Rezaul Hasan (✉)
Computer Engineering,
Institute of Information & Mathematical Sciences,
Massey University, Auckland, New Zealand
Tel.: +64-9-4140800
Fax: +64-9-4418136
E-mail: hasanmic@massey.ac.nz

Nazmul Ula
Department of Electrical Engineering,
Loyola Marymount University,
Los Angeles, CA, USA

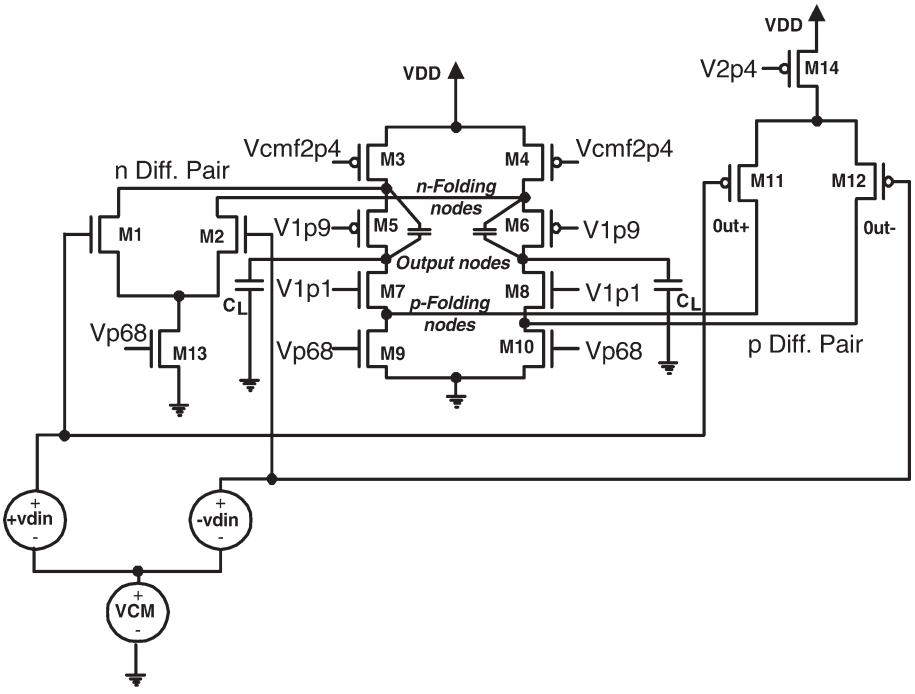

Fig. 1 Rail-to-rail OTA structure ("merged P-N CMOS folded cascode" architecture) with active and passive feed-forward (from the N-folding node to the output node)

device sizing. An improved common-mode feedback circuit with higher common mode gain is also used for the amplifier.

2 Novel feed-forward compensation technique

Figure 1 shows the circuit diagram of a fully differential CMOS folded cascode rail-to-rail amplifier (similar to [13]) which can be considered to be a "merged P-N CMOS folded cascode" topology containing two differential amplifiers merged together. Either differential amplifier can be viewed as a feed-forward circuit for the composite single-stage amplifier providing inherent active feed-forward compensation. Additional passive feed-forward compensation can be provided by way of a small value capacitance placed across the N-folding node (or the P-folding node) and the output. Consideration must be given to the amplifier's settling behavior in choosing this capacitance value (≈0.3 pF, possibly harnessed from the device parasitics). In order to elaborate the active compensation scheme, the rail-to-rail OTA of Fig. 1 can be described in detail as follows: MOSFETs M1, M2, M5 and M6 with fully differential NMOS cascode load devices M7, M8, M9 and M10 form a fully differential N-folded-cascode pair, which is blended with a second P-folded-cascode differential pair consisting of M11, M12, M7 and M8 with PMOS cascode load devices M3, M4, M5 and M6. The current sources (PMOS devices M3 and M4 and NMOS devices M9 and M10) and the cascode devices (PMOS devices M5 and M6 and NMOS devices M7 and M8) are thus *reused* as differential cascode loads. The overall output of the rail-to-rail OTA ("merged P-N CMOS folded cascode") topology is due to the superposition of the separate output contributions due to the two differential pairs. Let $H1(s)$ be the transfer function due to the N-differential pair, and, $H2(s)$ be the transfer function due to the P-differential pair, then the overall output is given by,

$$Y(s) = [H1(s) + H2(s)]X(s). \tag{1}$$

From the topology of the amplifier, we can deduce $H1(s)$ and $H2(s)$ approximately as follows:

$$H1(s) \cong \frac{a_1(0)}{(1+\tau_n s)(1+\tau_o s)}, \tag{2}$$

where, $a_1(0)$ is the DC gain from the input to the output due to the N-folded cascode, τ_n is the time constant at the N-folding node and τ_o is the time-constant at the output node. Also,

$$H2(s) \cong \frac{a_2(0)}{(1+\tau_p s)(1+\tau_o s)}, \tag{3}$$

where, $a_2(0)$ is the DC gain from the input to the output due to the second cascode pair and τ_p is the time constant at the P-folding node.

The *native* zeros of the N and P sub-circuits (i.e., of the type g_m/C_{gd} prior to the addition of any compensation capacitance) are considered to be well-beyond the Unity Gain Bandwidth frequency of the open-loop amplifier (usually a workable assumption).

The overall transfer function is thus given by,

$$H(s) = \frac{a_1(0)(1+\tau_p s) + a_2(0)(1+\tau_n s)}{(1+\tau_n s)(1+\tau_p s)(1+\tau_o s)}. \tag{4}$$

Or, after rearrangement,

$$H(s) = \frac{[a_1(0) + a_2(0)] \times \left[1 + \frac{(a_1(0)\tau_p + a_2(0)\tau_n)}{(a_1(0)+a_2(0))}s\right]}{(1+\tau_n s)(1+\tau_p s)(1+\tau_o s)}, \quad (5)$$

where, we now see the creation of a LHP zero at,

$$w_z = -\frac{(a_1(0) + a_2(0))}{(a_1(0)\tau_p + a_2(0)\tau_n)}. \quad (6)$$

The overall transfer function thus contains a zero and three poles. This new transmission zero resulting from "active feed-forward" can be designed (through proper device sizing) to provide reasonably close pole-zero cancellation of a non-dominant parasitic pole at one of the folding nodes. In addition, it can be combined with a passive (capacitive) feed-forward component to cancel the phase delay due to the second non-dominant pole.

The expressions for the DC gains can be determined quite easily for this rail-to-rail OTA circuit, by noting that, looking from the output node towards either differential pair of the OTA in Fig. 1, the output impedance is the same (for first order approximation). Thus,

$$a_1(0) \approx g_{m1,2}R_{\text{out}} \text{ and } a_2(0) \approx g_{m11,12}R_{\text{out}} \quad (7)$$

with,

$$R_{\text{out}} \approx \frac{\begin{array}{c}[(r_{o11,12}IIr_{o9,10}) \times r_{o7,8} \times g_{m7,8})] \\ \times[(r_{o3,4}IIr_{o1,2}) \times r_{o5,6} \times g_{m5,6}]\end{array}}{\begin{array}{c}[(r_{o11,12}IIr_{o9,10}) \times r_{o7,8} \times g_{m7,8})] \\ +[(r_{o3,4}IIr_{o1,2}) \times r_{o5,6} \times g_{m5,6}]\end{array}}. \quad (8)$$

Also, the approximate time-constants at the folding nodes and the output node can be easily determined. At the N-folding node the total capacitance is given by,

$$\begin{aligned} C_{N\text{-}fold} &= C_{dg3,4} + C_{gs5,6} + C_{db3,4} + C_{sb5,6} \\ &\quad + C_{dg1,2} + C_{db1,2}. \end{aligned} \quad (9)$$

So that the time constant τ_n is given by,

$$\tau_n = C_{N\text{-}fold}\left(\frac{1}{g_{m5,6}}IIr_{o3,4}IIr_{o1,2}\right). \quad (10)$$

Next at the P-folding node we have,

$$\begin{aligned} C_{P\text{-}fold} &= C_{dg9,10} + C_{gs7,8} + C_{db9,10} + C_{sb7,8} \\ &\quad + C_{dg11,12} + C_{db11,12}. \end{aligned} \quad (11)$$

So that the time constant τ_p is given by,

$$\tau_p = C_{P\text{-}fold}\left(\frac{1}{g_{m7,8}}IIr_{o9,10}IIr_{o11,12}\right), \quad (12)$$

and, the time constant τ_o at the output node is given by,

$$\tau_o = (C_L + C_{\text{out}})R_{\text{out}}, \quad (13)$$

where,

$$C_{\text{out}} = C_{dg7,8} + C_{db5,6} + C_{dg5,6} + C_{db7,8}. \quad (14)$$

Clearly, the pole due to τ_o, $w_{po} = -1/\tau_o$ is the dominant pole. On the other hand, $w_{pn} = -1/\tau_n$ due to τ_n and $w_{pp} = -1/\tau_p$ due to τ_p are the non-dominant parasitic poles targeted for pole-zero cancellation through a mixed active and passive feed-forward compensation technique. Small capacitive feed-forward is introduced from the N-folding (or the P-Folding) node, i.e., the source of the PMOS (or the NMOS) cascode device, to the output node (as shown in Fig. 1). This results in some modification of the non-dominant pole at the N-folding (or the P-Folding) node and a very slight modification of the pole at the output. At high frequencies, the N-folding (or the P-folding) node is shorted to the output via the feed-forward capacitive path and the N-folded (or the P-Folded) cascode now only has cascoded load (without cascoded input). The overall open loop amplifier now has only two poles, with the pole at the P-folding (or the N-Folding) node being the only non-dominant pole. The LHP zero W_Z can now be utilized for the approximate cancellation of this non-dominant pole, so that the overall compensated amplifier has almost an ideal single pole frequency response. It is to be noted here that impedance mismatch at differential nodes can result in added pole-zero doublets, their net contribution to phase margin, though, is usually minimal [11]. In addition, inaccurate pole-zero cancellation can result in slow settling which may sometimes have to be rectified (depending on application) with additional pole-zero compression circuitry [12]. Figure 2 shows the low-voltage bias circuit with start-up mechanism [9] used for the amplifier, while, Fig. 3 shows the common-mode feedback circuit [8].

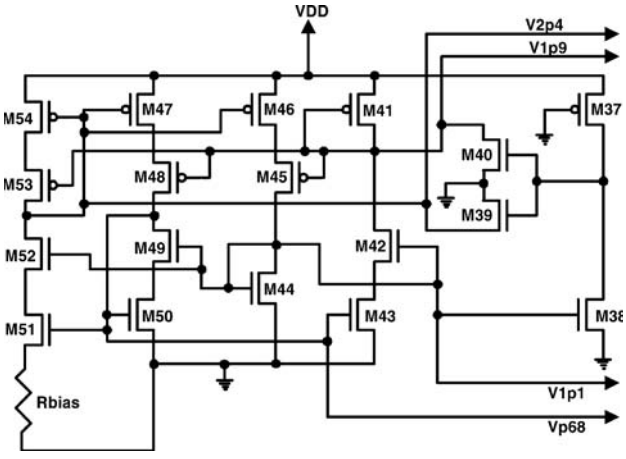

Fig. 2 Low-voltage bias circuit with start-up devices

3 Circuit simulation results

Extensive SPICE circuit-level simulations (using Tanner T-SPICE v.10.0) were conducted to verify the proposed mixed active and passive compensation scheme, using the Agilent (HP) 0.5 μm 3 M1P CMOS process technology parameters. Operation of the complete compensated amplifier in conjunction with the low-voltage bias circuit and the common-mode feedback circuit was verified through the simulations. A 3.3 V power supply (VDD) and a common-mode voltage (VCM) of

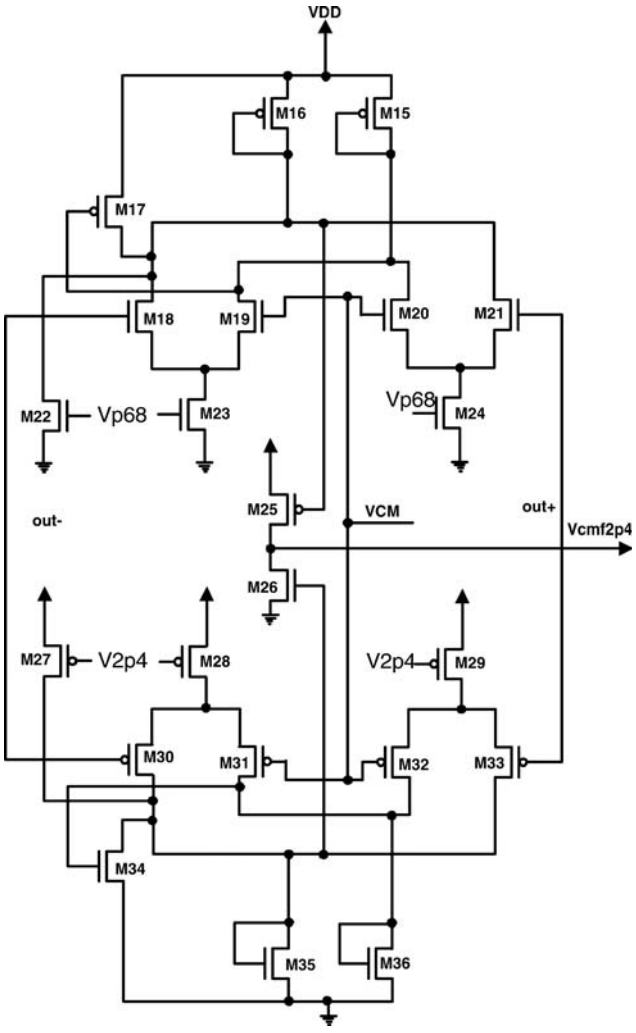

Fig. 3 "Fast sensing" common-mode feed-back circuit

1.6 V was used for the DC-bias condition. The VCM was chosen and held at almost the center (middle) of the supply rails so as to allow sufficient voltage-swing headroom for near rail-to-rail AC amplifier output. A load capacitance of 1 pF was assumed at the amplifier output (standard for many switched capacitor applications) in addition to the total internal transistor parasitic capacitances [C_{out} in (14)] due to transistors M5, M6, M7 and M8 connected at the output nodes. The total output load driven by the amplifier was thus estimated to be around 1.17 pF. In the common-mode feedback circuit [8] drain voltages of the 1.6 V VCM driven differential pair devices was used for "sense amplification" of the common-mode feedback signal using a combination of current source (current sink) and pull-down (pull-up) devices (as shown in Fig. 3).

The frequency response of a rail-to-rail CMOS OTA ("merged P-N CMOS folded cascade") *without* the application of the proposed compensation scheme was simulated and compared to two cases of the feed-forward compensated amplifier *with* the proposed mixed active and passive compensation technique. Case I consists of a topology with passive feed-forward from the P-folding node to the output, while, case II consists of a topology with passive feed-forward from the N-folding node to the output. A feed-forward capacitance of 0.4 pF was used for both case I and case II for the performance comparson. This value of the feed-forward capacitance was chosen based on the tradeoff between settling time and phase margin (in the bode diagram), and also, a compromise component value that can be reasonably conveniently *harvested* from the MOSFET parasitics without the use of large on-chip layout area (device *footprint*). Figure 4 shows the rail-to-rail amplifier's frequency response (*without compensation*) indicating a phase margin of 44° at the gain cross-over point. A phase margin in the range 50° to 60°, obtained at the expense of a very large load capacitance (10 pF), has been reported in [14] for an existing rail-to-rail amplifier using miller compensation and cascoded miller compensation techniques. Next, for the case I of our proposed technique depicted in Fig. 5 simulation results, the phase lag at unity gain for feed-forward from P-fold to output was around −124°, allowing a phase margin of around 55° (using only the total 1.17 pF load capacitance). Next, Fig. 6 displays the result for the case II where the phase lag at gain crossover is found to be around −98° leaving a phase margin of around 82° (@ the 1.17 pF total load) which is almost the response of a single-pole amplifier. This is a considerable improvement compared to all the previous cases. In addition, it can be seen from a comparison of the above bode diagrams, as well as the results in [13, 14], that using the topology in case II of our proposed compensation technique, unity gain bandwidth of around 320 MHz can be achieved using the low-cost CMOS process technology. The total power dissipation of our simulated feed-forward compensated amplifier was around 7.5 mW (which includes 0.5 mW dissipation by the bias circuit and a significantly large 5 mW dissipation by the "fast sensing" common-mode feedback circuit). Next, Fig. 7 shows that a 0.1% settling time of around 8.5 ns has been achieved by the amplifier corresponding to the 82° phase margin, when the amplifier is configured in a unity gain feedback configuration, and, a step input of 800 mV is applied. Also, in an open-loop configuration, a peak-to-peak output swing of around 2.83 V was achieved for the same feed-forward compensated amplifier topology (a near rail-to-rail swing for a 3.3 V supply as shown in Fig. 8) along with a total harmonic distortion (THD) of around –58 dB for a pure sinusoidal input of 26 mV(peak-to-peak) @ 5 MHz, thus delivering a voltage gain of over 60 dB. With small load and feed-forward capacitances the slew-rate of the amplifier was reasonably high at around 250 V/μS. The proposed new topology thus provides a single-stage compensated fully differential amplifier for signal processing which is competitive to other recent and contemporary single stage compensated CMOS folded cascade designs [6–8] and other existing rail-to-rail CMOS amplifier designs [13, 14].

Monte-Carlo Analysis: Additional insight regarding the process tolerances of the proposed compensation technique was

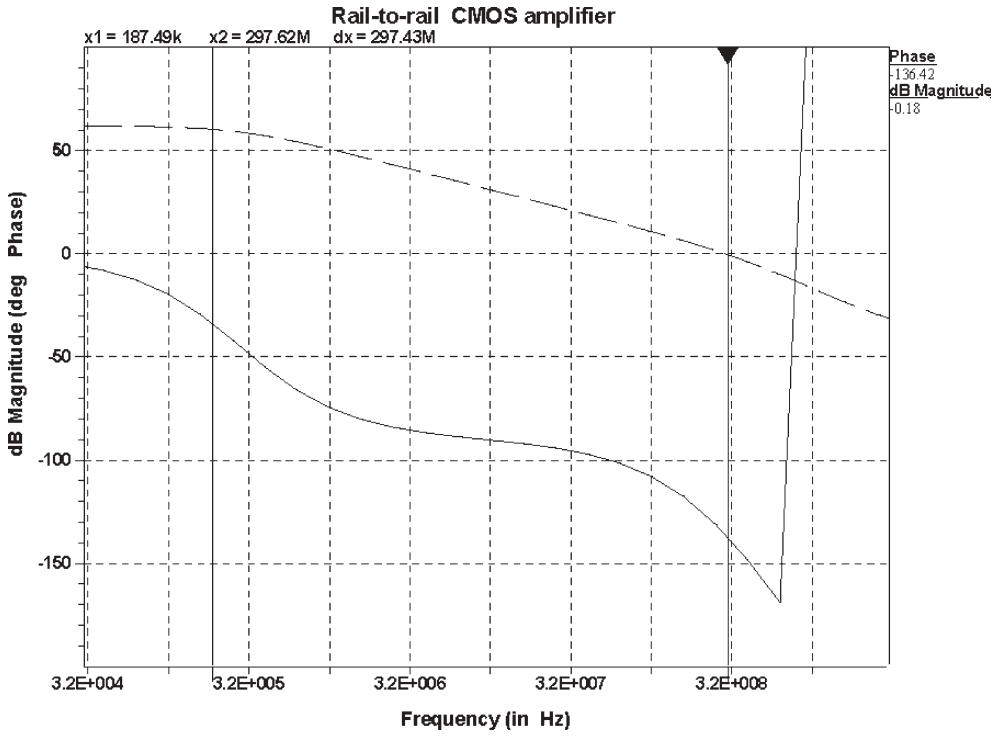

Fig. 4 Frequency response of the rail-to-rail CMOS OTA ("merged P-N CMOS folded cascade") *without* the application of the proposed compensation scheme

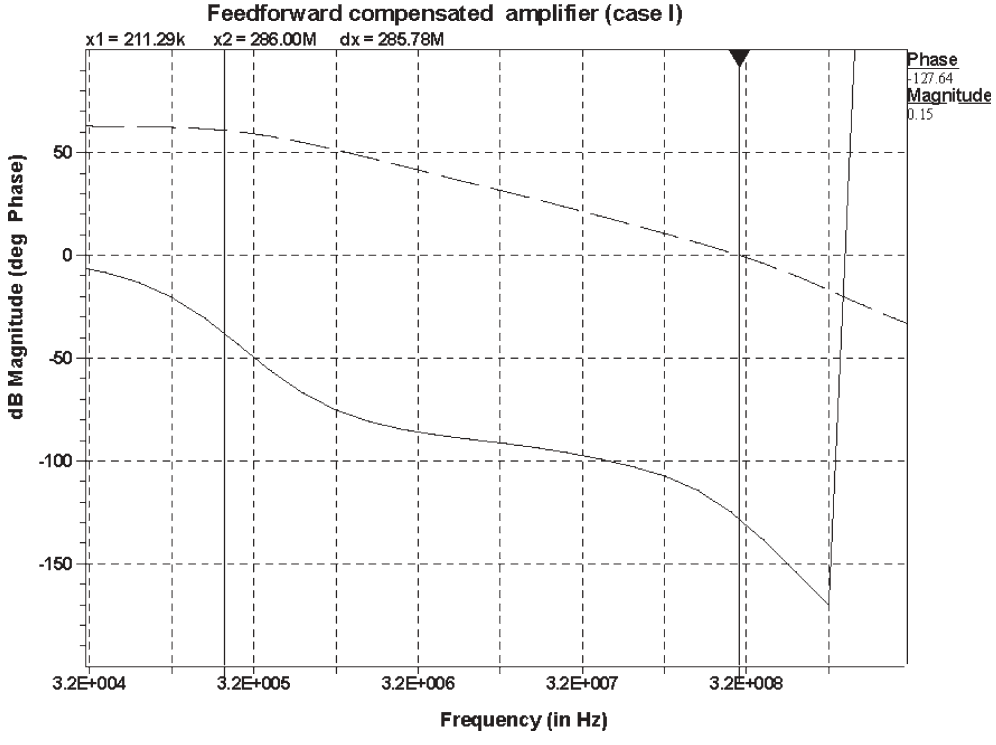

Fig. 5 Frequency response of the rail-to-rail CMOS OTA ("merged P-N CMOS folded cascade") *with* the application of mixed active and passive (capacitive across *P-fold* and output) feed-forward compensation

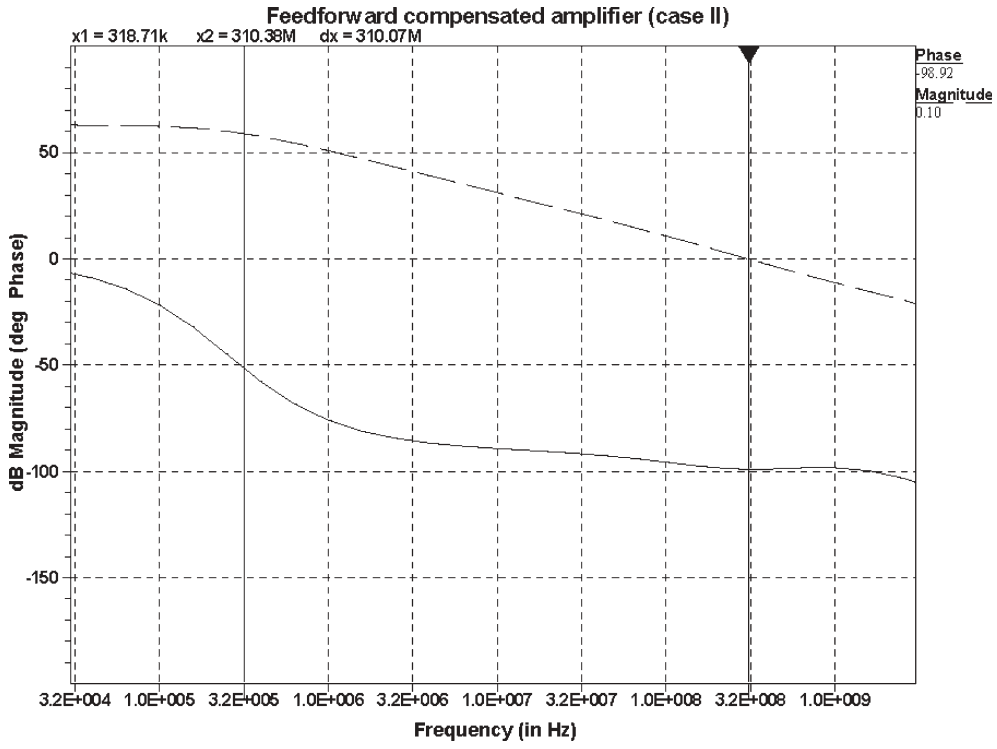

Fig. 6 Frequency response of the rail-to-rail CMOS OTA ("merged P-N CMOS folded cascade") *with* the application of mixed active and passive (capacitive across *N-fold* and output) feed-forward compensation

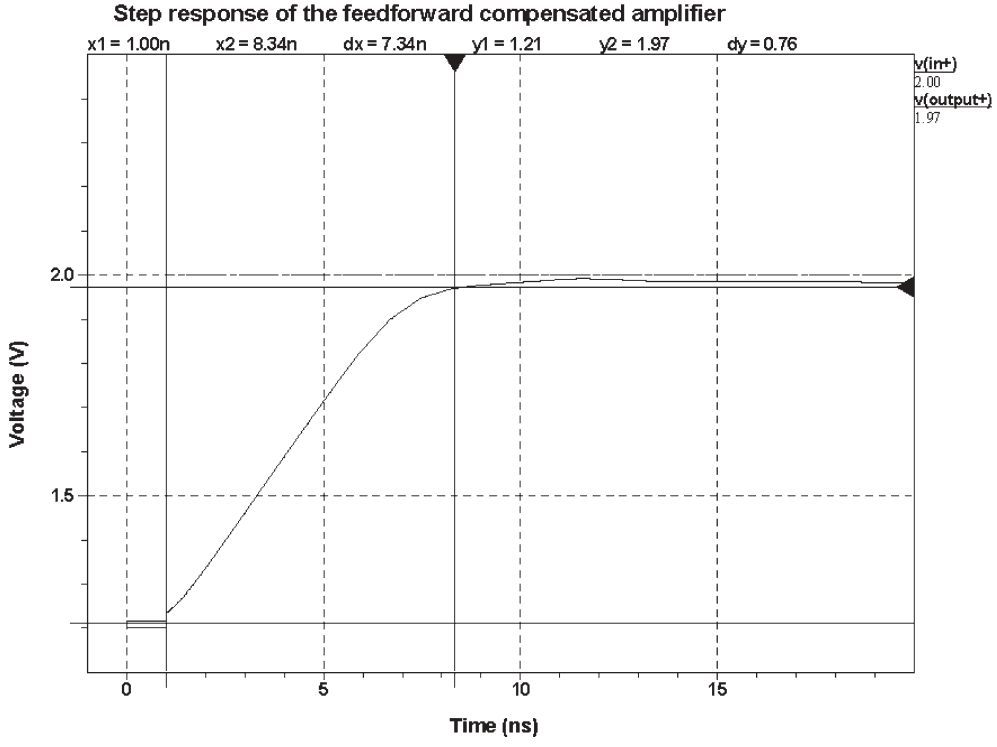

Fig. 7 Step response of the rail-to-rail CMOS OTA ("merged P-N CMOS folded cascade") using mixed active and passive (capacitive across N-fold and output) feed-forward compensation

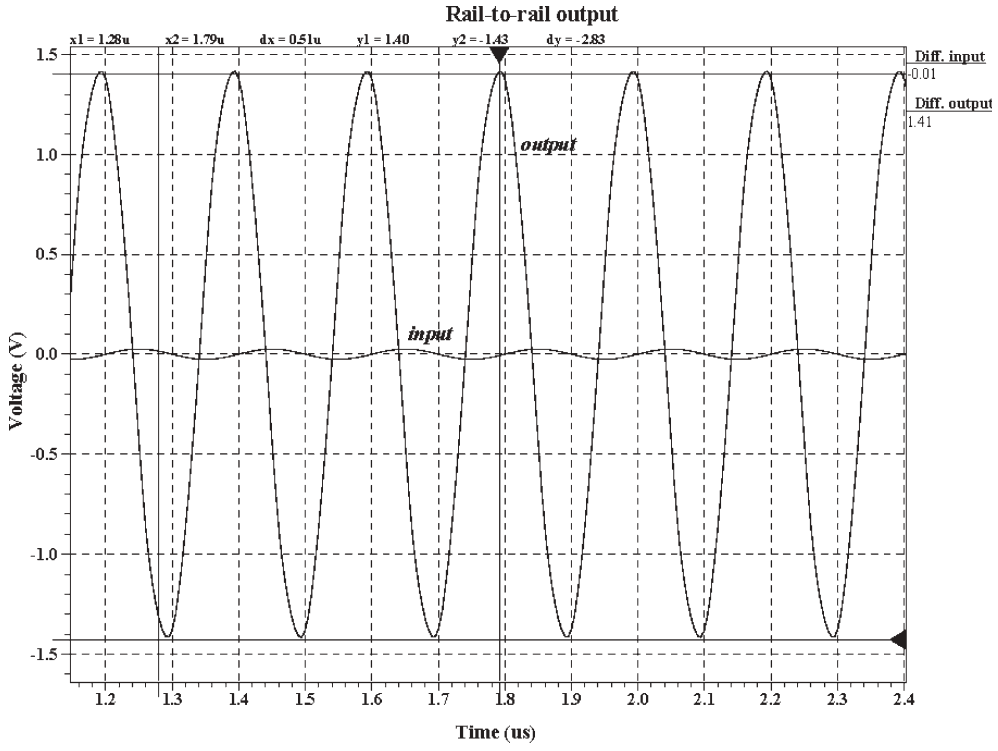

Fig. 8 Transient response of the rail-to-rail CMOS OTA ("merged P-N CMOS folded cascade") indicating near rail-to-rail swing

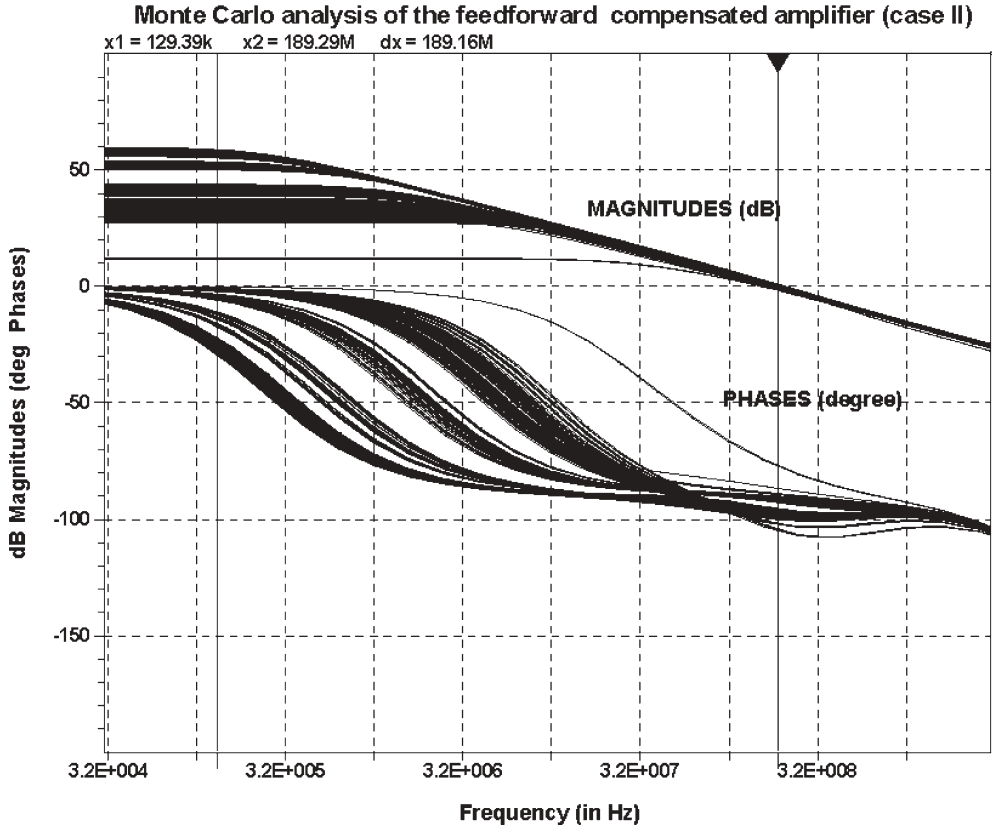

Fig. 9 Spectral Monte-Carlo analysis depicting the effect of process related threshold voltage variation on the frequency response of the rail-to-rail CMOS OTA ("merged P-N CMOS folded cascade") *with* mixed active and passive (capacitive across *N-fold* and output) feed-forward compensation

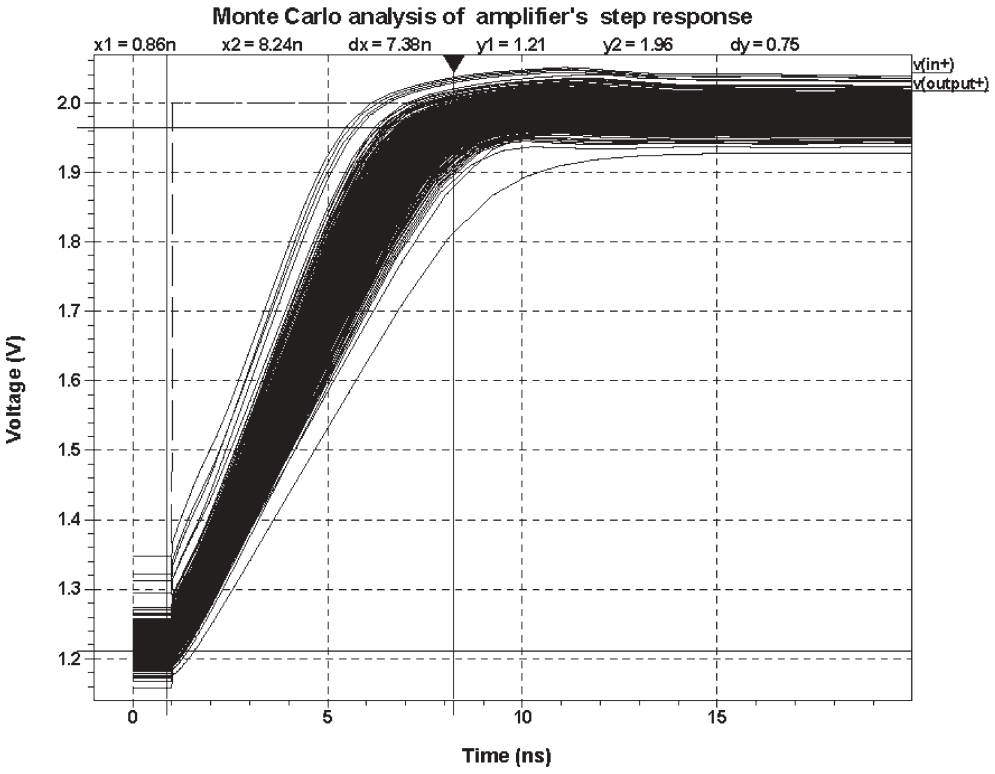

Fig. 10 Monte-Carlo analysis indicating the effect of process related threshold voltage variation on the settling response of the rail-to-rail CMOS OTA ("merged P-N CMOS folded cascade") *with* mixed active and passive (capacitive across *N-fold* and output) feed-forward compensation

gained through a series of Monte-Carlo simulations. In order to estimate the effect of process related threshold voltage variation of the MOSFET devices in the feed-forward compensated amplifier, Monte-Carlo analysis using a Gaussian distribution function taking into account about 20% variation of the threshold voltages was performed. Figure 9 shows the result for 300 iterations of the frequency response analysis (using the case II topology), which indicates a variation of the phase margin essentially within a *band* between the best case of 94° and the worst case of 70°. Next, Fig. 10 depicts the temporal Monte-Carlo analysis of the compensated amplifier's step response which indicates a variation of the settling accuracy by about 12.5%. This is mostly due to the variation of the amplifier's DC-gain with threshold voltage changes. Since the settling-time indicates the accuracy of the pole-zero cancellation [15], Fig. 10 also indicates that there is approximately 15% variation of the pole-zero cancellation error using this compensation scheme with around 20% process related variation in the threshold voltages. The compensation scheme can thus be considered to be reasonably robust to process parameter variations.

4 Conclusion

A novel compensation technique for the rail-to-rail CMOS differential OTA topology, along with extensive SPICE circuit simulation results has been presented. The proposed amplifier provides mixed active and passive feed-forward compensation resulting in pole-zero cancellation of non-dominant parasitic poles of the topology. A phase-margin of around 82° is achieved with the use of only small compensation capacitance value (@1.17 pF load) and without sacrificing the amplifier's unity-gain bandwidth. In addition, Monte Carlo analysis predicting spectral and temporal performance tolerances with 20% process related threshold voltage variations has also been provided. The compensation technique is suitable for OTAs used in mixed-signal switched capacitor applications.

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