The Recycling Folded Cascode: A General Enhancement of the Folded Cascode Amplifier

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***Abstract*—A recycling amplifier architecture based on the folded cascode transconductance amplifier is described. The proposed amplifier delivers an appreciably enhanced performance over that of the conventional folded. This is achieved by using previously idle devices in the signal path, which results in an enhanced transconductance, gain, and slew rate. Moreover, the input referred noise and offset analyses are included to demonstrate that the proposed modifications have no adverse effects on these design metrics. Transistor-level simulations and experimental results in TSMC 0.18 μm CMOS process confirm the theoretical results. When compared to the conventional folded cascode, and for the same area and power budgets, the proposed amplifier has almost twice the bandwidth (134.2 MHz versus 70.7 MHz) and better than twice the slew rate (94.1 V/μs versus 42.1 V/μs) while driving the same 5.6 pF load. Also a gain enhancement of 7.6 dB is observed.**

***Index Terms*—Amplifiers, CMOS analog integrated circuits, fast operational amplifiers, low-power low-voltage integrated circuits, operational amplifiers, operational transconductance amplifiers.**

I. Introduction

THE advancement of CMOS technologies paved the road for a growing market of mobile and portable electronic devices. This growth is driven by the continual integration of complex analog and digital building blocks on a single chip, making silicon area and power consumption the two most valued aspects of a design. The operational transconductance amplifier (OTA) is still a vital analog building block and for many applications is the largest and most power consuming.

Recently, one of the most commonly used architectures, whether as a single-stage or first stage in multi-stage amplifiers, had been the folded cascode (FC) amplifier for its high gain and reasonably large signal swing in the present and future low voltage CMOS processes. Moreover, the PMOS input FC has become the prime choice over its NMOS counterpart for its higher non-dominant poles, lower flicker noise, and input common mode level. The latter allows input switching using a single NMOS transistor in switched-capacitor (SC) applications [1], [2].

Previous work to enhance the performance of the FC used multi-path schemes [3] and [4]. Another multi-path scheme [5] was applied to the Three-Current-Mirror OTA to enhance the output impedance and slew rate, and another in [6] to emulate a class AB operation. However, they were not suitable for high-speed applications as the transfer function of the OTA had numerous low frequency pole-zero pairs. Nonetheless, [3]–[6] form the basis of the proposed modifications to the FC amplifier presented in Section II. In Section III, the effects of these modifications on the major design metrics of the proposed FC amplifier are presented, whereas Sections IV and V discuss the implementation, and experimental/simulations results respectively. Finally, the conclusions are presented in Section VI.

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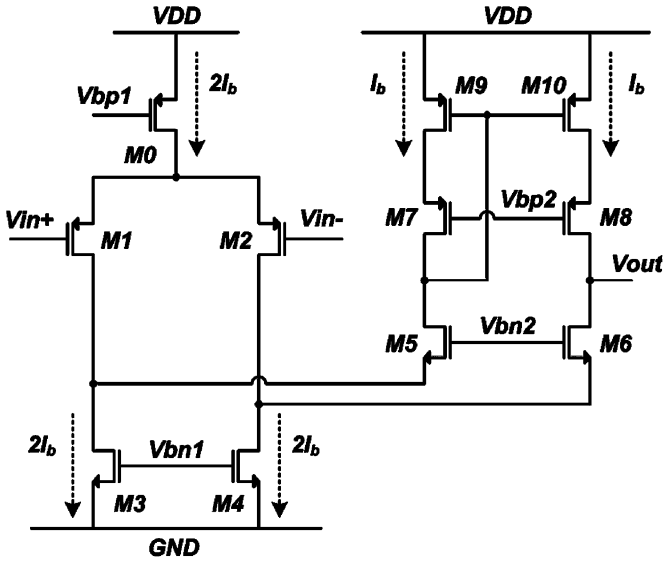

Fig. 1. The conventional folded cascode amplifier.

II. Proposed FC Amplifier

The conventional FC is shown in Fig. 1. Note how transistors $M3$ and $M4$ conduct the most current, and in many designs have the largest transconductance. However, their role is only limited to providing a folding node for the small signal current generated by the input drivers ($M1$ and $M2$).

To address this inefficiency, a modified FC is presented in Fig. 2.The proposed modifications are intended to use $M3$ and $M4$ as driving transistors [7]. First, the input drivers, $M1$ and $M2$ (Fig. 1), are split in half to produce transistors $M1a$, $M1b$, $M2a$, and $M2b$, which now conduct fixed and equal currents of $I_b/2$ (Fig. 2). Next, $M3$ and $M4$ (Fig. 1) are split to form the current mirrors $M3a$:$M3b$, and $M4a$:$M4b$ with a ratio of $K:1$ (Fig. 2). The cross-over connections of these current mirrors ensure the small signal currents added at the sources of $M5$ and $M6$ are in phase. Finally, $M11$ and $M12$ are sized similar to $M5$ and $M6$, and their addition helps maintain the drain potentials of $M3a$:$M3b$ and $M4a$:$M4b$ equal for improved matching.

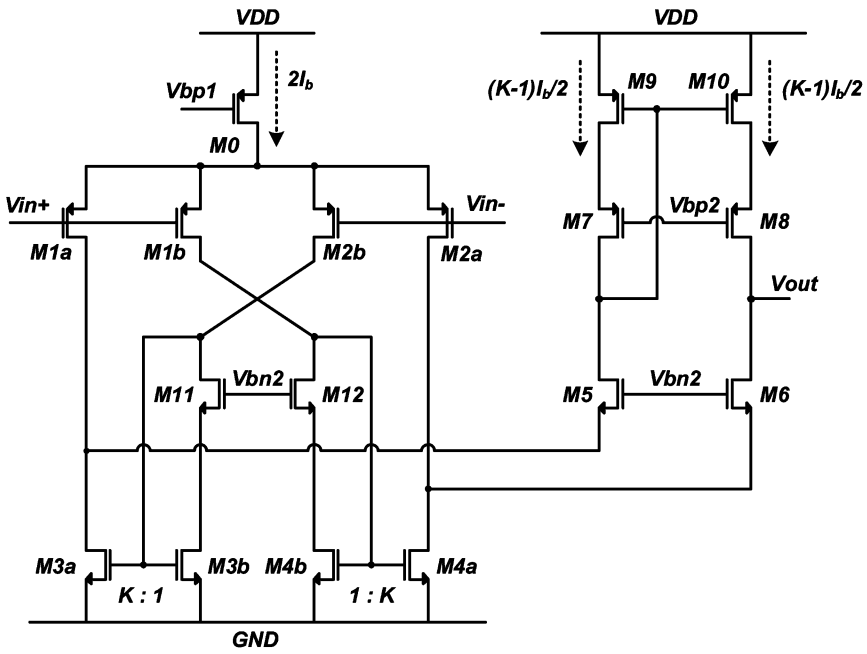

Fig. 2. The recycling folded cascode (RFC) amplifier.

We will refer to the modified FC as the recycling folded cascode (RFC), as we are reusing, or recycling, existing devices and currents to perform an additional task.

III. RFC Characteristics

The modifications presented in Section II provide the RFC with enhanced features over that of the FC. In order to present these enhancements quantitatively, all devices are assumed to operate in the saturation region following the simplified square-law drain current model given by

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{GS} - V_T\right)^2. \tag{1}$$

Here the symbols have their usual meanings of carrier mobility, gate oxide per unit area, device aspect ratio, gate-source voltage, and threshold voltage respectively. Also, the current gain K shown in Fig. 2 is selected to equal 3. This maintains the same power consumption for both the FC and RFC shown in Figs. 1 and 2. Note, however, that the current through $M5 - M10$ is now a function of K; for $K \neq 3$, $M5 - M10$ need to be scaled accordingly to maintain the same inversion level – equal power and area as the FC is only achieved at $K = 3$.

The analyses presented in Sections III-A–G are valid for both the single-ended and differential implementations of the amplifiers. Nonetheless, wherever appropriate further insight into the fully differential implementation will be provided.

A. Small Signal Transconductance

We first examine the amplifier's transconductance, Gm, by finding the short-circuit current at the output with respect to the input. The results for RFC and FC follow in (2) and (3).

$$Gm_{\mathrm{RFC}} = gm_{1a}\left(1 + K\right) \tag{2}$$

$$Gm_{\mathrm{FC}} = gm_1. \tag{3}$$

By taking into account that $M1$ is twice the size of $M1a$ and conducts twice the amount of current (i.e., $gm_1 = 2gm_{1a}$), and substituting for the value of K, the transconductance of the RFC is demonstrated to be twice that of the FC for the same power consumption. This shows that the RFC has twice the gain-bandwidth (GBW) as that of the FC for the same power, and consequently twice the speed.

B. Low Frequency Gain

The low frequency gain of OTAs is frequently expressed as the product of the small signal transconductance, Gm, and the low frequency output impedance, Ro. It was demonstrated that $Gm_{\mathrm{RFC}} = 2Gm_{\mathrm{FC}}$, which results in a 6 dB gain enhancement for the same output impedance. However, Ro_{RFC} is also enhanced over Ro_{FC}. The expressions for Ro_{RFC} and Ro_{FC} are represented by (4) and (5), respectively.

$$Ro_{\mathrm{RFC}} \cong gm_6 r_{ds6}\left(r_{ds2a} \,||\, r_{ds4a}\right)||gm_8 r_{ds8} r_{ds10} \tag{4}$$

$$Ro_{\mathrm{FC}} \cong gm_6\, r_{ds6}\left(r_{ds2} \,||\, r_{ds4}\right)||gm_8 r_{ds8} r_{ds10}\,. \tag{5}$$

The gain enhancement seen in Ro_{RFC} is attributed to the increased r_{ds} of $M2a$ and $M4a$, as they conduct less current compared to their counterparts $M2$ and $M4$ of the FC. Therefore, an overall low frequency gain enhancement of 8–10 dB can be seen in the RFC compared to the FC.

This added gain has two fundamental benefits. First, static settling errors are reduced because of the increased gain. Second, the power supply rejection ratio (PSRR) performance of the RFC is improved over its FC counterpart. PSRR is defined as the injected supply noise gain with respect to the input signal gain. Both the FC and RFC have similar noise injections gains from either supply, but the loop gain of the RFC is higher and hence its PSRR performance is better. Moreover, the extended GBW of the RFC extends the improved PSRR performance to higher frequencies than the FC.

C. Slew Rate

The slew rate is a critical design aspect as it directly adds to the settling time of an amplifier. Assuming a capacitive output load C_L and a large signal seen at the inputs of the RFC, the slew rate can be derived as follows.

Suppose Vin+ goes high, it follows that $M1a$ and $M1b$ turn off, which forces $M4b$ and $M4a$ to turn off. Consequently, the drain voltage of $M4a$ rises and $M6$ is turned off whereas $M2a$ is driven into deep triode. This directs the tail current, $2I_B$, into $M2b$ and in turn is mirrored by a factor K ($M3b$:$M3a$) into $M5$, and again by a factor of 1 ($M9$:$M10$) into C_L. If we ignore any parasitic capacitance at the drain of $M0$ for simplicity, and follow the same derivation steps but assuming Vin+ goes low, the result is a symmetric slew rate expressed by (6). Similar derivations for the FC result in (7).

$$\mathrm{SR_{RFC}} = \frac{2KI_B}{C_L} \tag{6}$$

$$\mathrm{SR_{FC}} = \frac{2I_B}{C_L}. \tag{7}$$

By examining (6) and (7), and substituting for the value of K, the slew rate of the RFC is enhanced 3 times over the FC for the same power consumption. This, however, is the theoretical limit. In an actual design the devices assumed to fully turn off still conduct some current, and hence reduce the amount reaching the output. Moreover, the accuracy of the current mirrors is degraded for large transients. Nonetheless, with proper sizing and biasing of devices, a slew rate enhancement greater than 2 can be realized for $K = 3$.

The symmetry of the slew rate as described previously is made possible in the single-ended implementation by the unity current mirror $M9$:$M10$. In fully-differential implementations, however, $M9$ and $M10$ are controlled by a common-mode feedback (CMFB) circuit, and following the foregoing analysis for this scenario it would seem that the differential outputs are asymmetrically charged/discharged. This is indeed the case, but the asymmetry is quickly converted into a common mode error, which forces the CMFB circuit to balance the differential output charge/discharge rates leading to a symmetric slew rate as described by (6) for the same single-ended load [7]. Hence, the CMFB loop gain and bandwidth need to be carefully considered when using the RFC in a fully differential implementation.

D. Phase Margin

The phase margin is often viewed as a good indicator to the transient response of an amplifier, and is determined by the poles and zeros of the amplifier transfer function. In comparison with the FC, the RFC shares a dominant pole ω_{p1} determined by the output impedance and capacitive load and a non-dominant pole ω_{p2} determined by the parasitics at the source of $M5/M6$. In addition, the RFC has a pole-zero pair, ω_{p3} and ω_{z1} ($= (K+1)\omega_{p3}$), associated with the current mirrors $M3a$:$M3b$ and $M4a$:$M4$. However, this pole-zero pair is associated with NMOS devices, which puts it at a high frequency.

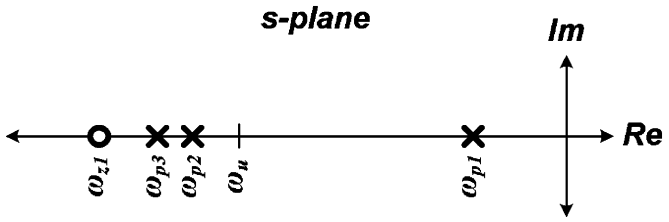

Fig. 3. Pole-zero locations of the RFC in the s-domain.

This is depicted in Fig. 3 where it is assumed that all non-dominant poles and zeros are beyond the unity gain frequency, ω_u, for good phase margin and stability. Also, the locations of ω_{p2} and ω_{p3} may be interchanged depending on design.

The choice of K plays a significant role in determining the phase margin of the RFC, so the selection of K will be limited by the amplifier application; for high speed applications K can be chosen such that $\omega_{p3} > 3\omega_u$, which places an upper boundary on K as described by

$$\omega_{p3} > 3\omega_u \Rightarrow K < \sqrt{\frac{gm_{3b}C_L}{3gm_{1a}Cgs_{3b}}} - 1. \tag{8}$$

A reasonable range for K values to minimize phase margin degradation is 2–4.

E. Noise

In many applications, such as audio amplifiers, continuous time filters and data converters, noise can be the limiting factor in a design. The maximum noise current power seen at the output of a MOSFET is given by

$$\overline{i_o^2} = \left[4k_{\mathbf{B}}T\gamma gm + \frac{K_F I_D}{C_{ox}L^2 f}\right] \cdot \Delta f \tag{9}$$

where the first and second terms represent the thermal and flicker noise contributions respectively. Equation (9) is a simplified form of other complex models [8] and [9] to aid derivations.

For comparison purposes the thermal and flicker noise components are examined individually to reduce clutter. Following the procedure outlined in [10], the input referred thermal noise of RFC and FC are expressed in (10) and (11).

$$\overline{v_{iT,RFC}^2} = \frac{8k_BT\gamma}{gm_{1a}(1+K)} \cdot \left[\frac{(1+K^2)}{(1+K)} + \frac{gm_{3a}}{gm_{1a}} + \frac{1}{(1+K)}\frac{gm_9}{gm_{1a}}\right] \cdot \Delta f \tag{10}$$

$$\overline{v_{iT,FC}^2} = \frac{8k_BT\gamma}{gm_1}\left[1 + \frac{gm_3}{gm_1} + \frac{gm_9}{gm_1}\right] \cdot \Delta f. \tag{11}$$

By substituting for gm_{1a} in terms of gm_1, gm_{3a} in terms of gm_3, and the value of K, we transform (10) to (12):

$$\overline{v_{iT,RFC}^2} = \frac{8k_BT\gamma}{gm_1}\left[\frac{5}{4} + \frac{3}{4}\frac{gm_3}{gm_1} + \frac{1}{4}\frac{gm_9}{gm_1}\right] \cdot \Delta f. \tag{12}$$

The flicker noise expressions of the RFC and the FC are given by (13) and (14).

$$\overline{v_{\text{if,RFC}}^2} = \frac{K_{\text{FP}}}{\mu_P C_{ox}^2 W_{1a} L_{1a} (1+K) f} \cdot \left[\frac{(1+K^2)}{(1+K)} + K \frac{K_{\text{FN}}}{K_{\text{FP}}} \left(\frac{L_{1a}}{L_{3a}} \right)^2 + \frac{(K-1)}{(1+K)} \left(\frac{L_{1a}}{L_9} \right)^2 \right] \cdot \Delta f \tag{13}$$

$$\overline{v_{\text{if,FC}}^2} = \frac{K_{\text{FP}}}{\mu_P C_{ox}^2 W_1 L_1 f} \cdot \left[1 + 2 \frac{K_{\text{FN}}}{K_{\text{FP}}} \left(\frac{L_1}{L_3} \right)^2 + \left(\frac{L_1}{L_9} \right)^2 \right] \cdot \Delta f. \tag{14}$$

The modifications made to the FC to result in the RFC did not alter the channel lengths of the devices, only the widths. Therefore, by substituting for W_{1a} in terms of W_1 and for the value of K, we transform (13) to (15).

$$\overline{v_{\text{if,RFC}}^2} = \frac{K_{\text{FP}}}{\mu_P C_{ox}^2 W_1 L_1 f} \cdot \left[\frac{5}{4} + \frac{3}{2} \frac{K_{\text{FN}}}{K_{\text{FP}}} \left(\frac{L_1}{L_3} \right)^2 + \frac{1}{4} \left(\frac{L_1}{L_9} \right)^2 \right] \cdot \Delta f. \tag{15}$$

A first look at (11) and (12), and (14) and (15), is inconclusive as to which has lesser noise. However, since two terms in (12) and (15) are smaller than their counterparts in (11) and (14), it is likely the RFC has a lesser or equivalent noise to that of the FC.

F. Input Offset

Manufacturing process variations across the chip lead to mismatch in devices, which are otherwise identical by design. A mismatch model [11] based on the study of equal area rectangular devices, states that the variance of a parameter ΔP can be expressed as

$$\sigma^2 (\Delta P) = \frac{A_P^2}{WL + S_P^2 D_x} \tag{16}$$

where A_P is the area proportionality constant for parameter P, S_P is the variation of P with spacing, and D_x is the distance between two devices along x. Since critical devices, such as the input pair or current mirrors, are interdigitated or cross-coupled, D_x approaches zero, and the second term of (16) can be neglected. Using (1), the drain-current variance due to process variation can be expressed as

$$\sigma^2 (I_D) = 4 I_D^2 \frac{\sigma^2 (V_T)}{(V_{GS} - V_T)} + I_D^2 \frac{\sigma^2 (\beta)}{\beta^2} \tag{17}$$

assuming $\sigma^2(V_T)$ and $\sigma^2(\beta)$ are uncorrelated. Here β represents $\mu C_{ox} W/L$. Equation (17) is very useful, because from a circuit analysis stand point, the drain-current variance can be treated as a small signal that can be referred to the gate of the MOS device through its transconductance, gm. The result is

$$\sigma^2 (V_{GS}) = \sigma^2 (V_T) + \frac{I_D^2}{gm^2} \frac{\sigma^2 (\beta)}{\beta^2} \tag{18}$$

and since in analog design gm/I_D is generally maximized, the effect of the second term of (18) is diminished. Therefore

$$\sigma^2 (V_{GS}) \cong \sigma^2 (V_T) = \frac{A_{V_T}^2}{WL}. \tag{19}$$

Here A_{VT} is the area proportionality constant for the threshold voltage, V_T, which is provided by process characterization.

Using (19), the input offset variance can be expressed as the sum of all device drain-current variances seen at the output, and then referred to the input using the amplifier's Gm. The results for RFC and FC are given in (20) and (21).

$$\sigma^2 (V_{OS,RFC}) = 2 \frac{A_{V_{TP}}^2}{W_{1a} L_{1a} (1+K)} \cdot \left[\frac{(1+K^2)}{(1+K)} + 3 \frac{\mu_N}{\mu_P} \frac{A_{V_{TN}}^2}{A_{V_{TP}}^2} \left(\frac{L_{1a}}{L_{3a}} \right)^2 + \frac{2}{(1+K)} \left(\frac{L_{1a}}{L_9} \right)^2 \right] \tag{20}$$

$$\sigma^2 (V_{OS,FC}) = 2 \frac{A_{V_{TP}}^2}{W_1 L_1} \cdot \left[1 + 2 \frac{\mu_N}{\mu_P} \frac{A_{V_{TN}}^2}{A_{V_{TP}}^2} \left(\frac{L_1}{L_3} \right)^2 + \left(\frac{L_1}{L_9} \right)^2 \right]. \tag{21}$$

By substituting for W_{1a} in terms of W_1 and for the value of K, we transform (20) to (22). Again, by examining (21) and (22), it is inconclusive as to which has lesser input offset.

$$\sigma^2 (V_{OS,RFC}) = 2 \frac{A_{V_{TP}}^2}{W_1 L_1} \cdot \left[\frac{5}{4} + \frac{3}{2} \frac{\mu_N}{\mu_P} \frac{A_{V_{TN}}^2}{A_{V_{TP}}^2} \left(\frac{L_1}{L_3} \right)^2 + \frac{1}{4} \left(\frac{L_1}{L_9} \right)^2 \right]. \tag{22}$$

G. Area and Power

Amplifier design is application specific. However, the amplifier's bandwidth, gain and slew rate are arguably the most critical design criteria. The foregoing analysis shows that for the same area and power consumption, the RFC delivers twice the bandwidth, 8–10 dB expected higher gain, and more than twice the slew rate of the FC. Suppose we take the RFC (call it RFC1) and reduce the widths of all devices by half to produce RFC2, where RFC2 now occupies half the area and uses half the current of the RFC1, and hence the FC. It follows that (2), (6), (12), (15) and (22) become (23)–(27), respectively.

$$Gm_{\text{RFC2}} = \frac{gm_{1a} (1+K)}{2} \tag{23}$$

$$\text{SR}_{\text{RFC2}} = \frac{K I_B}{C_L} \tag{24}$$

$$\overline{v_{iT,RFC2}^2} = \frac{8k_BT\gamma}{gm_1}\left[\frac{5}{2} + \frac{3}{2}\frac{gm_3}{gm_1} + \frac{1}{2}\frac{gm_9}{gm_1}\right]\cdot\Delta f \tag{25}$$

$$\overline{v_{\text{if,RFC2}}^2} = \frac{K_{\text{FP}}}{\mu_P C_{ox}^2 W_1 L_1 f} \cdot\left[\frac{5}{2} + 3\frac{K_{\text{FN}}}{K_{\text{FP}}}\left(\frac{L_1}{L_3}\right)^2 + \frac{1}{2}\left(\frac{L_1}{L_9}\right)^2\right]\cdot\Delta f \tag{26}$$

$$\sigma^2\left(V_{OS,RFC2}\right) = 2\frac{A_{V_{TP}}^2}{W_1 L_1}\cdot\left[\frac{5}{2} + 3\frac{\mu_N}{\mu_P}\frac{A_{V_{TN}}^2}{A_{V_{TP}}^2}\left(\frac{L_1}{L_3}\right)^2 + \frac{1}{2}\left(\frac{L_1}{L_9}\right)^2\right]. \tag{27}$$

Examining (23) shows the RFC2 to have the same transconductance as the FC, whereas (24) shows the RFC2 to have a better slew rate than the FC. Equations (25)–(27), however, demonstrate a degradation in noise and input offset compared to RFC1, and hence FC.

IV. Implementation

To validate the theoretical results presented thus far, a FC amplifier was designed as a benchmark following proven analog design practices; a large input pair biased in weak/moderate inversion to maximize bandwidth and minimize noise and offset, and current mirror devices with long channels biased in strong inversion to improve mirroring accuracy and output impedance. The main constraint applied to the design is a power budget of 800 μA. Once the FC design was finalized, RFC1 and RFC2 were derived as outlined in Sections II and III-F. Table I details the transistor sizes used in the implementation of the FC, RFC1 and RFC2.

V. Experimental and Simulation Results

The amplifiers were fabricated with on-chip RC loads in TSMC 0.18 μm CMOS process using core devices and a nominal V_{DD} of 1.8 V. Fig. 4 shows the chip micrograph highlighting the amplifiers FC, RFC1 and RFC2, the on-chip RC load and the biasing circuit. The test setup used to characterize the performance of the amplifiers is given in Fig. 5. A Tektronix AFG 3102 dual signal generator was used to supply the input signal and the output was captured using a Tektronix TDS 5054 oscilloscope.

To preserve the high output impedance of the amplifiers and limit the DC output current drawn, R was set to be 560 kΩ. As for C_1 and C_2 they were set to 2.2 pF and 2.5 pF, respectively (C_2 includes 0.3 pF pad capacitance). Along with 2 pF of the Tektronix P6205 active probe, the overall load is approximately 5.6 pF. The amplifiers are configured such that the output is set at $V_{\text{DD}}/2$ to maximize swing. A summary of the presented results is given in Table II for easy reference including commonly used amplifier FoMs.

The simulated open loop AC response of the amplifiers is given in Fig. 6, where the load included a simple model for the Tektronix P6205 active probe and PCB trace capacitance in addition to R, C_1 and C_2. The GBW of the FC, RFC1 and RFC2 is 73.1 MHz, 139.8 MHz and 73.0 MHz respectively, which indeed demonstrates the enhanced transconductance of the RFC. As for the phase margin, the FC, RFC1 and RFC2 measured 83.6°, 70.6° and 79.8° at their respective GBWs. Comparing the FC with RFC2 as they have the same GBW, RFC2 shows only 3.8° degradation. On the other hand, the phase margin of the FC drops to 77.7° at 139.8 MHz, and hence the RFC1 shows 7.1° of degradation. Nevertheless, neither amplifier is expected to show any ringing in transient performance.

To measure the gain bandwidth of the amplifiers experimentally, a small signal step, 100 mVpp at 10 MHz was applied to the input and the 1% settling time (4.6 time constants) was measured. The small signal step response of the amplifiers is given in Fig. 7. Clearly RFC1 (Ch2) has the wider bandwidth, while FC (Ch1) and RFC2 (Ch3) have virtually the same bandwidth. The 1% settling times for the FC, RFC1 and RFC2 are 20.7 ns, 11.2 ns, and 20.8 ns; taking into account that the feedback factor of the tested amplifier configurations is very close to 0.5, this corresponds to an open loop bandwidth of 70.7 MHz, 134.2 MHz and 70.4 MHz respectively in good agreement with simulated results. Moreover, Fig. 7 shows the peak-to-peak amplitude of the output. Using this information the DC gain of the

TABLE I
Amplifier Device Sizes (μm)

DEVICE	FC	RFC1	RFC2
M0	128/0.5	128/0.5	64/0.5
M1/M2	128/0.36	-	-
M1a/M1b/M2a/M2b	-	64/0.36	32/0.36
M3/M4	32/0.5	-	-
M3a/M4a	-	24/0.5	12/0.5
M3b/M4b	-	8/0.5	4/0.5
M5/M6	16/0.18	16/0.18	8/0.18
M7/M8	64/0.18	64/0.18	32/0.18
M9/M10	64/0.5	64/0.5	32/0.5
M11/M12	-	8/0.18	4/0.18

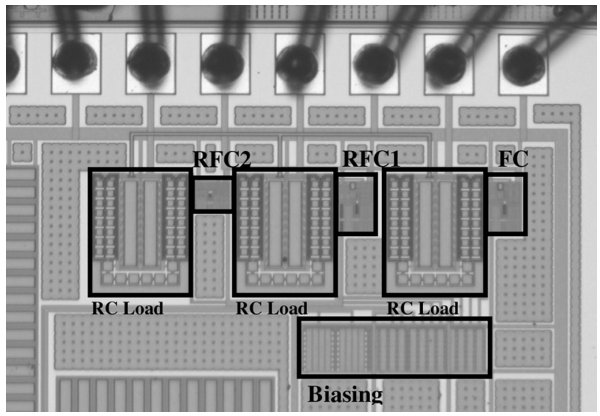

Fig. 4. Enlarged die section showing the FC, RFC1 and RFC2 with their on-chip RC loads and biasing circuit.

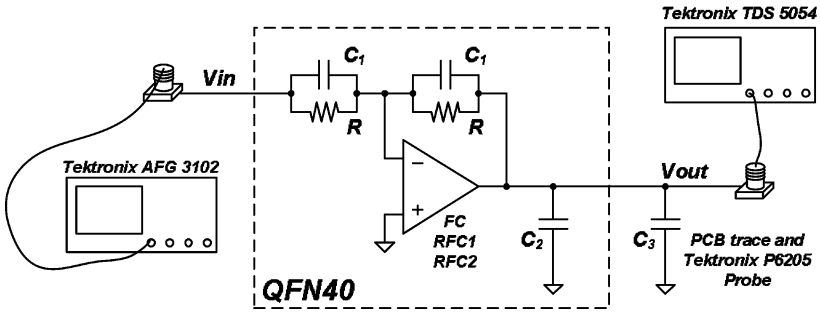

Fig. 5. Amplifier characterization setup used to measure the performance of the amplifiers.

TABLE II
AMPLIFIER CHARACTERIZATION RESULTS

PARAMETER	FC	RFC1	RFC2
Power (Bias current) [µA]	800	800	400
Area [μm^2]	4712.9 (53.8×87.6)	4958.2 (56.6×87.6)	3001.8 (58.4×51.4)
DC Gain [dB]	46.0 (52.6*)	53.6 (60.9*)	54.9 (59.7*)
GBW [MHz]	70.7	134.2	70.4
Open Loop PM [deg]*	83.6	70.6	79.8
Capacitive Load [pF]	5.6	5.6	5.6
Slew Rate (average) [V/µs]	42.1	94.1	48.1
1% Settling Time [ns]	20.7	11.2	20.8
IM3, 1Vpp at 1MHz [dB]	-61.7	-66.1	-61.6
Input Referred Noise* (1Hz-100MHz) [µVrms]	53.2	48.5	69.7
Input Offset* (3σ) [mV]	7.9	7.6	11.1
FoM_1 (MHzpF/mA)	494.9	939.4	492.8
FoM_2 ((V/µs)pF/mA)	294.7	658.7	336.7

* Simulation Results

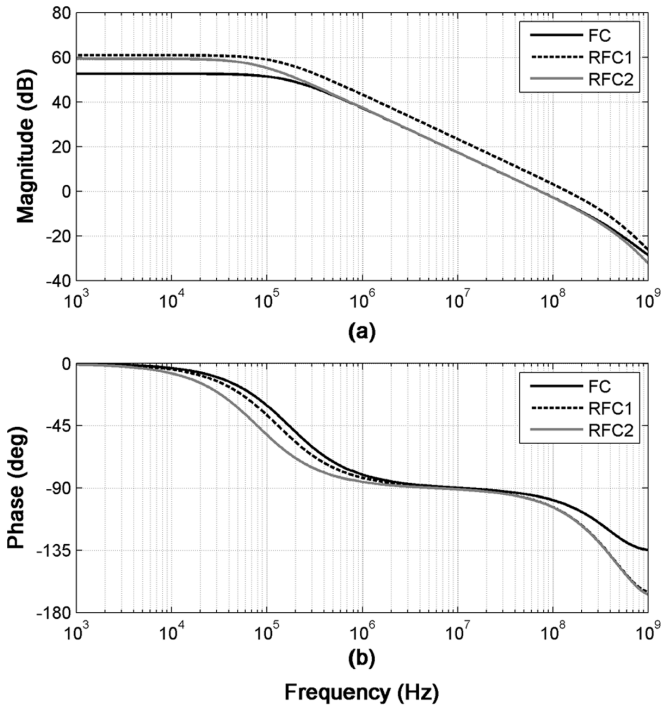

Fig. 6. Amplifiers AC response. (a) Magnitude. (b) Phase.

amplifiers can be extracted, and it is 46.02 dB for FC, 53.56 dB for RFC1 and 54.89 dB for RFC2. These gain values differ from their respective AC results of Fig. 6, which are 52.6 dB, 60.9 dB and 59.7 dB respectively. This discrepancy is partly caused by the inherent errors introduced by the transient signal (modulation of output impedance) and partly by the modeling of short channel effects. Nonetheless, the enhanced gain of the RFC over the FC is still apparent and within the expected range of 8–10 dB.

For the slew rate measurement, a large step, 1 Vpp at 5 MHz was applied to the amplifiers and the results are given in Fig. 8. Fig. 8, the RFC1 has a clearly improved slew rate over the FC despite the same bias current. Moreover, at half the bias current, the slew rate of the RFC2 is slightly better than the FC. The average slew rate of the FC, RFC1 and RFC2 is 42.15 $V/\mu s$, 94.13 $V/\mu s$, and 48.12 $V/\mu s$ respectively; that is the slew rate of the RFC1 is enhanced 2.23 times over the FC for the same bias current, while that of the RFC2 is enhanced 1.14 times over the FC for half the bias current. Furthermore, no signs of ringing are visible in either step response, which shows that the addition of the current mirrors $M3a$:$M3b$ and $M4a$:$M4b$ in the RFC amplifier signal path has negligible effects on the amplifiers phase margin.

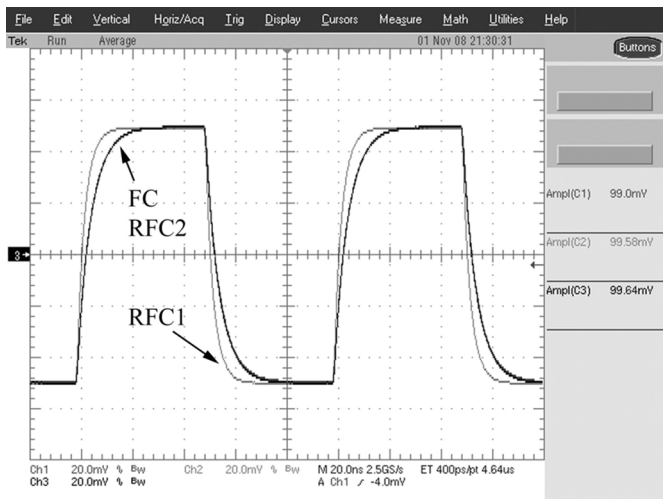

Fig. 7. Amplifier small signal step response.

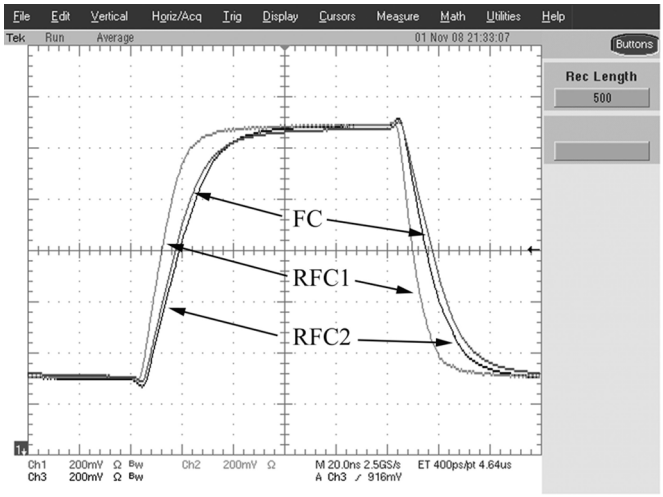

Fig. 8. Amplifier large signal step response.

The linearity of the amplifiers can be measured through their distortion behavior. A 1 Vpp two tone test centered at 1 MHz and separated by 100 kHz (500 mVpp at 0.95 MHz and 500 mVpp at 1.05 MHz) was applied to all amplifiers and the FFT data of the outputs was captured using the Tektronix TDS 5054 and plotted in MATLAB. The results are given in Fig. 9. The third intermodulation distortion, $IM3$, is -61.7 dB for the FC, -66.1 dB for RFC1 and -61.6 dB for RFC2.

According to the slew rate results presented earlier, the FC, RFC1 and RFC2 amplifiers can support signals up to 13.4 MHz, 29.9 MHz and 15.3 MHz respectively without slewing. Hence the distortion is solely due to the reduced amplifier gain around 1 MHz. The FC and RFC2 have almost identical bandwidths and hence it is not surprising to see them have similar IM3 performance, as they have the same gain around 1 MHz. The RFC1, on the other hand has a wider bandwidth and hence a higher gain around 1 MHz, which explains the improved IM3 performance.

The noise was characterized through simulations and the spectral density of the input referred noise is given in Fig. 10. When integrated over a bandwidth of 1 Hz–100 MHz, the noise of the FC, RFC1 and RFC2 is 53.16 μVrms, 48.48 μVrms and 69.71 μVrms respectively. Hence, for this particular design, the RFC1 has a better noise performance, while RFC2 has a worse noise performance as demonstrated by (24) and (25).

Similarly, the offset characterization of the amplifiers was performed through simulations as the number of physical samples was limited. Standard Monte Carlo simulations were used, where statistical variations of process parameters affecting individual device threshold voltage and carrier mobility as characterized by TSMC models were performed along with temperature variations ($-40\,^{\circ}$C, $25\,^{\circ}$C, and $85\,^{\circ}$C). Relying on the feedback network, the offset was extracted by noting the node voltage difference of the positive and negative amplifier inputs. The results are summarized in Fig. 11. While the offset standard deviation is similar for both FC and RFC1, it is larger for RFC2 as demonstrated by (26). Also, a non-zero mean is observed in Fig. 11 due to systematic offset, not random process variations.

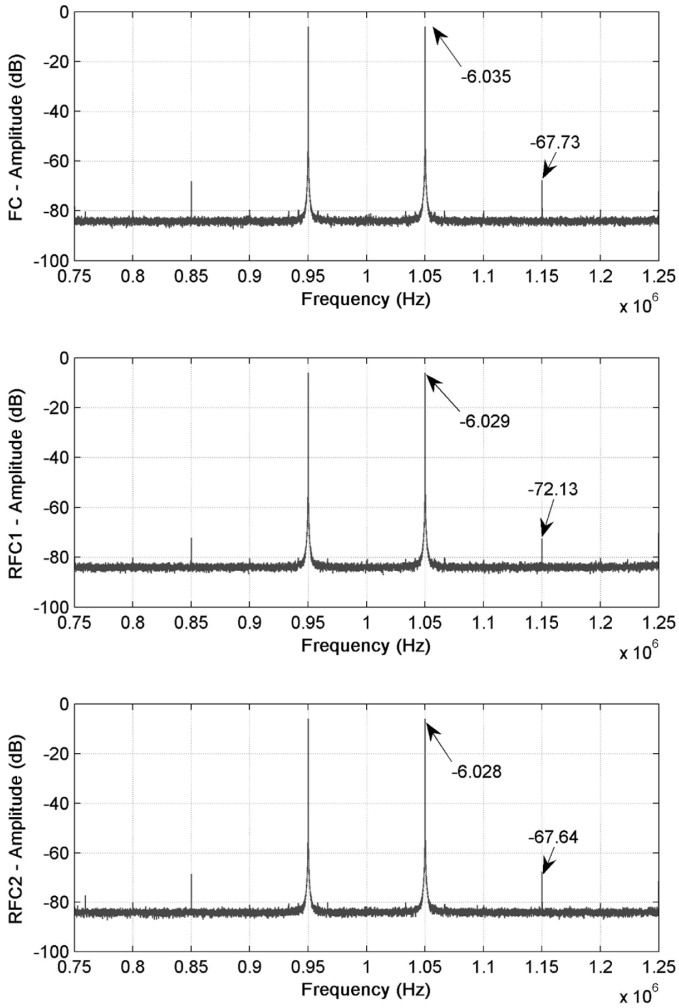

Fig. 9. Two tone FFT spectrums of the FC, RFC1 and RFC2 for a 1 Vpp signal centered at 1 MHz and separated by 100 kHz.

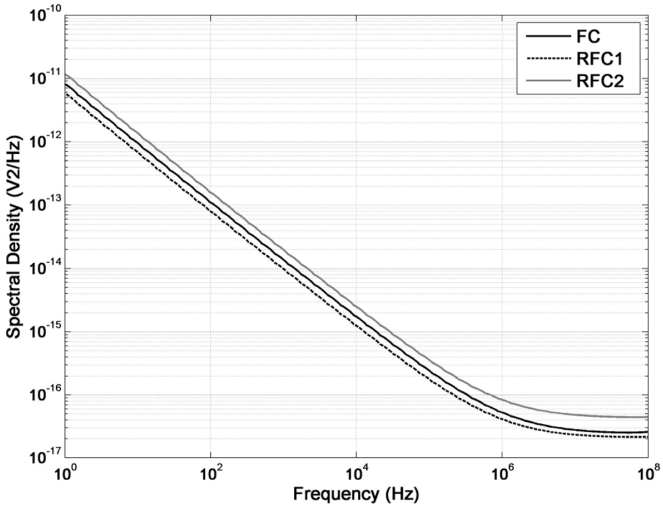

Fig. 10. Input referred noise spectral power density.

This systematic offset has two components. First, there is a finite current drawn by the load $(2R)$. Second, the feedback network sets the output to $\mathrm{V_{DD}}/2$, while ideally $Vout$ should follow the

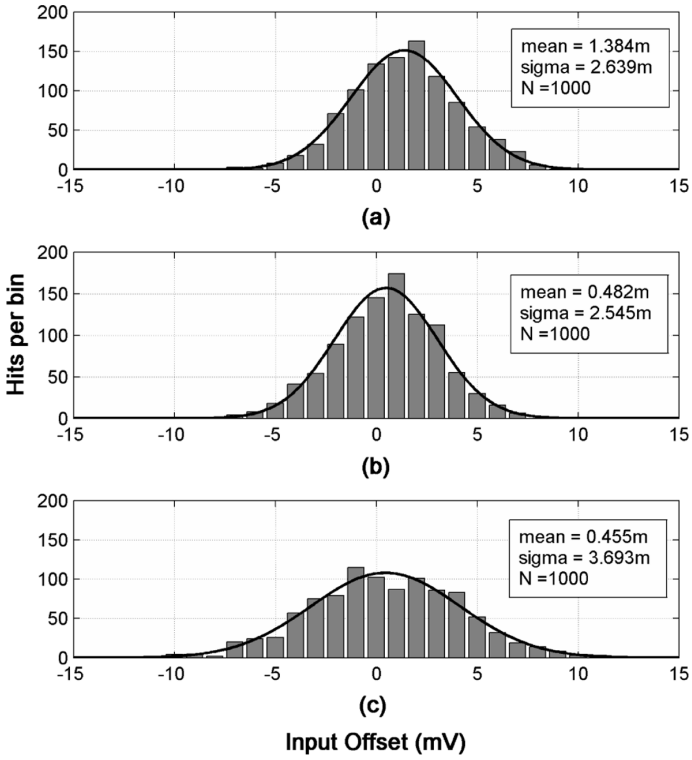

Fig. 11. Input offset distributions. (a) Conventional folded cascode. (b) Recycling folded cascode 1. (c) Recycling folded cascode 2.

gate voltage of $M9$. This systematic offset is more evident in FC because of its lower DC gain.

VI. Conclusion

It has been demonstrated that the proposed modifications to the conventional folded cascode, using the same area and power budgets, can boost the gain, bandwidth and slew rate without adversely affecting the noise performance or introducing offset, which results in a better FoM. On the other hand, by using half the area and half the power budgets of the conventional folded cascode, the proposed amplifier is still capable of delivering the same dynamic performance, but on the expense of a 2.3 dB noise increase and 40% added offset. The theoretical results were confirmed with good agreement by both experimental and simulation data.

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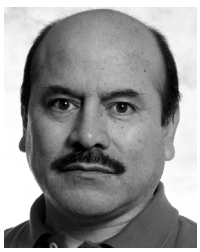

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