Low Voltage Low Power Class-AB OTA with Negative Resistance Load

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***Abstract*—In this paper, a low voltage low power rail to rail class-AB OTA in standard CMOS technology is proposed. The architecture is based on current mirror OTA topology with a local feedback between the output nodes of the first stage. The negative resistance load (NRL) is employed for compensation parasitic resistance of the first stage and the dc gain of the proposed OTA is enhanced. Compared to conventional voltage controlled NRL circuit transistor sizing controlled NRL circuit is used to avoid negative voltage circuits in the proposed OTA. Class AB output stage is implemented to obtain rail to rail output swing and higher slew rate. Using a 0.18-um standard CMOS process, the OTA has been designed to operate with 1V supply voltage. For a load capacitance of 5pf the proposed OTA achieves DC gain of 58.25dB, GBW of 50MHz, phase margin of 61 degrees, and slew rate of 2.3v/uS with a quiescent power consumption of 67uW.**

I. INTRODUCTION

CMOS technology is continually scaled down to achieve low-cost, high density, lower power and high speed digital systems [1]. With the scaling down of the CMOS technology, it is necessary to reduce the supply voltage to ensure device reliability. On the other hand, portable electronics has been developed rapidly and they are often battery-operated systems. They also need reduced supply voltage when considering the battery weight and lifetime. However, the threshold voltage is not scaled proportionally with the supply voltage to avoid higher off-state transistor current.

OTA is a very important building block and is often used in many systems, such as ADC or filters. In such applications, high dc gain of the OTA is a very important performance to ensure the performance of the whole system. However, it is becoming more and more difficult to obtain high dc gain of OTA with low voltage decreasing. Cascoding [2] is an effective method to enhance the dc gain of OTA while it will not be applied to low voltage environment because of the limit of output swing. Multistage [3] is another effective way to get high dc gain through more than two stages cascaded. However, it is very complicated to achieve stable. What's more, multistage will need frequency compensation and this will cause bandwidth reduction and extra power consumption.

The power consumption of digital circuits will reduced with the supply voltage scaling while it is not the case for analog circuits. This is because for deep submicron transistor the square law vanishes and the corresponding value of transconductance per unit current is low [4]. However, Low power is very important in portable applications to extend the life of battery. Thus reduction the power consumed in analog circuits is another challenge in low voltage circuits.

A current mirror class-AB OTA with negative resistance load is proposed in this paper. Section II describes the proposed OTA architecture, including the principle of the size controlled enhanced gain NRL, class-AB output stage and CMFB circuit. Section III describes the simulation results.

II. PROPOSED OTA ARCHITECTURE

As mentioned in [5] single-stage OTA is more power efficient than the two stage OTA because no power is wasted in driving the compensation capacitance in the single stage. To obtain lower power and rail to rail output swing, a current mirror OTA is used. With CMOS technology advanced the intrinsic voltage gain of the transistor is low due to the lower output impedance [5]. In this design, current mirror OTA combined NRL technique [6] [7] [8] is chosen to enhance the dc gain of the current mirror OTA. In additional, class-AB operation is used to improve power efficient further.

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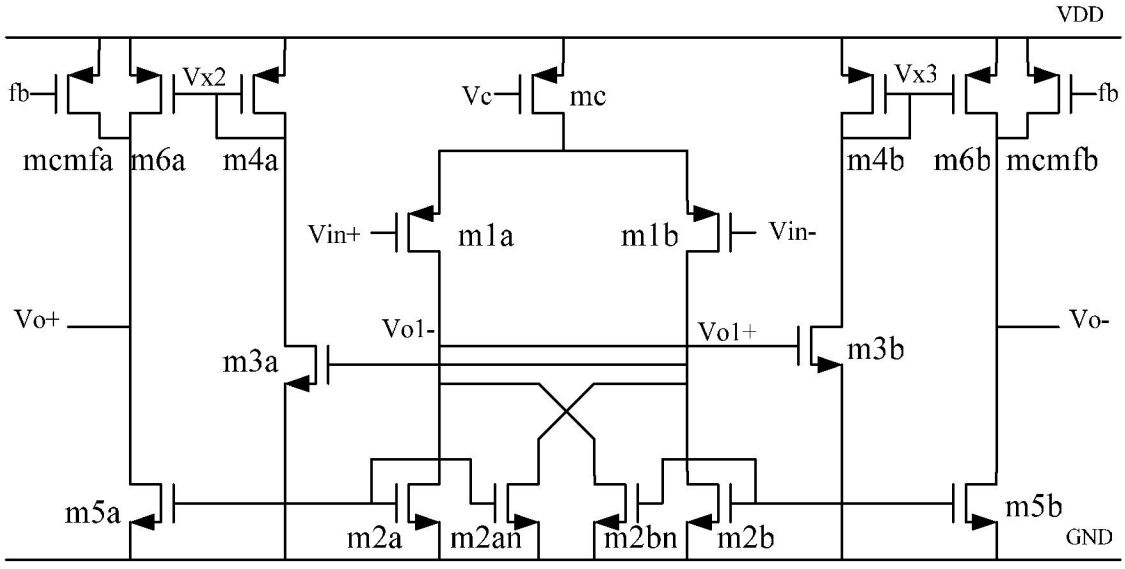


Figure 1. Schematic of the proped OTA.

A. *Enhanced Gain with NRL*

As shown in Fig.1, NRL is formed by M2a, M2b, M2an, and M2bn. The principle of this method is that M2an and M2bn introduce local positive feedback between the nodes Vo1+ and Vo1- and a negative resistance is produced which will be used to compensate the parasitic output resistance of the nodes Vo1+ and Vo1- [6]. This is very attractive for low voltage environment to improve dc gain of the OTA because it does not need stacked transistors which will introduce extra internal nodes.

PMOS input transistor is used and the input common mode voltage will be chosen ground. Thus NMOS switch is allowed to be connected to the input common mode voltage of the OTA and will work properly with 1V supply voltage without bootstrapped circuits or voltage-double circuits. If using voltage-controllable negative resistance just like [6] a negative voltage will be necessary for NMOS loads, which will make circuit more complicated. In this design, the negative resistance could be well controlled by sizing M2an and M2bn.

Fig.2 shows the small-signal model of half circuit equivalent of the first stage, where gm1 is the small signal transconductance of M1a and M1b.

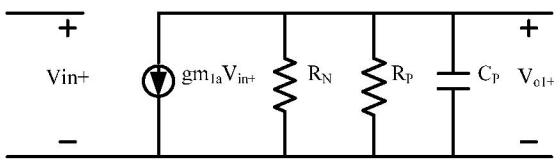


Figure 2. Small-signal model of half equivalent circuit of node Vo1+

From this model, the transfer function of first stage is given by

$$A(s)=\frac{Vol(s)}{Vin(s)}=\frac{gm_1}{\frac{1}{R_P}+\frac{1}{R_N}+sC_P} \tag{1}$$

Where Cp is parasitic capacitor

The equivalent negative resistance R_N is derived as

$$R_N=-\frac{1}{gm_{2bn}-gm_{2a}} \tag{2}$$

From equal (2), we can see that R_N can be tuned by varying the size of M2b.

The parasitic output resistance of the first stage transconductance circuit R_P is shown as equal.(3).

$$R_P=\frac{1}{gds_{1a}+gds_{2a}+gds_{2bn}} \tag{3}$$

From equal (1), it can be derived that if R_N=R_P the dc gain of the first stage is infinite. To avoid instability, $gm_{2bn} \le gm_{2a}+1/R_P$ must be ensured. In actual simulation, to obtain a good phase performance (R_P-R_N) should not be too small although (R_P-R_N) is smaller and the dc gain of the first stage is larger. In this design, the sizes of M2a, M2b, M2an, and M2bn are equal and high load impedance for differential signal is obtained because the gm2a and gm2b can be cancelled by the gm2an and gm2bn, respectively.

B. *Class-AB Operation*

To obtain higher power efficiency, higher slew rate, and rail to rail output swing, class-AB operation is used. The class-AB push-pull output stage [9] is implemented by M3-M6.

C. *CMFB Circuit*

CMFB circuit is implemented by Switched capacitor CMFB circuit, shown in Fig.3 clk+ and clk- are two non-overlap clocks. Capacitor Cc is three time more than capacitor Cs. To ensure the proper operation of the switch, voltage doubler was used.

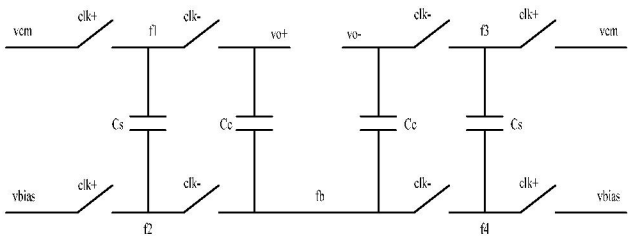
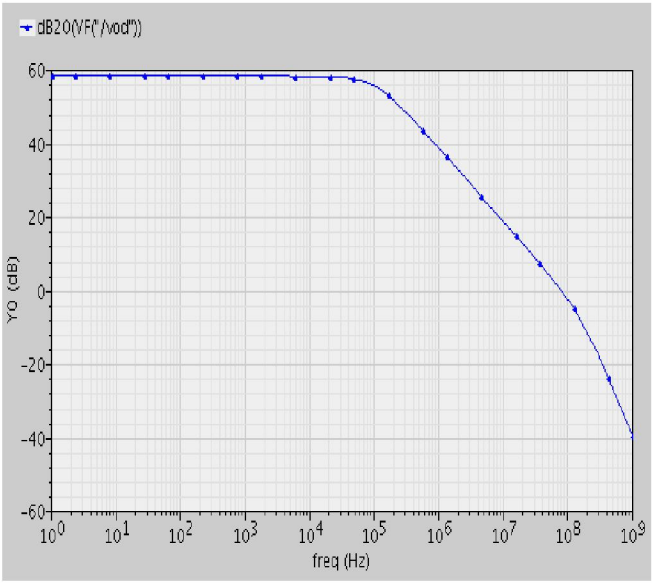


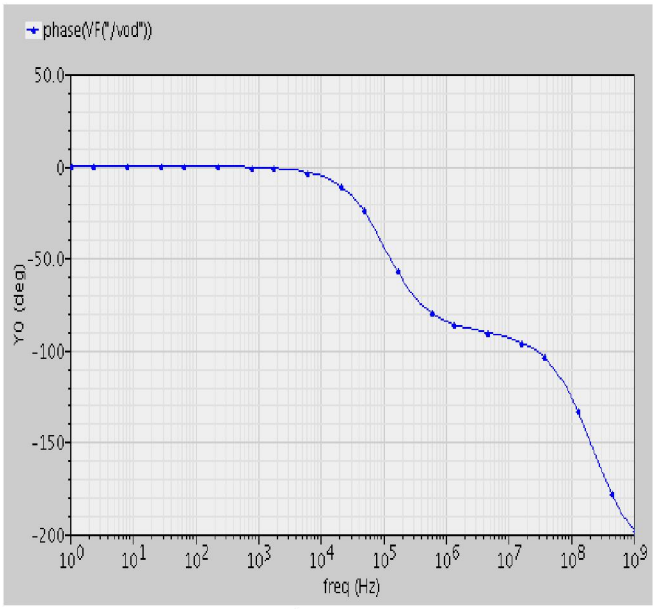
Figure 3. Switched capcitor CMFB circuit

III. SIMULTATION RESULTS

The proposed OTA has been designed and simulated using Cadence Spectra and 0.18um standard CMOS technology with V_{thn}=0.421v and V_{thp}=0.438v. The supply voltage is 1V and the load capacitor is 5pF. Fig.4 shows the simulated open loop frequency response of the proposed OTA. The GBW of the OTA is 79.53MHz and the power consumed by the whole OTA is 67uW. The dc gain of the OTA achieves 58.25dB and the phase margin is 61 degrees.



(a)



(b)

Figure 4. Open loop frequency response, where (a) gain response (b) phase response

The unity gain configuration with proposed OTA is shown in Fig.5. The input capacitor and feedback capacitor both are 1pf and the load capacitor is 5pf. The transient response of the unity gain configuration is shown in Fig.6. The upper signal is output signal and the below one is input signal. The common mode output voltage is 500mv. Table 1 show the simulated performance of the proposed OTA.

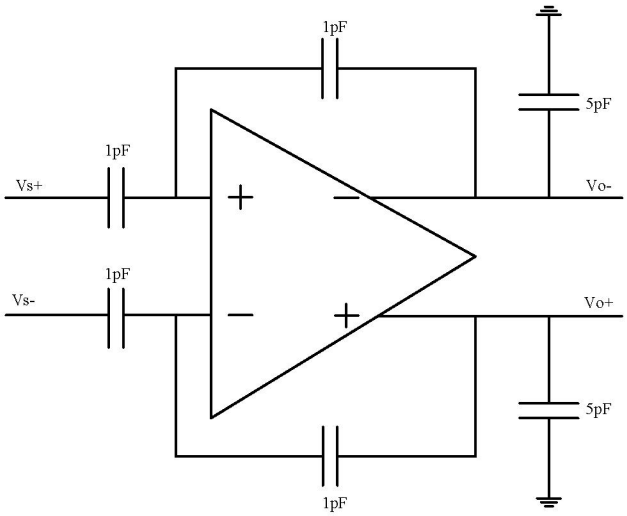


Figure 5. Unity gain configuration of the proposed OTA.

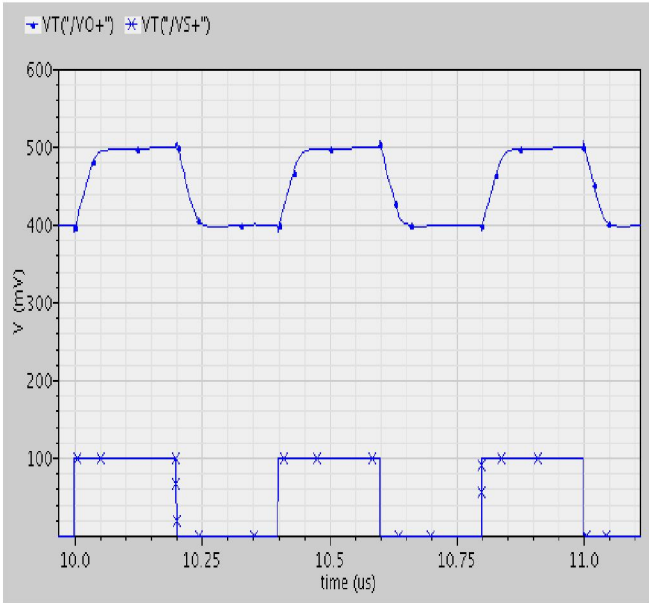


Figure 6. Simulated transient response

Table 1 summarizes the simulated performance of the OTA

TABLE I. SUMARIZES THE SIMULATED PERFORMANCE OF THE OTA

Parameter	Value
Vdd	1v
Load capacitor	5pF
DC Gain	58.25dB
Phase Margin	61degree
GBW	79.53Mhz
Slew Rate	2.3v/uS
Output swing	0.8Vpp
Power Consumption	67uW

IV. CONCLUSION

The proposed OTA is based on current mirror OTA with negative resistance load to improve dc gain. The dc gain can be enhanced by enlarging the sizes of the transistor M_2n and a moderate dc gain is achieved to ensure the stability of the OTA. In addition, class AB operation is used to achieve higher power efficiency and rail to rail output swing. The proposed OTA has a dc gain of 58.25dB with 5pf capacitor load and operates under 1V supply voltage. A GBW of 79.53MHz and phase margin of 61 degrees is achieved. This low voltage low power class-AB OTA is very suitable for low voltage switched-capacitor applications.

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