A Nano-Watt Power CMOS Amplifier with Adaptive Biasing for Power-Aware Analog LSIs

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***Abstract*— This paper presents an ultra-low power CMOS amplifier (AMP) using a simple and novel adaptive biasing current circuit (ABCC). The circuit uses a nano-ampere current source to achieve nano-watt power dissipation and the adaptive biasing technique to achieve high speed operation. The ABCC monitors the input voltages and supplies adaptive biasing current to the AMP. Because the adaptive biasing current is generated only when the AMP does not maintain its "virtual short" characteristic in the feedback configuration, the circuit operates with nano-watt power dissipation. Measurement results demonstrated that the circuit can operate with ultra-low power of 325 nA and high speed of 0.0506 V/μs at the rise time and 0.0579 V/μs at the fall time, when the input pulse frequency and the amplitude were 1 kHz and 0.8 V_{pp}.**

I. Introduction

One of the most arduous and challenging research areas in microelectronics is the development of ultra-low power CMOS LSIs capable of handling nano-ampere current [1]–[4]. However, methods for designing such LSIs have not been established yet. Thus, we have to explore and expand design techniques to achieve ultra-low power LSI systems. At a step toward this goal, we here describe an ultra-low power CMOS amplifier (AMP) using a simple and novel adaptive biasing technique for extremely low power analog LSIs.

The AMP is one of the most fundamental and important building blocks of linear CMOS circuits, switched capacitor circuits, and so on. It usually dissipates most of the dc power used up by the device. Therefore, low power design techniques are strongly required. The most effective and direct way to reduce power dissipation is to reduce the bias current to nano-ampere. However, because it is the bias current that mainly determines AMP performance, the poor driving capability that results from reducing it to this level degrades the performance. For example, an AMP's transient response time can be expressed in term of the $C_L V_{TAG}/I_{BIAS}$ relationship, where C_L is output capacitance, V_{TAG} is target voltage swing, and I_{BIAS} is bias current. A low bias current will therefore degrade the response time and make it difficult to support high-speed and low-power operation at the same time.

A CMOS AMP using an adaptive biasing technique was proposed by Degrauwe and others to address this issue [5]. The technique can achieve low power dissipation and extend driving capability even though the circuit is operated at a low bias current [6]. However, the AMP cannot generate a large drive current because the adaptive bias current is limited by the current mirror ratio used in the AMP. Therefore, sufficient performance improvement cannot be obtained. To enhance the drive current, several adaptive biasing AMPs have been investigated [7]–[10]. However, because these AMPs consume high power dissipation, they cannot be used in power-aware applications.

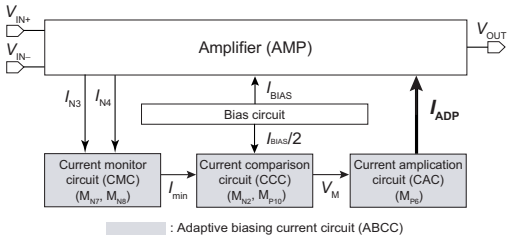

Fig. 1. Proposed amplifier architecture.

In light of this background, we have developed CMOS AMP using a simple and novel adaptive biasing current circuit (ABCC). The ABCC monitors the input voltages as current, and compares the current with reference current in the feedback configuration. It generates a large amount of adaptive bias current only when the AMP does not maintain its "virtual short" characteristic. Therefore, the proposed circuit can simultaneously achieve both low power and high speed. Its details are described in the following section.

II. Amplifier Design

Figure 1 shows the architecture of our proposed circuit. It consists of a bias circuit, an AMP and an ABCC. In order to achieve ultra-low power dissipation, a nano-ampere current generator is used as the bias circuit [3]. The ABCC consists of a current monitor circuit (CMC), a current comparison circuit (CCC), and a current amplification circuit (CAC). The CMC monitors the currents flowing in the input differential pair and detects the smaller current between them. The CCC accepts the current and compares it with the bias current. The CAC generates an adaptive bias current I_{ADP} on the basis of the comparison result. When the two input voltages are equal, no I_{ADP} is generated. On the other hand, when they are not equal, I_{ADP} is generated so that they become the same. The schematic of the proposed circuit is shown in Fig. 2. The operation principles of the circuits are as follows.

A. CMC: Current Monitor Circuit

The CMC consists of two MOS transistors connected in series (M_{N7} and M_{N8}). It monitors currents flowing through

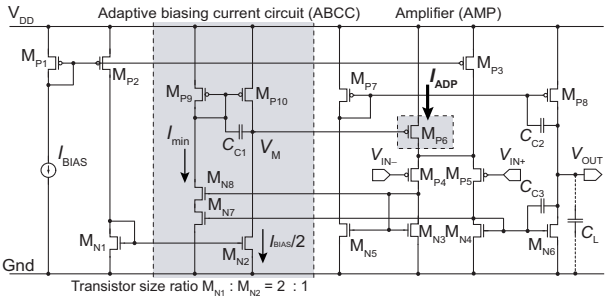

Fig. 2. Schematic of the proposed amplifier.

the input differential pair and copies the smaller current between them. Because the CMC's output current I_{min} is determined by the gate-source voltages of transistors $\mathrm{M_{N7}}$ and $\mathrm{M_{N8}}$, smaller gate-source voltage, or smaller current, will limit the current flowing in the CMC. For example, if I_{N4} is smaller than I_{N3}, the output current I_{min} will be I_{N4}. On the other hand, when the input voltages are equal, because I_{N3} is equal to I_{N4}, the CMC generates I_{min} on the basis of $I_{N3}(= I_{N4})$. Note that the CMC generates maximum current at the condition ($V_{IN+} = V_{IN-}$) and the current decreases as input voltage difference increases.

B. CCC: Current Comparison Circuit

The CCC consists of a common source amplifier comprising the MOS transistors $\mathrm{M_{P10}}$ and $\mathrm{M_{N2}}$. It compares I_{min} with bias current of $I_{BIAS}/2$ and generates V_M as the comparison result. As explained before, the CMC generates maximum current when input voltages are equal. Therefore, V_M will be a maximum voltage at the condition ($V_{IN+} = V_{IN-}$) and will decrease from this maximum when the input voltage difference becomes large.

C. CAC: Current Amplification Circuit

The CAC consists of a MOS transistor $\mathrm{M_{P6}}$. It accepts voltage of V_M and generates the adaptive biasing current I_{ADP} on the basis of the voltage level of V_M. Because the CAC is composed of a pMOS transistor, more I_{ADP} is generated as V_M decreases.

D. Operation of ABCC

As shown in Figs. 1 and 2, our proposed ABCC is included in a feedback loop. Within the loop, it generates I_{ADP} only when the input voltages are not equal. Because the input voltages play an important role in the ABCC operation, we describe the operation in term of these voltages.

1) Input voltages: $V_{IN+} = V_{IN-}$

   When the input voltages are equal and the total current flowing in the input differential pair is $I_{BIAS}+I_{ADP}$, the output current I_{min} of CMC can be expressed as

$$I_{min} = \alpha \left(\frac{I_{BIAS} + I_{ADP}}{2} \right), \qquad (1)$$

   where α is the CMC's current gain factor and is less than 1 ($\alpha < 1$). The CCC accepts current I_{min} and compares it with $I_{BIAS}/2$. Because the V_M voltage is determined by these currents, it settles at a voltage such that I_{min} is equal to $I_{BIAS}/2$.

2) Input voltages: $V_{IN+} \neq V_{IN-}$

   When the input voltages are not equal, most of the current flows through one or the other of the input differential pair paths. The CMC generates current I_{min} from the smaller current. Because I_{min} becomes smaller than Eq. (1) in this case, V_M decreases and I_{ADP} becomes large.

As described above, a large amount of adaptive bias current I_{ADP} is generated only when the input voltages are not equal. This means that, when the AMP used in the feedback configuration does not maintain its virtual short characteristic, the ABCC detects the change and generates the adaptive bias current such that the AMP settles into the steady-state condition quickly. This enables faster operation speed to be achieved. Because the circuit operates with very small current I_{BIAS} at the steady-state of the AMP ($V_{IN+} = V_{IN-}$), it consumes low power.

III. Simulation Results

The performance of the proposed AMP (Prop.) was evaluated by using SPICE with a set of 0.18-μm parameters. V_{DD} was set to 3 V. For comparison, we also evaluated an AMP without an ABCC (Conv.1) and a conventional adaptive biasing AMP [5] (Conv.2: the current feedback factor was set to 0.5).

Figure 3 shows simulated waveforms of the proposed and conventional AMPs with a unity-gain buffer configuration. The amplitude and frequency of the input pulse and the bias current were set to 0.5-1.3 V_{pp}, 1 kHz, and 50 nA, respectively. The output capacitance was set to 1 pF. In the Fig. 3, (a) and (b) respectively show the waveforms and adaptive bias current I_{ADP}, and (c) and (d) are their partial enlarged views. When the input pulse was applied, all of the circuits operated correctly. As shown in (c), the output operation speed of Prop. was faster than that of Conv.2. This was because Prop. generated large adaptive biasing current I_{ADP}.

Table I summarizes the results obtained for the slew rates and current dissipation I_{total}. Slew rate SR was defined as the slope between 10% to 90% of the steady-state voltage. Although all the circuits showed small slew rates, those of Prop. and Conv.2 were higher than those of Conv.1 because both of the former used adaptive bias current techniques. Of the three, Prop. showed the highest SR with only a slight increase in current dissipation.

Figure 4 (a) shows a Bode diagram of the ABCC feedback loop. The loop gain and phase margin of the adaptive biasing loop were 43.9 dB and 61.3 degrees. This means that the loop exhibits stable operation. Figure 4 (b) shows a Bode diagram of the proposed AMP, for which the gain and phase margin were 61.5 dB and 57.5 degrees.

IV. Experimental Results

We fabricated a prototype chip of our AMP using a 0.18-μm standard CMOS process. Conv.1 and Conv.2 [5] were

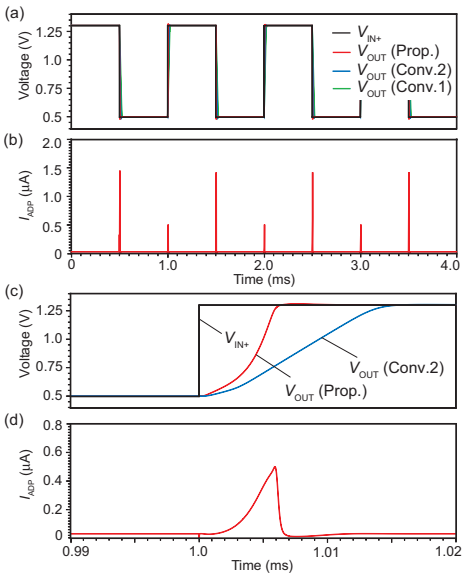

Fig. 3. (a) Simulated waveforms of the proposed and conventional AMPs, and (b) the current I_{ADP} of the proposed AMP. Partial enlarged view of (a) and (b) are respectively shown in (c) and (d).

TABLE I

SIMULATED SLEW RATES AND CURRENT DISSIPATION

Type.	SR^+ (V/μs)	SR^- (V/μs)	I_{total} (nA)
Prop.	0.165	0.221	321.5
Conv.1	0.035	0.033	152.3
Conv.2 [5]	0.066	0.061	268.5

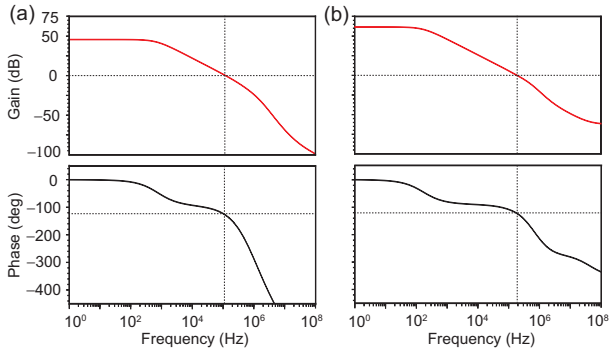

Fig. 4. Simulated Bode diagrams of the proposed circuit. Gain and phase of the ABCC feedback loop are shown in (a) and those of the proposed AMP are shown in (b).

also implemented in the same chip. Figure 5 (a) shows a micrograph of the chip and its partial enlarged views. The areas of Prop., Conv.2 and Conv.1 were 3807 μm^2, 3192 μm^2 and 2624 μm^2, respectively. In the measurements, input pulse and I_{BIAS} were set to 0.8 V_{pp} and 50 nA. We used a commercial operational amplifier as a buffer to drive the resistive and capacitive loads.

We measured the transient response of the proposed and conventional AMPs with a unity-gain configuration. Figure 5 (b)-(d) shows the measured waveforms. The input frequency was set to 1 kHz. The measured delays were slow compared with the simulation results because the output capacitance of the AMPs was larger than expected (simulations: 1 pF) due to the parasitic capacitance. Conv.2 and Prop. were faster

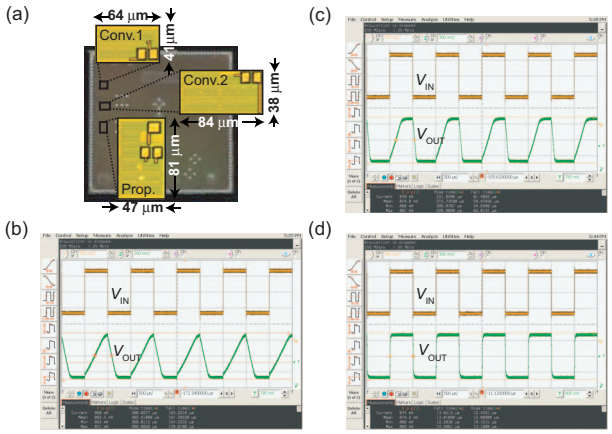

Fig. 5. (a) Chip micrograph and measured waveforms of (b) Conv.1 (c) Conv.2, and (d) Prop. at 1-kHz, 0.8 V_{pp} input pulse.

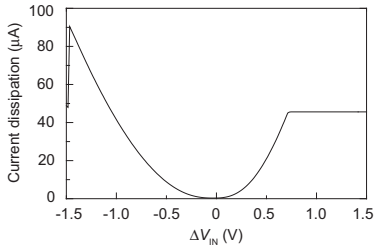

Fig. 6. Measured current dissipation as function of Δ V_{IN}.

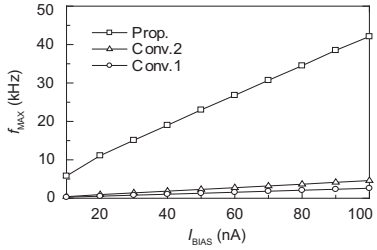

Fig. 7. Measured maximum operating frequency f_{MAX} as function of I_{BIAS}.

than Conv.1 because both of the former used adaptive biasing circuits. Prop. operated 28 times faster than Conv.1 at the rise time and 14 times faster at fall time. The speed-up rates were faster than those of simulation results. This is because our ABCC generated more current than that of Prop. in simulations. The larger the output capacitance becomes, the more adaptive biasing current is generated. If the output capacitance is small, it is charged quickly and the adaptive biasing current stops being generated. That is, the effects of the adaptive current become large when the output capacitance becomes large.

Figure 6 shows the measured current dissipation of our AMP as a function of $\Delta V_{IN} (= V_{IN-} - V_{IN+})$. V_{IN-} was set to 1.5 V and V_{IN+} was swept from 0 to 3 V. The current dissipation increased as Δ V_{IN} became larger. When $\Delta V_{IN} = 0$ ($V_{IN+} = V_{IN-}$), I_{ADP} was quite small, and the total current dissipation I_{total} was 325 nA. When $\Delta V_{IN} > 0.8$ V, the current was not generated correctly. This was because of the AMP's limited input range.

Figure 7 shows the measured maximum operating frequencies f_{MAX} as a function of bias current I_{BIAS}. Note that f_{MAX} was defined as the maximum input frequency at which the

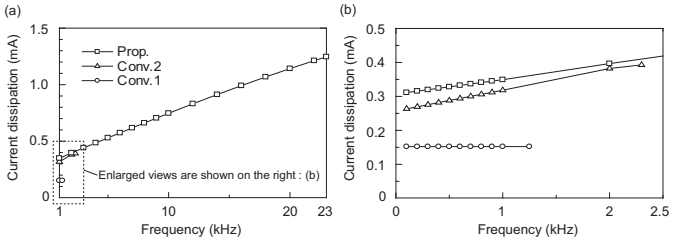

Fig. 8. (a) Measured current dissipation as function of input frequency. I_{BIAS} was set to 50 nA. (b) shows enlarged views of (a).

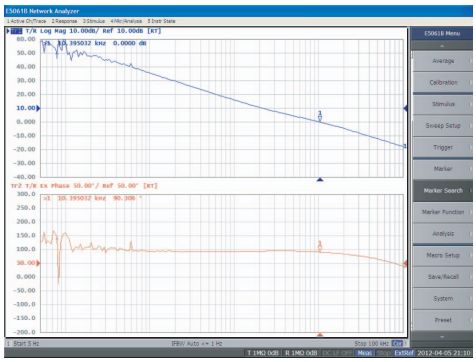

Fig. 9. Measured Bode diagram of the proposed circuit.

output voltage can follow the input pulse. For all the circuits, f_{MAX} increased with I_{BIAS}. Though f_{MAX} of Conv.2 was twice as fast as that of Conv.1, f_{MAX} of Prop. was 16 times faster than that of Conv.1.

Figure 8 (a) shows the measured current dissipations as a function of input frequency and partial enlarged views of (a) are shown in (b). The current dissipation of Conv.1 was independent of the input frequency because the circuit operated with constant bias current I_{BIAS}. In contrast, the current dissipations of Conv.2 and Prop. increased as the input frequency increased. Compared to Conv.2, Prop. operates at a higher frequency with smaller power overhead. This means that the proposed ABCC amplifies the current more effectively than the circuit in Conv.2.

Figure 9 shows the measured Bode diagram of the proposed circuit, for which the gain and phase margin were 60 dB and 90 degrees.

Table II summarizes measured AMP performances. The results showed that our proposed AMP can achieve high-speed, low-power and stable operation. In order to show the effectiveness of our AMP more clearly, we changed the bias current I_{BIAS} such that the proposed and conventional AMP would consume the same current dissipation at 1-kHz input. Under this condition, all of the AMPs consumed 200 nA. The results are shown in Table III. It was clear that our proposed AMP can achieve high speed operation with small bias current.

Table IV summarizes circuit performances in comparison with other adaptive biasing AMPs [8]–[10]. Our proposed AMP achieved the lowest power dissipation and the smallest area. Slew rates were inferior to others. This is because our AMP used nano-ampere bias current. However, as shown in Tabs. II and III, they were faster than other low-power amplifiers. Thus, it can be concluded that our AMP is useful for power-aware analog LSIs.

TABLE II

MEASURED PERFORMANCE SUMMARY OF AMPS

AMP	Prop.	Conv.2 [5]	Conv.1
Technology	0.18-μm CMOS		
Area	3807 μm^2	3192 μm^2	2624 μm^2
V_{DD}	3.0 V		
I_{BIAS}	50 nA		
SR^+ (f_{IN}=1 kHz)	0.0506 V/μs	0.0032 V/μs	0.0018 V/μs
SR^- (f_{IN}=1 kHz)	0.0579 V/μs	0.0118 V/μs	0.0043 V/μs
I_{total} (f_{IN}=1 kHz)	352 nA	323 nA	152 nA
f_{MAX}	23 kHz	2.3 kHz	1.3 kHz
open-loop gain	60dB	50dB	50dB
phase margin	90°	96°	99°

TABLE III

MEASURED PERFORMANCE UNDER THE SAME CURRENT DISSIPATION

AMP	Prop.	Conv.2 [5]	Conv.1
I_{total} (f_{IN}=1 kHz)	200 nA		
I_{BIAS}	25 nA	27 nA	66 nA
SR^+ (f_{IN}=1 kHz)	0.0358 V/μs	0.0017 V/μs	0.0024 V/μs
SR^- (f_{IN}=1 kHz)	0.0247 V/μs	0.0039 V/μs	0.0055 V/μs
f_{MAX}	13.5 kHz	1.3 kHz	1.6 kHz

TABLE IV

COMPARISON OF REPORTED ADAPTIVE BIASING AMPS

AMP	This work	[8]	[9]	[10]
Technology	0.18-μm	0.5-μm	90-nm	0.18-μm
Area (mm^2)	0.0038	0.054	simulation	simulation
I_{total} (μA)	0.35(@1 kHz)	110 (static)	80	1.25
SR^+ (V/μs)	0.05	10(@80pF)	37(@10pF)	0.12(@10pF)
SR^- (V/μs)	0.06	15(@80pF)	-	-
GBW	10 kHz	3.27 MHz	9.5 MHz	40 kHz
DC Gain	60dB	37dB	80dB	51dB
Phase margin	90°	56°	85°	65°

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