HW #8

Cahlen Brancheau #54

30/30

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	Add	Sub	Lw	Sw	BEQ	Addi
RegDst	1	1	0	D	D	0
ALUSrc	0	0	1	1	0	1
MemToReg	0	0	1	D	D	0
Reg Write	1	1	1	0	0	1
PCSrc	0	0	0	0	1	0
Mem Write	D	D	0	1	0	D
Mem Read	D	D	1	0	0	D
ALU OP	add	Sub	add	add	Sub	add

✓

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NewLW rd, rs(rt) op rs rt rd # [rd] ← Mem[[rs]+[rt]]

RegDst 1
ALUSrc 0
MemToReg 1
Reg write 1
Mem Read 1
Mem write 0

No changes required. ✓

✓

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