

HW #8

Cahlen Brancheau #154

19

30  
30

	Add	Sub	Lw	Sw	BEQ	Addi
RegDst	1	1	0	0	0	0
ALUSrc	0	0	1	1	0	1
MemToReg	0	0	1	0	0	0
RegWrite	1	1	1	0	0	1
PCSrc	0	0	0	0	1	0
MemWrite	0	0	0	1	0	0
MemRead	0	0	1	0	0	0
ALU OP	add	sub	add	add	sub	add

✓

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NewLWrd, rs(rt) op rs, rt rd  $\neq$  [rd]  $\leftarrow$  Mem[rs] + [rt]

RegDst 1  
ALUSrc 0  
MemToReg 1  
RegWrite 1  
MemRead 1  
MemWrite 0

No changes required.

✓

✓



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Start →

0 IF

ALUSrcA=0  
ALUSrcB=01  
ALUOp=00  
PCSrc=00  
PCWrite=1  
MemRead=1  
JorD=1  
IRWrite=1

→ 1 ID

ALUSrcA=0  
ALUSrcB=11  
ALUOp=00

Op=00

Op=NotEq

2 EX

ALUSrcA=0  
ALUSrcB=01  
ALUOp=01

4 EX

ALUSrcA=1  
ALUSrcB=00  
ALUOp=00

3 WB

MemToReg=0  
RegWrite=1  
RegDst=0

5 Mem

JorD=1  
MemRead=1

6 WB

MemToReg=1  
RegWrite=1  
RegDst=1

