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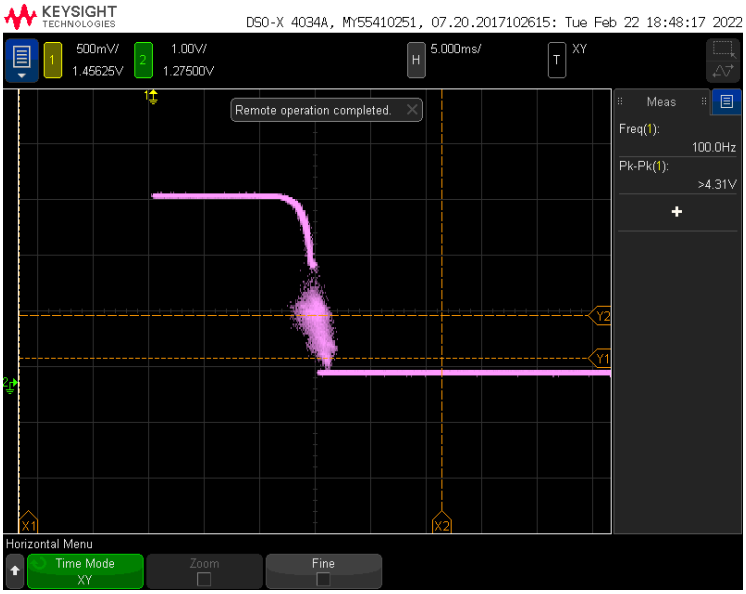
EE E3082. Digital Electronics Laboratory
Laboratory 1: Basic Digital Circuit Elements

1. XY-plot of the DC transfer function for a TTL-NAND gate. The x-axis is the output of the triangular wave, in volts, and the y-axis is the output of the TTL-NAND gate, in volts.

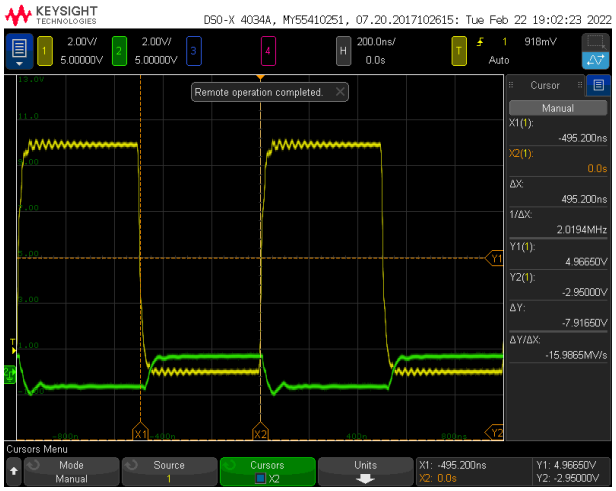


We found:
VIL = 1.218 V
VOL = 156.25 mV,
VIH = 1.442 V
VOH = 3.381 V

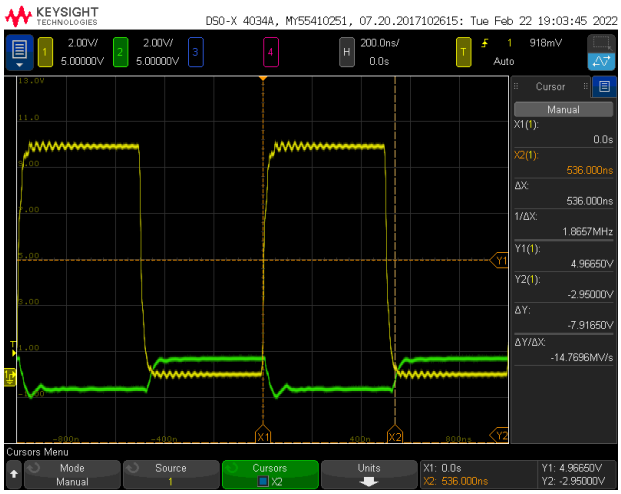
NMH = VOH - VIH = 1.939 V
NML = VIL - VOL = 1.062 V

We expect that with more capacitance, there should be less noise. Capacitors take time to charge, so the output would be smoothed as the capacitor slowly charged.

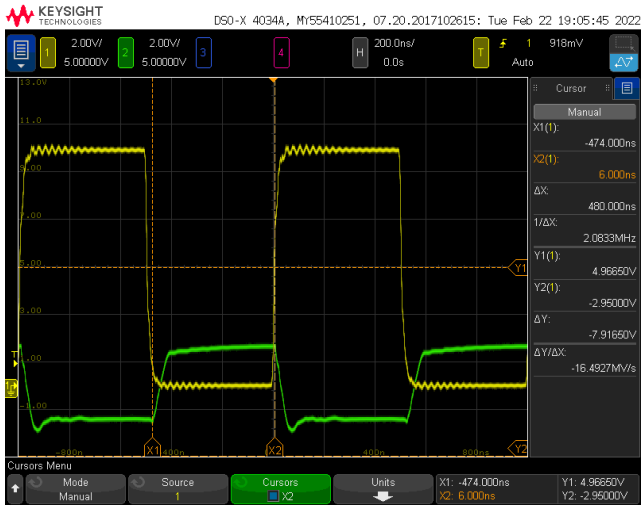
2. We applied at 1MHz output to the gate.
   For 66 pF of output load, we got two graphs, one for low to high, the other for high to low.



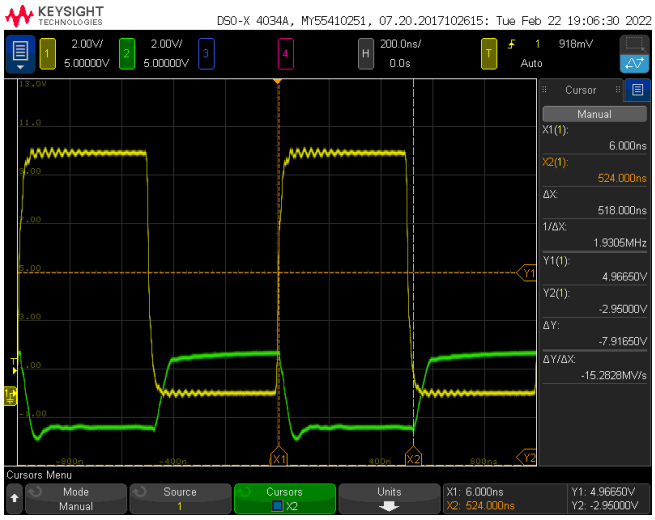
This is the graph with time stamps X1 and X2 delineated. The t_{pHL} here is 495.200 nanoseconds. Below is the same graph with time stamps X1 and X2 delineated, and the t_{pLH} here is 536.000 nanoseconds.



We did the same thing for 0.1 μF.
Below is the graph with which we calculated t_{pHL} = 480 nanoseconds.

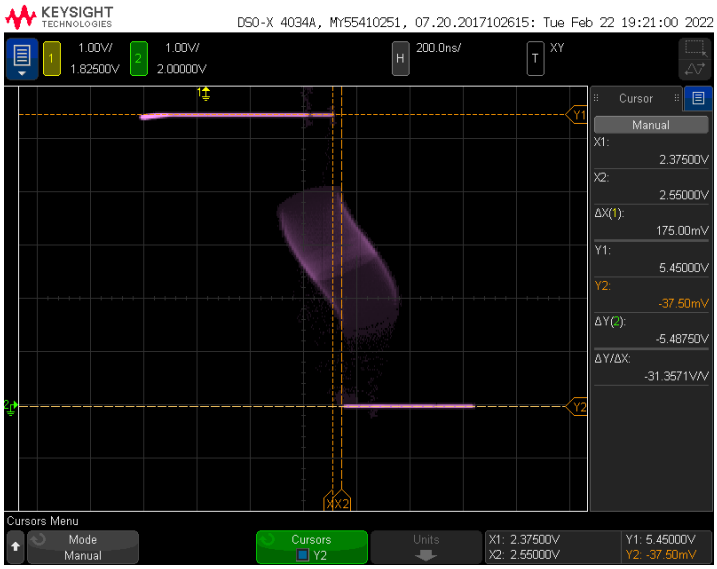


Below is the graph with which we calculated t_{pLH} = 518 nanoseconds.



We repeated Questions 1 and 2 for a CMOS 74HC00.

3.



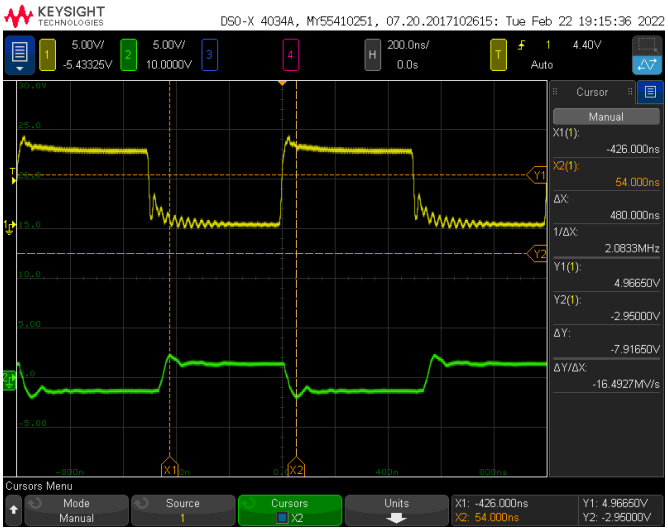
Above is the XY DC transfer plot for a CMOS 74HC00. The x-axis is the output of the triangular wave, in volts, and the y-axis is the output of the CMOS NAND gate, in volts.

We found:
VIL = 2.375 V
VOL = -37.50 mV
VIH = 2.550 V
VOH = 5.450 V

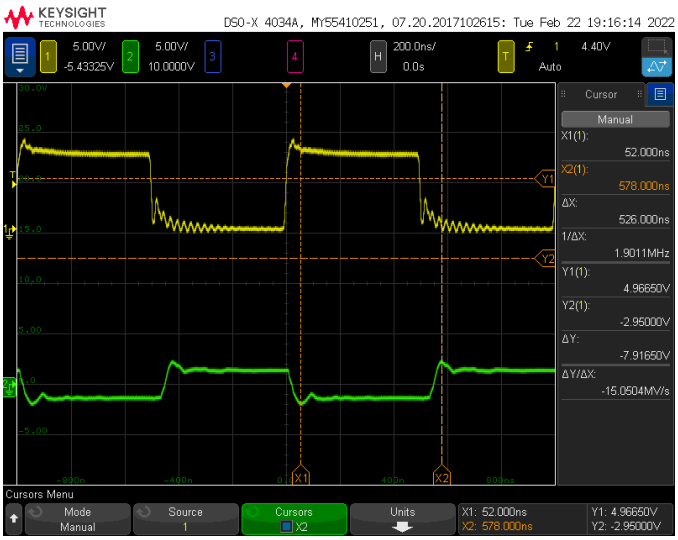
NMH = 2.90 V
NML = 2.41 V

Again, as mentioned before, a higher load capacitance would smooth the very blurred areas of the DC transfer plot that can be seen above.

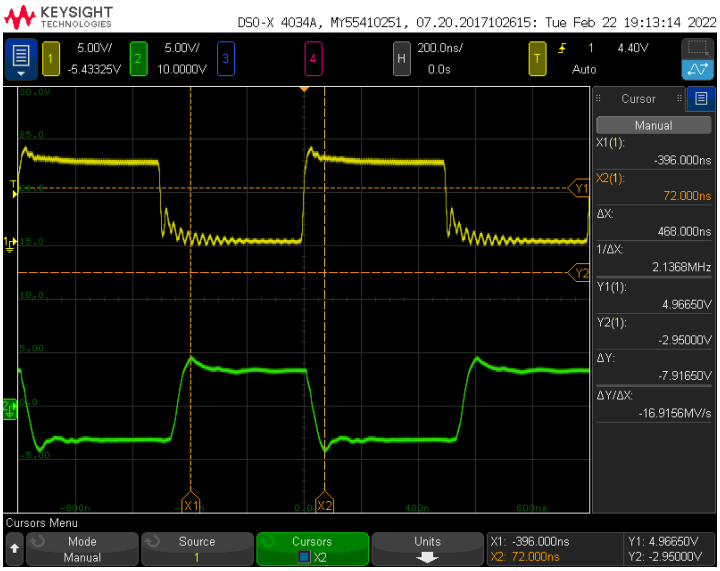
4. We applied at 1MHz output to the CMOS NAND gate.
   For 66 pF of output load, we got two graphs, one for high to low, the other for low to high.



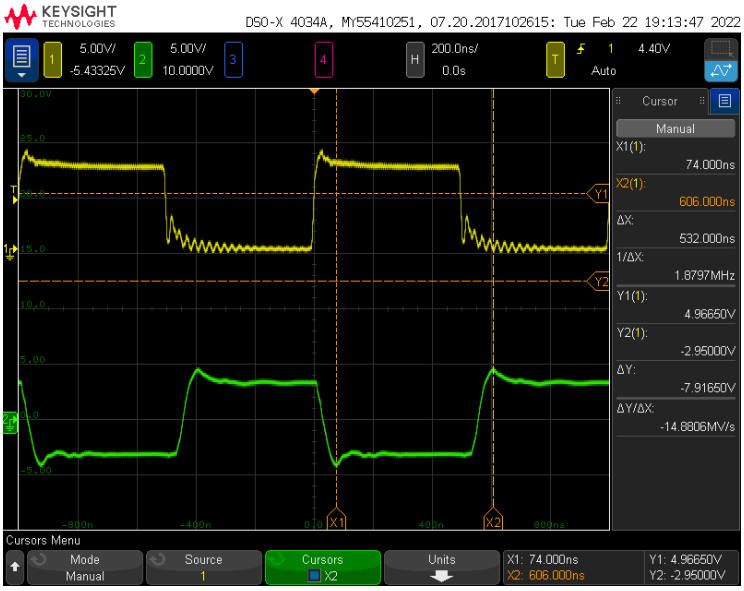
This is the graph with time stamps X1 and X2 delineated. The t_{pHL} here is 480.000 nanoseconds. Below is the same graph with time stamps X1 and X2 delineated, and the t_{pLH} here is 526.000 nanoseconds.



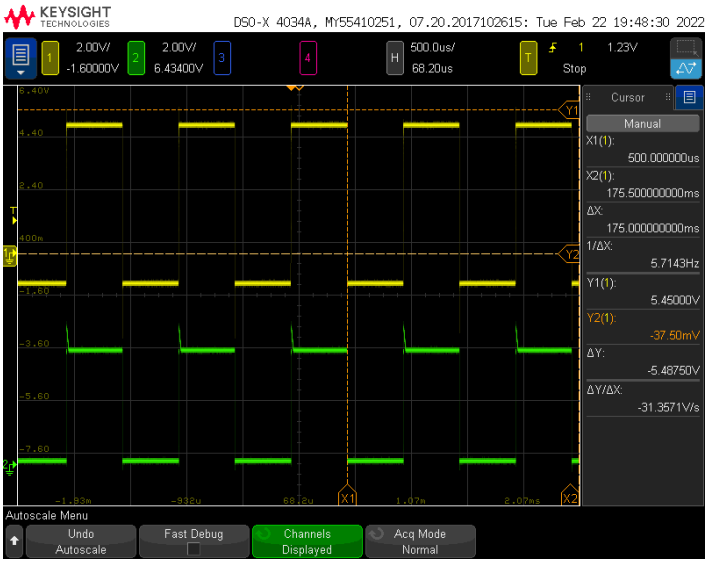
We did the same thing for 0.1 μF. Below is the graph with which we calculated t_{pHL} = 468 nanoseconds.



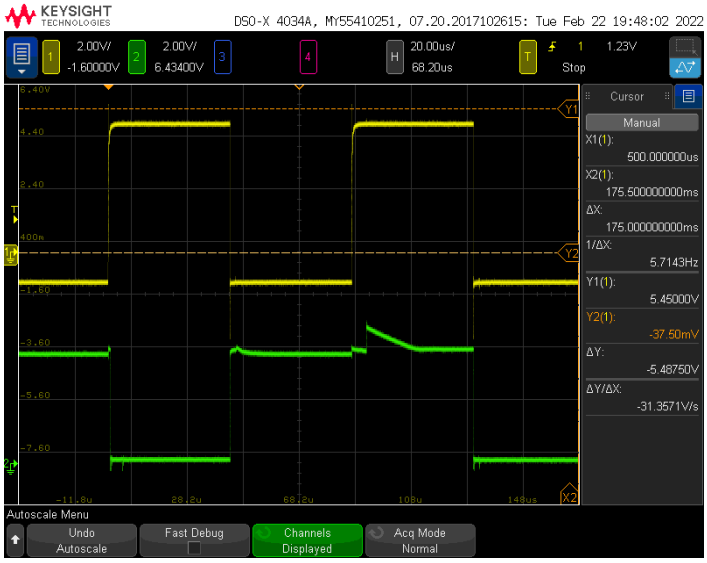
Below is the graph with which we calculated t_{pLH} = 532 nanoseconds.



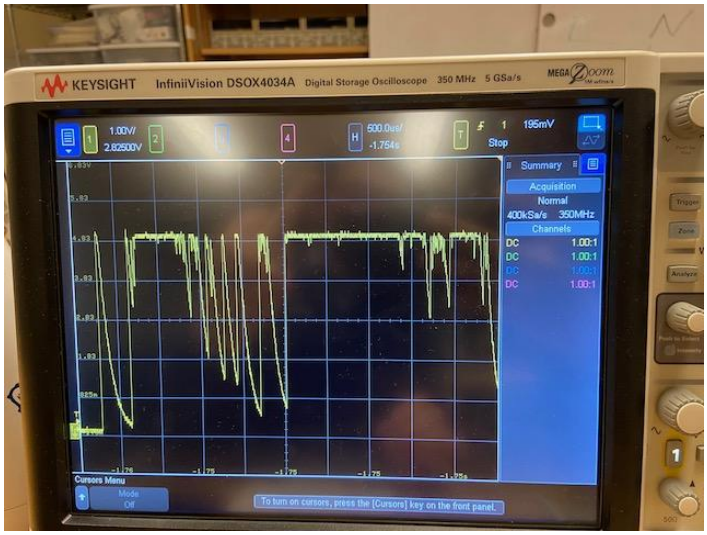
5.



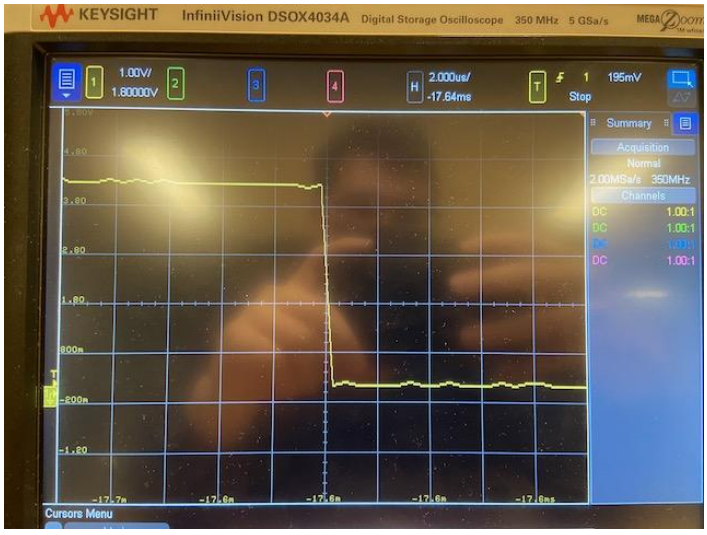
The input (yellow) and output (green) frequency are inverted. This broke down at 11.5 kHz, and can be seen below, where the inversion fails in the second pictured cycle.



6. The debouncer in Figure 4 operates by holding the new value of the button in a latch, acting as a buffer between the push button and the inputs to the main circuit. This prevents the main circuit from reading multiple button presses due to the mechanical bounce within the button. The button, when off, drives 5V to the R input, which resets the latch to 0, and when on, drives 5V to the S input, which sets the latch to 1 and drives a 5V input to the main circuit. In the counter design we built, the output from the SR latch was connected to the clock of the counter.



The switch output before debouncing shows a high number of false readings.



The switch output after debouncing shows a much more accurate reading with just one falling edge.

Our counter was signed off on in person and a video of the completed counter is available here. The schematic is as below: