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Experiment 4 Lab Report
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PMOS Common-Source Amplifier

DC Operating Point Analysis

Using the PMOS common-source amplifier, a simplified model of which is seen in *Figure 1*, allows for characteristic calculations of the circuit and transistor to be completed. A PMOS transistor, such as the CD4007 can be used.

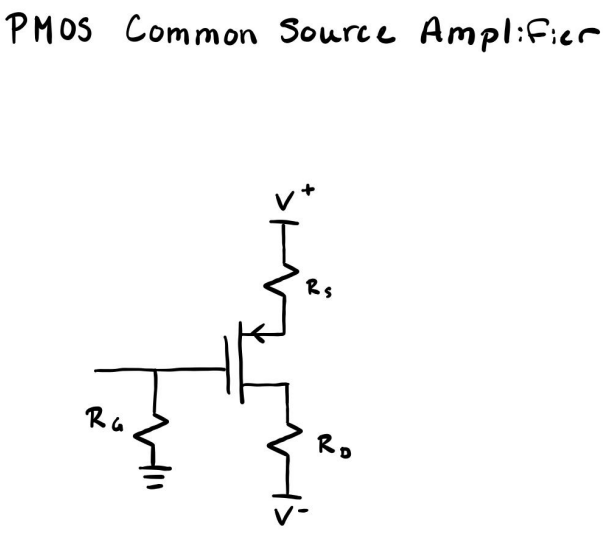

Figure 1: Simplified PMOS common-source amplifier.

The DC current going through R_g can be found to equal ~0A. This reveals that the transistor has an overdrive voltage of 2.12V, seen in the following calculation:

$$V_{OV} = V_{SG} - |V_{tp}|$$

$$I_D = \frac{1}{2} k_p' \frac{W}{L} (v_{SG} - |v_{tp}|)^2 \text{ such that}$$

$$v_{SG} = \sqrt{\frac{2I_D}{k_p' \frac{W}{L}}} + |v_{tp}|$$

$$V_{OV} = \sqrt{\frac{2I_D}{k_p' \frac{W}{L}}} + |v_{tp}| - |v_{tp}| = \sqrt{\frac{2I_D}{\mu_p \frac{\epsilon_{ox}}{t_{ox}} \frac{W}{L}}} = 2.12V$$

From there, we can calculate

$$g_m = \frac{2I_D}{V_{OV}} = 943.4\mu S$$

$$V_{SG} = V_{OV} + |V_{tp}| = 2.62\text{V}$$

$$r_o = \frac{1}{\lambda I_d'} = 23.8k\Omega$$

Finally, we can calculate R_S, which can be achieved by connecting resistors in any series or parallel combination to achieve R_S.

$$R_S = \frac{V_s - V_{ss}}{I_D} = 17.62k\Omega$$

AC Analysis

The PMOS common-source amplifier can be modeled using a small-signal analysis seen in *Figure 2*. The resulting model has no R_S, as a result of a bypass capacitor. Additionally, V_+ becomes part of the transconductance and acts to bias the circuit.

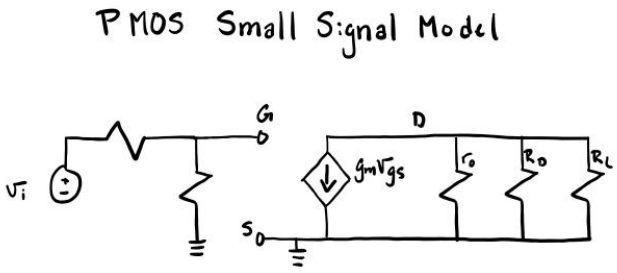

Figure 2: PMOS small-signal model.

By inspection, we can see that $v_i = v_{sig}$, as v_{sig} is the small signal input voltage for the model. This means that $\frac{v_i}{v_{sig}} \approx 1$. Further, the voltage gain, A_v, can be derived from the following calculations:

$$v_o = -g_m v_{gs} R_D$$

$$v_i = v_{sig} = v_{gs}$$

$$A_v = \frac{v_o}{v_i} = -g_m(R_D || R_L)$$

This would mean that, for a small-signal voltage gain of at least $A_v = -5\,V/V$, that $(R_D || 10k\Omega) = \frac{A_v}{-g_m} = 5.3k\Omega$ such that $R_D = 12.7k\Omega$. While this value isn't a standard resistance, it can be achieved by connecting resistors in any series or parallel combination to achieve R_D. The DC voltage at the drain is equal to -2.3V. Since $v_{DG} \geq |V_{tp}|$ the transistor is in saturation. Finally, r_o is equal to that found before: $r_o = \frac{1}{\lambda I_d'} = 23.8k\Omega$.

Simulation

Simulating this circuit with capacitances of 47µF and the resistance values found above provides the following outputs in *Figure 3, Figure 4,* and *Figure 5*. The DC values are seen in *Figure 6*.

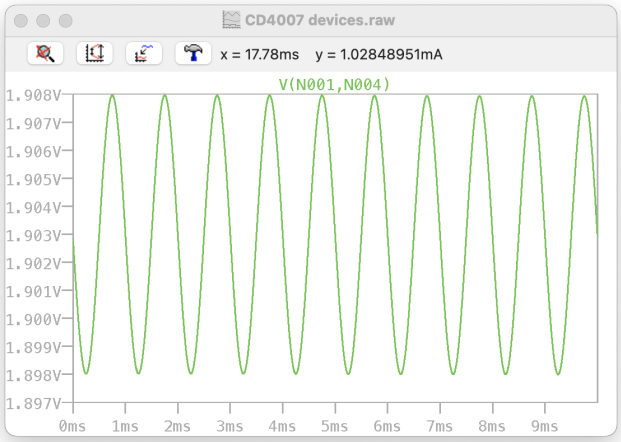

Figure 3: V_{SG}.

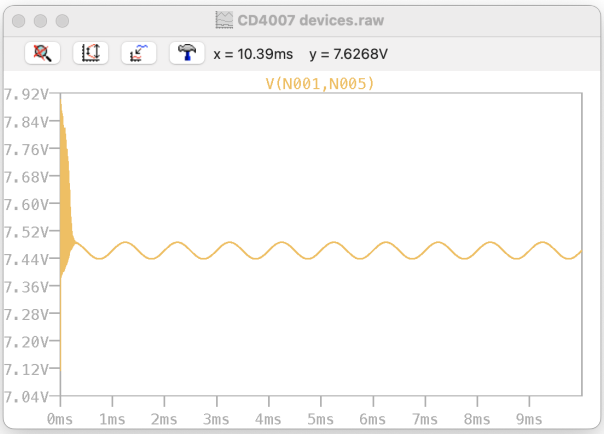

Figure 4: V_{SD}.

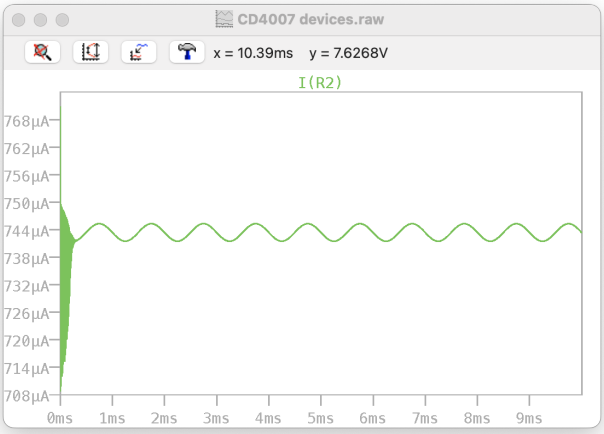

Figure 5: I_D.

V_{SG}	~1.90V
V_{SD}	~7.48V
I_D	~744µA

Figure 6: DC values of measurements.

These values seem to be consistent with the calculations, when it is taken into account that, because of the more complex model of a real transistor, there are some small variations. Finally, in *Figure 7* we can see the input and output signals. The observed output is closer to -4.9 V/V rather than -5 V/V.

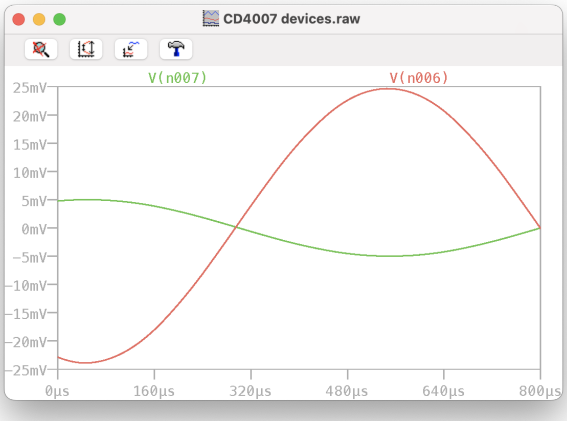

Figure 7: Input vs output signals.

NMOS Common-Source Amplifier

DC Operating Point Analysis

Using the NMOS common-source amplifier, a simplified model of which is seen in *Figure 8*, allows for characteristic calculations of the circuit and transistor to be completed. A NMOS transistor, such as the CD4007 can be used.

NMOS Common Source Amplifier

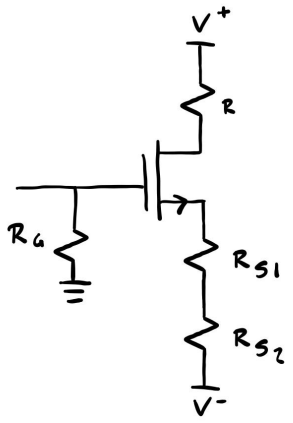

Figure 8: Simplified NMOS common-source amplifier.

The DC current going through R_g can be found to equal ~0A. This reveals that the transistor has an overdrive voltage of 2.88V, seen in the following calculation:

$$V_{OV} = V_{GS} - V_{tn}$$

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_{tn})^2 \text{ such that}$$

$$v_{GS} = \sqrt{\frac{2I_D}{k_n'\frac{W}{L}}} + V_{tn}$$

$$V_{OV} = \sqrt{\frac{2I_D}{k_n'\frac{W}{L}}} + V_{tn} - V_{tn} = \sqrt{\frac{2I_D}{\mu_n\frac{\epsilon_{ox}}{t_{ox}}\frac{W}{L}}} = 2.88V$$

From there, we can calculate

$$g_m = \frac{2I_D}{V_{OV}} = 694.4\mu S$$

$$V_{GS} = V_{OV} + V_{tn} = 3.98\text{V}$$

$$r_o = \frac{1}{\lambda I_d'} = 7.58k\Omega$$

Finally, we can calculate R_{S2}, which can be achieved by connecting resistors in any series or parallel combination to achieve R_S.

$$R_S = \frac{V_s - V_{ss}}{I_D} - 220\Omega = 10.98k\Omega$$

AC Analysis

The NMOS common-source amplifier can be modeled using a small-signal analysis seen in *Figure 9*. The resulting model has no R_{S2}, as a result of a bypass capacitor. The model does, however, have a R_{S1} component. Additionally, V_- becomes part of the transconductance and acts to bias the circuit.

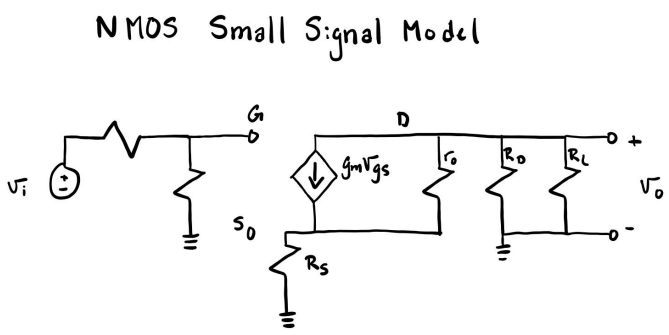

Figure 9: NMOS small-signal model.

By inspection, we can see that $v_i = v_{sig}$, as v_{sig} is the small signal input voltage for the model. This means that $\frac{v_i}{v_{sig}} \approx 1$. Further, the voltage gain, A_v, can be derived from the following calculations:

$$v_o = IR_D$$

$$I = \frac{g_m v_i}{1+g_m R_s}$$

$$v_i = v_{sig} = v_{gs}$$

$$A_v = \frac{v_o}{v_i} = -\frac{(R_D||R_L)}{1/g_m + R_S}$$

This would mean that, for a small-signal voltage gain of at least $A_v = -4\,V/V$, that $(R_D||10k\Omega) = A_V(-\frac{1}{g_m} + R_S) = 4.88k\Omega$ such that $R_D = 9.55k\Omega$. While this value isn't a standard resistance, it can be achieved by connecting resistors in any series or parallel combination to achieve R_D. The DC voltage at the drain is equal to $V_D = 1mA(9.55k\Omega) - 15V = -5.45V$ meaning that since $v_{GD} \leq V_{tn}$ that the transistor is in saturation.

Simulation

Simulating this circuit with capacitances of 47μF and the resistance values found above provides the following outputs in *Figure 10, Figure 11,* and *Figure 12*. The DC values are seen in *Figure 13*.

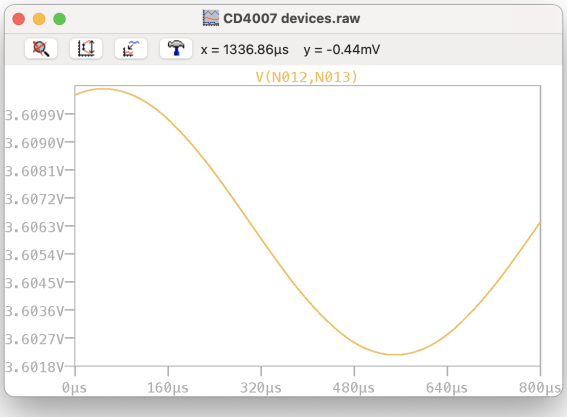

Figure 10: V_{GS}

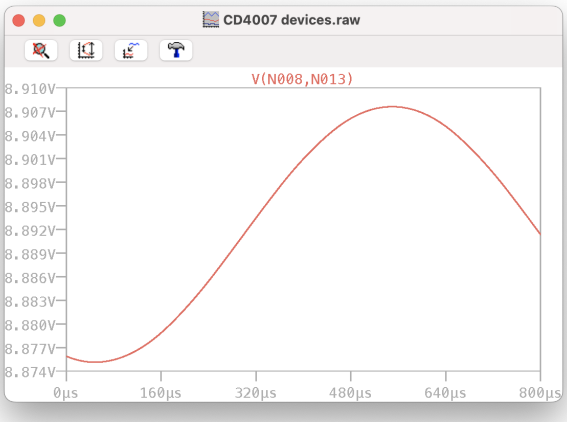

Figure 11: V_{DS}

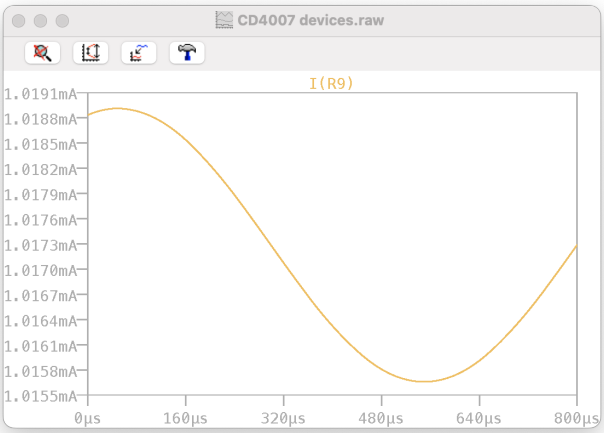

Figure 12: I_D.

V_{GS}	~3.60V
V_{DS}	~8.89V
I_D	~1.02mA

Figure 13: DC values of measurements.

These values seem to be consistent with the calculations, when it is taken into account that, because of the more complex model of a real transistor, there are some small variations. Finally, in *Figure 14* we can see the input and output signals. The observed output is closer to -3.08 V/V rather than -4 V/V.

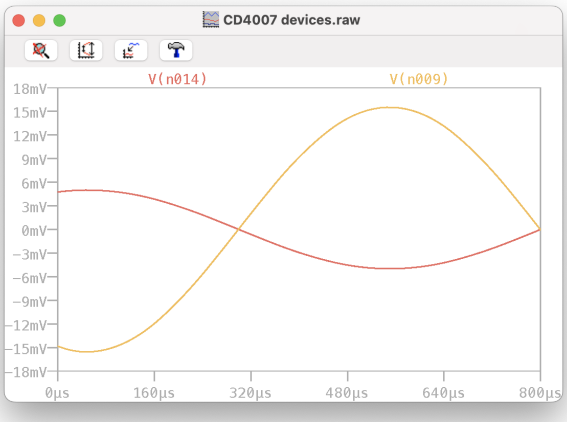

Figure 14: Input vs. output signal.

NMOS Source Follower

DC Operating Point Analysis

Using the PMOS common-source amplifier, a simplified model of which is seen in *Figure 15*, allows for characteristic calculations of the circuit and transistor to be completed. A NMOS transistor, such as the CD4007 can be used.

NMOS Source Follower

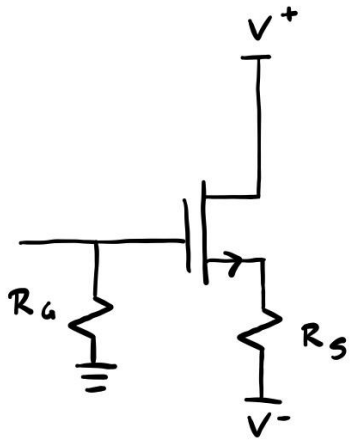

Figure 15: Simplified NMOS source follower.

The DC current going through R_g can be found to equal ~0A. As seen in the NMOS common-source amplifier, this transistor has an overdrive voltage of 2.88V.

$$V_{OV} = V_{GS} - V_{tn}$$

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{tn})^2 \text{ such that}$$

$$v_{GS} = \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}} + V_{tn}$$

$$V_{OV} = \sqrt{\frac{2I_D}{k_n' \frac{W}{L}}} + V_{tn} - V_{tn} = \sqrt{\frac{2I_D}{\mu_n \frac{\epsilon_{ox}}{t_{ox}} \frac{W}{L}}} = 2.88V$$

With a required I_D of 1mA, this means that $R_S = 2.88k\Omega$.

AC Analysis

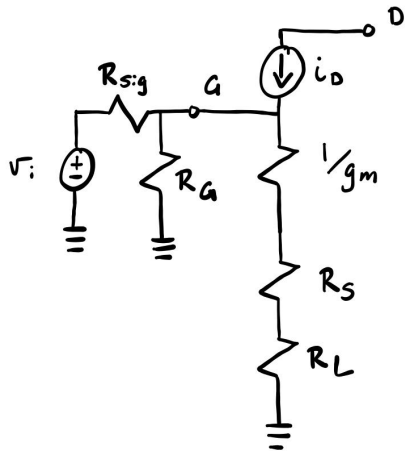

Figure 16: NMOS source follower small-signal model.

From this model, we can find that the ratio between the output and input signals can be simplified as follows:

$$v_i = v_{sig} \text{ such that } \frac{v_i}{v_{sig}} = 1$$

$$A_v = \frac{V_o}{V_i} = \frac{(R_L+R_S)}{(R_L+R_S)+1/g_m}$$

$$g_m = \frac{2I_D}{V_{OV}} = 694.4\mu S$$

$$A_v = \frac{(R_L+R_S)}{(R_L+R_S)+1.44k\Omega}$$

$$R_o = \frac{1}{g_m} = 1.44k\Omega$$

From these equations, we can see that (R_L ||R_S) must be at least 5.67kΩ, therefore, $R_L = R_S = 11.34k\Omega$.

Simulation

Simulating this circuit with capacitances of 47μF and the resistance values found above provides the following outputs in *Figure 17, Figure 18,* and *Figure 19*. The DC values are seen in *Figure 20*.

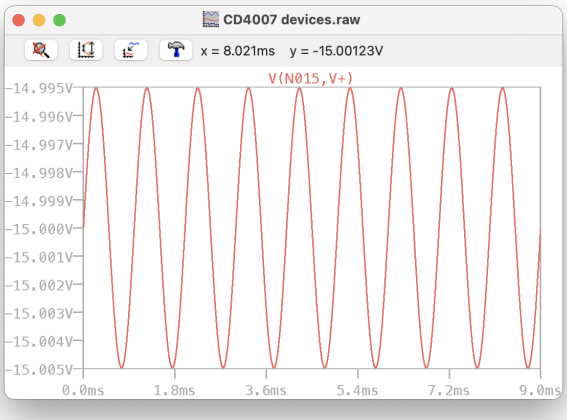

Figure 17: V_{GS}

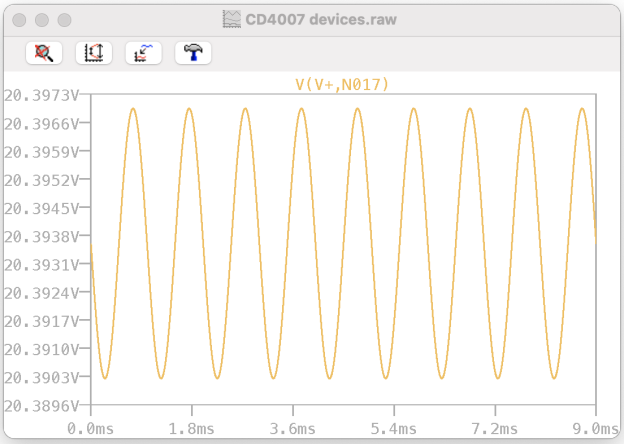

Figure 18: V_{DS}

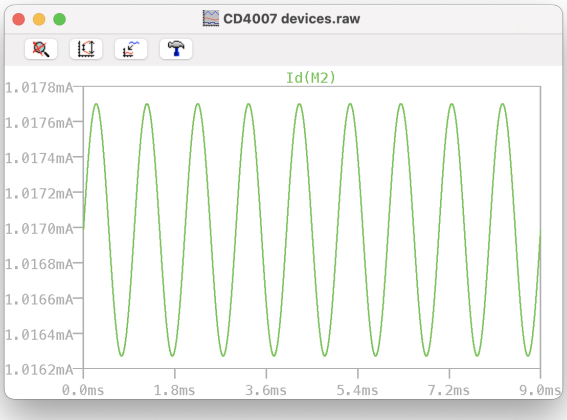

Figure 19: I_D.

V_{GS}	~15.0V
V_{DS}	~20.39V
I_D	~1.02mA

Figure 13: DC values of measurements.

These values seem to be consistent with the calculations, when it is taken into account that, because of the more complex model of a real transistor, there are some small variations. Finally, in *Figure 14* we can see the input and output signals. The observed output is closer to -0.68 V/V rather than -0.8 V/V.

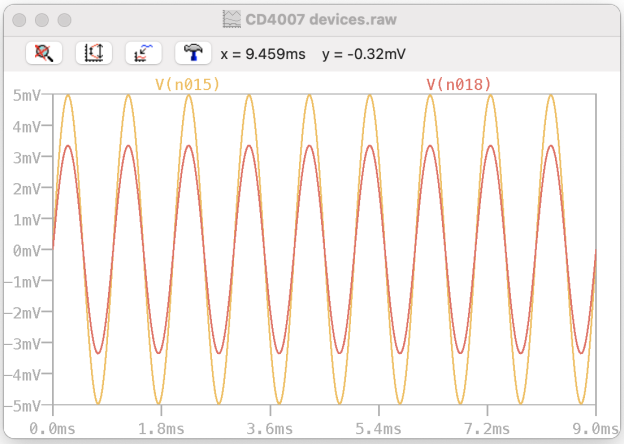

Figure 20: Input vs. output signal.