IC Lab Formal Verification Bonus Report 2024 Fall

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(a) What is Formal verification?
What's the difference between **Formal** and **Pattern** based verification?
And list the pros and cons for each.

Ans: Formal verification 是一種用來驗證電路功能性或是其他指標的方法，Formal verification 會使用窮舉法去進行驗證，較費時但可靠性較高。Pattern based verification 則是採用隨機變數的方式去驗證，驗證的速度較快但可靠性不高，可能會有 Corner case 測不到的問題。

(b) Explain SVA (SystemVerilog Assertions) and the roles of Assertion, Cover, and Assumption.
What is glue logic?
Why will we use **glue logic** to simplify our SVA expression?

Ans: SVA: 一種用來描述 property 的語言
Assertion: 根據 property 而制定的設計規範
Cover: 檢查特定的變數組合是否出現特定的次數
Assumption: 設定特定的條件，讓 tool 只去檢查條件為真的狀況

Glue logic 提供額外的語法去追蹤事件，讓 designer 可以用更簡潔的 code style 去描述 property。

(c) What is the difference between **Functional coverage** and **Code coverage**?
What's the meaning of 100% code coverage, could we claim that our assertion is well enough for verification? Why?

Ans: Functional coverage:用於檢查電路的 functionality，須由 designer 去設定特定的條件
Code coverage: 通常由 tool 自動生成，用來檢查程式碼中有被實際執行到的比例

Code coverage 100%只有確保程式碼中的每一行都是有用的，但不代表其執行結果為正確

(d) What is the difference between **COI coverage** and **proof coverage** for realizing checker's completeness? Try to explain from the meaning, relationship, and tool effort perspective.

Ans: COI coverage 會檢查所有可能跟 Assertion 有關的 cover items，而 proof coverage 會找出實際上與 Assertion 有關的 cover items，因此 proof coverage 是 COI coverage 的子集合，且 proof coverage 需要執行 formal 但 COI coverage 不需要，故 proof coverage 所需的成本較高

(e) What are the roles of **ABVIP** and **scoreboard** separately?
Try to explain the definition, objective, and the benefit.

Ans: ABVIP: Assertion Based Verification Intellectual Properties，常用於 protocol 的檢查因為在檢查 protocol 需要大量的 Assertion，而這些 Assertion 可以拿來重複使用，於是就產生了 ABVIP 讓 designer 可以加速進行 protocol 之驗證
scoreboard: 類似一個 monitor，可以即時檢查輸入輸出的結果是否正確，加速 designer 進行電路驗證

(f) Among the JasperGold tools (Formal Verification, SuperLint, Jasper CDC, IMC Coverage), which one do you think is the most effective based on its functionality and typical application scenarios? Please explain your reasoning by describing a hypothetical scenario where this tool would be particularly beneficial, and discuss any potential challenges or limitations that might arise when using it.

Ans: 我覺得在實際應用面來說 Jasper CDC 是實用的，因為大部分電路系統都需要 Memory 來儲存資料，而記憶體的讀取速度通常又都是系統的效能 bottlemeck，這時使用 CDC 來控制不同速度的元件才能達到整個系統的最高效率，CDC 作為每個元件中溝通的橋樑，其功能的正確性就至關重要。在驗證 CDC 時的難點在於每一個 protocol 的 SPEC 都需要驗證清楚，否則可能會造成資料傳輸的錯誤。