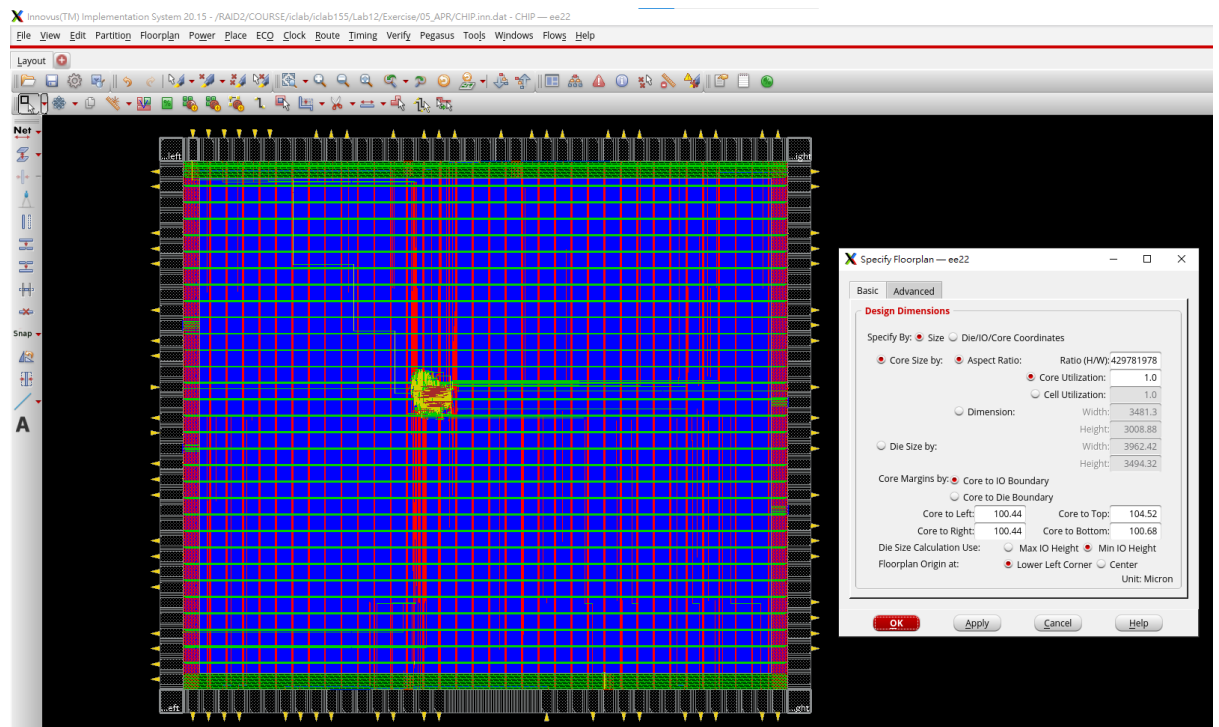
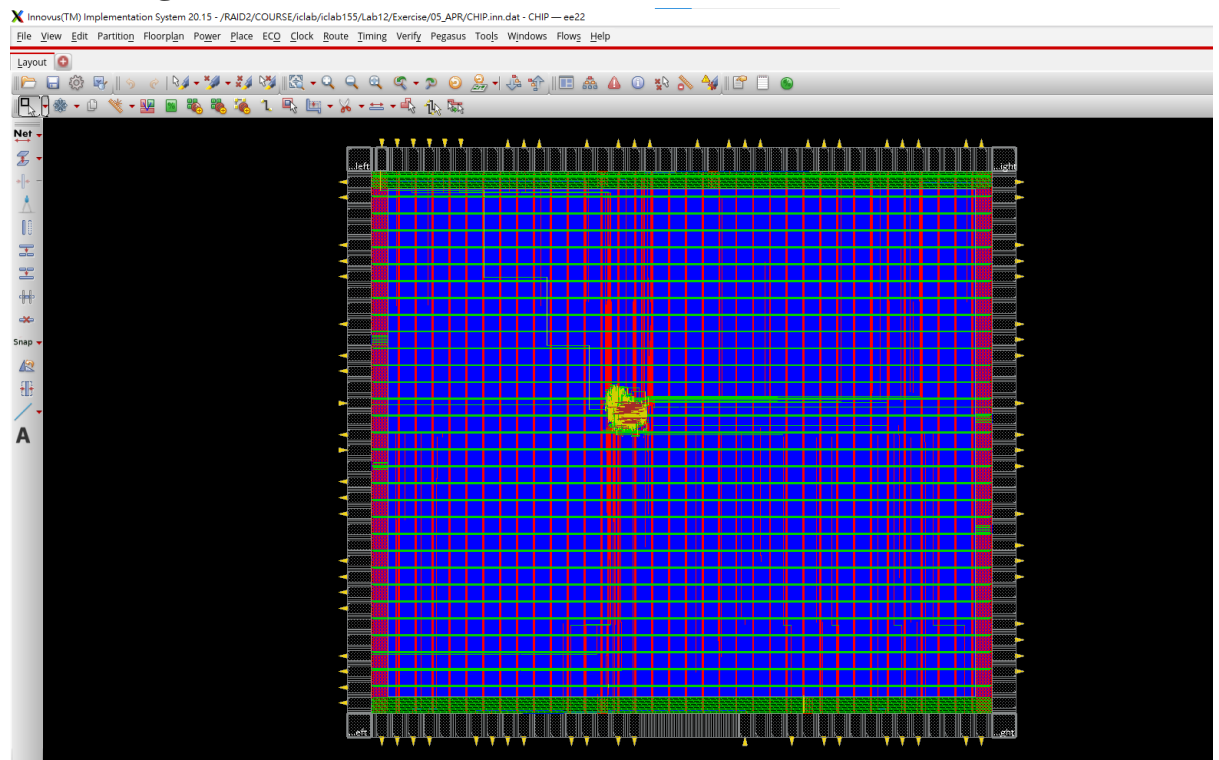


# Report

## 1. Core to IO boundary :



## 2. Core Ring :





```

ee22.siz.lee.nyu.edu.tw (iclab155)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
# Design Name: CHIP
# Design Mode: 180nm
# Analysis Mode: MMCM OCY
# Parasitics Mode: SPEF/RCDB
# Signoff Settings: SI On
*****
AAE INFO: 1 threads acquired from CTE.
Start delay calculation (fullDC) (1 T). (MEM=2999.34)
*** Calculating scaling factor for lib_min libraries using the default operating condition of each library.
Total number of fetched objects 1421
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 1372, 100.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=3043.38 CPU=0:00:00.4 REAL=0:00:00.0)
Loading CTE timing window with TwFlowType 0... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 3043.4M)
Add other clocks and setupCteToAAEClockMapping during iter 1
Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 3043.4M)
Starting SI iteration 2
Start delay calculation (fullDC) (1 T). (MEM=3007.5)
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0.
Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 1421.
Total number of fetched objects 1421
AAE INFO: Total number of nets for which stage creation was skipped for all views 0
AAE INFO-618: Total number of nets in the design is 1372, 0.0 percent of the nets selected for SI analysis
End delay calculation. (MEM=3046.66 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=3046.66 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.7 real=0:00:00.0 totSessionCpu=0:04:45 mem=3046.7M)

-----
timeDesign Summary
-----

Hold views included:
av_func_mode_min

+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
| WNS (ns) | 0.234 | 0.234 | 19.726 |
| TNS (ns) | 0.000 | 0.000 | 0.000 |
| Violating Paths: | 0 | 0 | 0 |
| All Paths: | 595 | 247 | 366 |
+-----+-----+-----+-----+

Density: 0.393%
(126.759% with Fillers)
-----
Reported timing to dir timingReports
Total CPU time: 1.14 sec
Total Real time: 2.0 sec
Total Memory Usage: 2978.929688 Mbytes
Reset AAE Options
*** timeDesign #7 [finish] : cpu/real = 0:00:01.1/0:00:01.5 (0.7), totSession cpu/real = 0:04:45.2/0:38:42.8 (0.1), mem = 2978.9M

```

## 5. DRC result :

```

ee22.siz.lee.nyu.edu.tw (iclab155)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
VERIFY DRC ..... Sub-Area: {2453.760 2956.800 2726.400 3225.600} 164 of 182
VERIFY DRC ..... Sub-Area: {164 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2726.400 2956.800 2999.040 3225.600} 165 of 182
VERIFY DRC ..... Sub-Area: {165 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2999.040 2956.800 3271.680 3225.600} 166 of 182
VERIFY DRC ..... Sub-Area: {166 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3271.680 2956.800 3544.320 3225.600} 167 of 182
VERIFY DRC ..... Sub-Area: {167 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3544.320 2956.800 3775.180 3225.600} 168 of 182
VERIFY DRC ..... Sub-Area: {168 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {0.000 3225.600 272.640 3494.320} 169 of 182
VERIFY DRC ..... Sub-Area: {169 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {272.640 3225.600 545.280 3494.320} 170 of 182
VERIFY DRC ..... Sub-Area: {170 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {545.280 3225.600 817.920 3494.320} 171 of 182
VERIFY DRC ..... Sub-Area: {171 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {817.920 3225.600 1090.560 3494.320} 172 of 182
VERIFY DRC ..... Sub-Area: {172 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1090.560 3225.600 1363.200 3494.320} 173 of 182
VERIFY DRC ..... Sub-Area: {173 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1363.200 3225.600 1635.840 3494.320} 174 of 182
VERIFY DRC ..... Sub-Area: {1635.840 3225.600 1908.480 3494.320} 175 of 182
VERIFY DRC ..... Sub-Area: {175 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {1908.480 3225.600 2181.120 3494.320} 176 of 182
VERIFY DRC ..... Sub-Area: {176 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2181.120 3225.600 2453.760 3494.320} 177 of 182
VERIFY DRC ..... Sub-Area: {177 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2453.760 3225.600 2726.400 3494.320} 178 of 182
VERIFY DRC ..... Sub-Area: {178 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2726.400 3225.600 2999.040 3494.320} 179 of 182
VERIFY DRC ..... Sub-Area: {179 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2999.040 3225.600 3271.680 3494.320} 180 of 182
VERIFY DRC ..... Sub-Area: {180 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3271.680 3225.600 3544.320 3494.320} 181 of 182
VERIFY DRC ..... Sub-Area: {181 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3544.320 3225.600 3775.180 3494.320} 182 of 182
VERIFY DRC ..... Sub-Area: {182 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.8 ELAPSED TIME: 1.00 MEM: 0.0M) ***

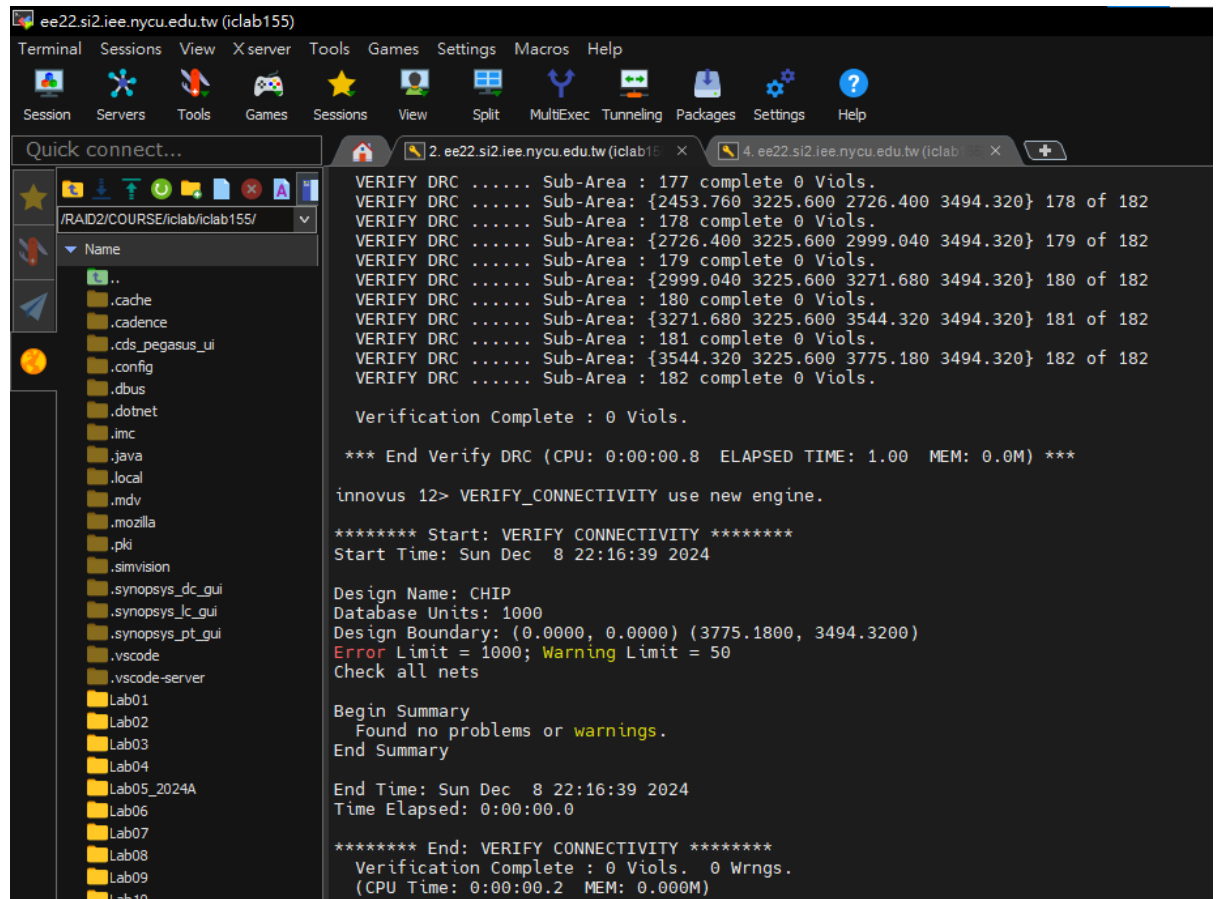
innovus 12> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sun Dec 8 22:16:39 2024

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (3775.1800, 3494.3200)
Error Limit = 1000; Warning Limit = 50
Check all nets

```

## 6. LVS result :



```
ee22.si2.iee.nycu.edu.tw (iclab155)
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...
/RAID2/COURSE/iclab/iclab155/
Name
.cache
.cadence
.cds_pegasus_ui
.config
.dbus
.dotnet
.imc
.java
.local
.mdv
.mozilla
.plk
.simvision
.synopsys_dc_gui
.synopsys_ic_gui
.synopsys_pt_gui
.vscode
.vscode-server
Lab01
Lab02
Lab03
Lab04
Lab05_2024A
Lab06
Lab07
Lab08
Lab09
Lab10

VERIFY DRC ..... Sub-Area : 177 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2453.760 3225.600 2726.400 3494.320} 178 of 182
VERIFY DRC ..... Sub-Area : 178 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2726.400 3225.600 2999.040 3494.320} 179 of 182
VERIFY DRC ..... Sub-Area : 179 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {2999.040 3225.600 3271.680 3494.320} 180 of 182
VERIFY DRC ..... Sub-Area : 180 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3271.680 3225.600 3544.320 3494.320} 181 of 182
VERIFY DRC ..... Sub-Area : 181 complete 0 Viols.
VERIFY DRC ..... Sub-Area: {3544.320 3225.600 3775.180 3494.320} 182 of 182
VERIFY DRC ..... Sub-Area : 182 complete 0 Viols.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.8 ELAPSED TIME: 1.00 MEM: 0.0M) ***

innovus 12> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Sun Dec 8 22:16:39 2024

Design Name: CHIP
Database Units: 1000
Design Boundary: (0.0000, 0.0000) (3775.1800, 3494.3200)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
Found no problems or warnings.
End Summary

End Time: Sun Dec 8 22:16:39 2024
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.2 MEM: 0.000M)
```

## 7. Post Layout simulation result :

ee22.si2.tee.nycu.edu.tw (iclab155)

Terminal Sessions View X server Tools Games Settings Macros Help

Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help

Quick connect...

/RAID2/COURSE/iclab/iclab155/

Name

- ..
- .cache
- .cadence
- .cds\_pegasus\_ui
- .config
- .dbus
- .dotnet
- .imc
- .java
- .local
- .mdv
- .mozilla
- .pki
- .simvision
- .synopsys\_dc\_gui
- .synopsys\_ic\_gui
- .synopsys\_pt\_gui
- .vscode
- .vscode-server
- Lab01
- Lab02
- Lab03
- Lab04
- Lab05\_2024A
- Lab06
- Lab07
- Lab08
- Lab09
- Lab10
- Lab11
- Lab12
- Midterm\_Project
- OT
- .bash\_logout
- .bash\_profile
- .bashrc
- .flexlmrc
- .history
- .kshrc
- .viminfo
- .Xauthority

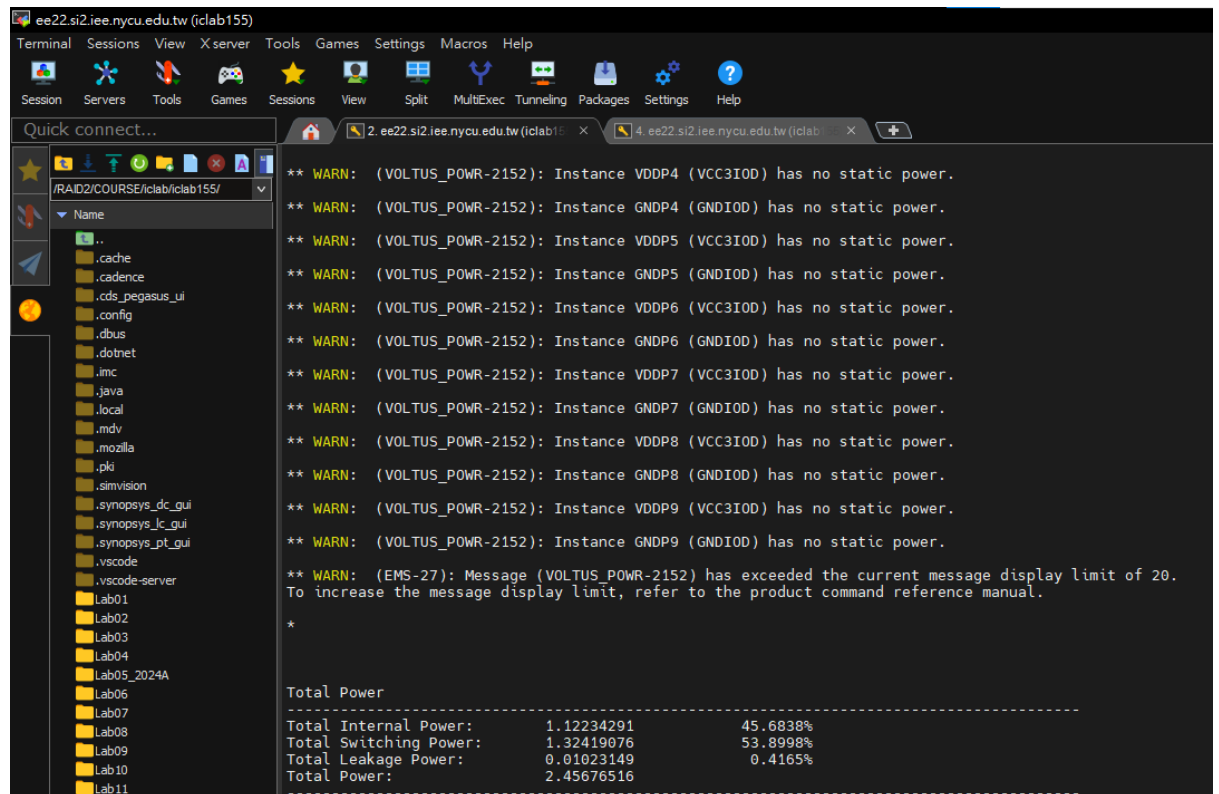
No. 954 PASS  
No. 955 PASS  
No. 956 PASS  
No. 957 PASS  
No. 958 PASS  
No. 959 PASS  
No. 960 PASS  
No. 961 PASS  
No. 962 PASS  
No. 963 PASS  
No. 964 PASS  
No. 965 PASS  
No. 966 PASS  
No. 967 PASS  
No. 968 PASS  
No. 969 PASS  
No. 970 PASS  
No. 971 PASS  
No. 972 PASS  
No. 973 PASS  
No. 974 PASS  
No. 975 PASS  
No. 976 PASS  
No. 977 PASS  
No. 978 PASS  
No. 979 PASS  
No. 980 PASS  
No. 981 PASS  
No. 982 PASS  
No. 983 PASS  
No. 984 PASS  
No. 985 PASS  
No. 986 PASS  
No. 987 PASS  
No. 988 PASS  
No. 989 PASS  
No. 990 PASS  
No. 991 PASS  
No. 992 PASS  
No. 993 PASS  
No. 994 PASS  
No. 995 PASS  
No. 996 PASS  
No. 997 PASS  
No. 998 PASS  
No. 999 PASS

\*\*\*\*\*  
Congratulations!  
execution cycles = 84824  
clock period = 40.000000ns  
\*\*\*\*\*  
\$finish called from file "PATTERN.v", line 26.  
\$finish at simulation time 4461420000  
V C S Simulation Report  
Time: 4461420000 ps  
CPU Time: 6.790 seconds; Data structure size: 0.6Mb  
Sun Dec 8 22:57:35 2024  
CPU time: 6.844 seconds in simulation  
22:57 iclab155@ee22[~/Lab12/Exercise/06\_POST]\$

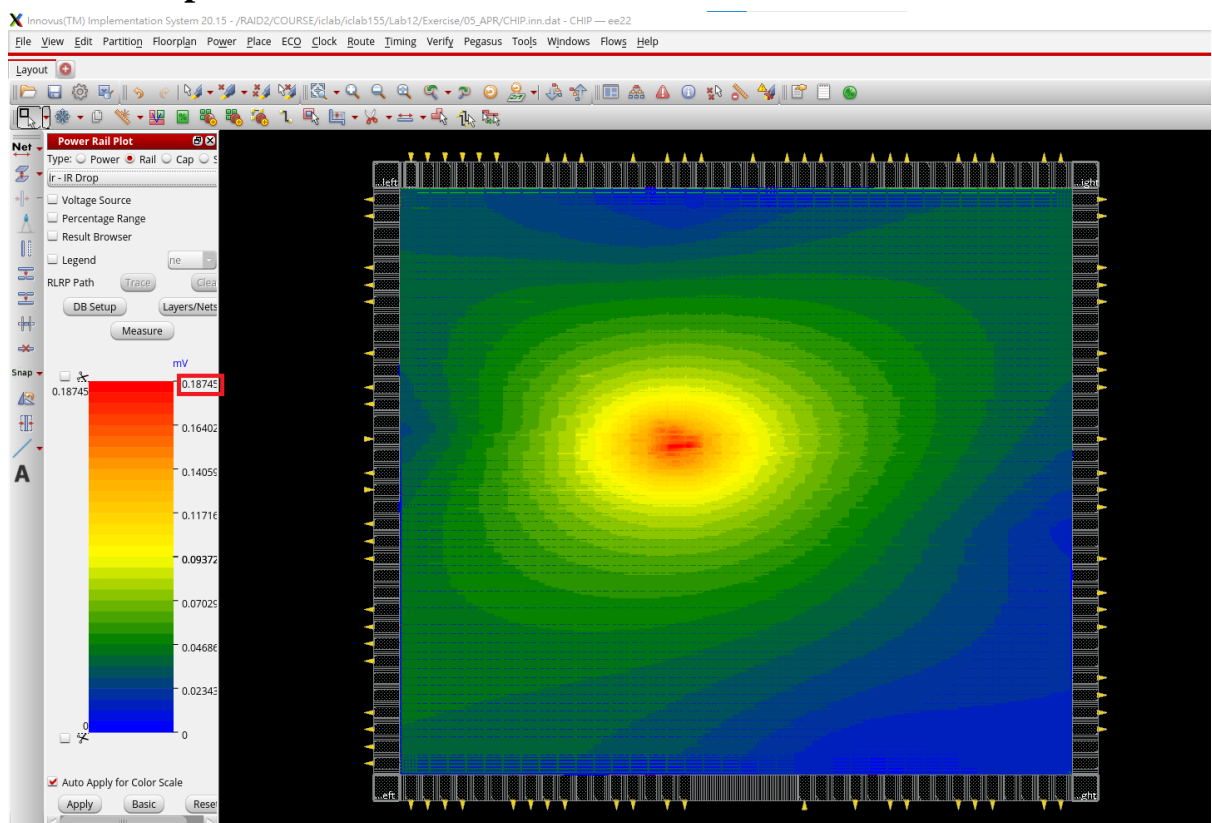
Remote monitoring  
☐ Follow terminal folder



## 8. Power result :



## 9. IR Drop Results :



我把utilization設定成0.7，並把4組的core power pad 盡量往中間擺，讓core裡的點到power pad的距離都不會太遠，最後的結果大約落在0.187mv左右。