AXI DMA - Test Plan

Test ID	Feature	Test Name	Description	Input Stimulus	Expected	Checking Procedure	Status	Comments/Screenshots
1	**Reset**	reset_test	When reset is asserted, the DMA Core is resetted and no read or write operation can happen unless configured.	Apply clock; axi_resetn = 0;	DMA core should reset.	From the Waveform. There should be no read/write activity across all channels.	Pass	
Independent Operation								
2	**MM2S Enable**	mm2s_enable_test	Enables the Memory Mapped to Stream Read Operation. The dut will start reading from the provided base address and streams the data on the AXI-Stream Interface.	Configure the DMA's internal registers as following: 1. MM2S_DMACR = 32'h11003 2. MM2S_SA = 32'h0 3. MM2S_LENGTH = 32'h80			In Progress	
3	**S2MM Enable**	s2mm_enable_test	Enables the Stream to Memory Mapped Write Operation. The dut will take stream as input and start writing on the provided base address via AXI-4 Interface.	Configure the DMA's internal registers as following: 1. S2MM_DMACR = 32'h11003 2. S2MM_DA = 32'h0 3. S2MM_LENGTH = 32'h80			In Progress	
4 KB Boundary Protection								
4	**4 KB Boundary Protection**	boundary_test	The AXI DMA should provide 4 KB address boundary protection (when configured in non-Micro DMA).				Not Started	
Data Re-Alignment								
5	**Data Re-Alignment**	data_alignment_test	AXI DMA provides byte-level data realignment allowing memory reads and writes starting at any byte offset location.					
AXI4 DATA WIDTHS								
6	**32 bits**	axi_32_test	AXI DMA has primary AXI4 data width support of 32, 64, 128, 256, 512, and, 1,024 bits				Not Started	
7	**64 bits**	axi_64_test					Not Started	
8	**128 bits**	axi_128_test					Not Started	
9	**256 bits**	axi_256_test					Not Started	
10	**512 bits**	axi_512_test					Not Started	
11	**1024 bits**	axi_1024_test					Not Started	
AXI-Stream DATA WIDTHS								
12	**8 bits**	axis_8_test	AXI DMA has primary AXI4-Stream data width support of 8, 16, 32, 64, 128, 256, 512, and, 1,024 bits				Not Started	
13	**16 bits**	axis_16_test					Not Started	
14	**32 bits**	axis_32_test					Not Started	
15	**64 bits**	axis_64_test					Not Started	
16	**128 bits**	axis_128_test					Not Started	
17	**256 bits**	axis_256_test					Not Started	
18	**512 bits**	axis_512_test					Not Started	
19	**1024 bits**	axis_1024_test					Not Started	
Interrupt on Completion (IOC)								
20	**Read Interrupt**	read_interrupt_test	DMA asserts **mm2s_introut** signal at the end of a read transfer when the IOC_IrqEn bit is set/enabled in MM2S_DMACR register.				Pass	
21	**Write Interrupt**	write_interrupt_test	DMA asserts **s2mm_introut** signal to indicate the end of a write transfer when the IOC_IrqEn bit is set/enabled in S2MM_DMACR register.				Pass	
Register Bits								
22	**Run/Stop Bits**	rs_test	Run/Stop control for controlling running and stopping of the DMA channel. 0 = Stop; 1 = Run **Note:** For Direct Register mode pending commands/transfers are flushed or completed. AXI4-Stream outs are potentially terminated.				Not Started	
23	**Soft Reset**	soft_reset	Setting either MM2S_DMACR.Reset = 1 or S2MM_DMACR. Reset = 1 resets the entire AXI DMA engine. After completion of a soft reset, all registers and bits are in the Reset State. • 0 = Normal operation. • 1 = Reset in progress.				Not Started	
Interrupt on Error								
24	**Read Error**	read_error_test	DMA asserts **mm2s_introut** signal to indicate read error when the Err_IrqEn bit is set/enabled in MM2S_DMACR register.				Not Started	
25	**Write Error**	write_error_test	DMA asserts **s2mm_introut** signal to indicate write error when the Err_IrqEn bit is set/enabled in S2MM_DMACR register.				Not Started	
Halted Bit								
26	**Halted**	halted_test	When halted, writing to the LENGTH register has no effect on DMA operations. • 0 = DMA Channel Running • 1 = DMA Channel Halted				Not Started	
Idle Bit								
27	**Idle**	idle_test	Indicates the state of AXI DMA operations. • 0 = Not Idle (Transfer not Complete) • 1 = Idle (Transfer is Complete)				Not Started	
Error bits								
28	**Slave Error**	slave_error_test	This error occurs if the slave read from the Memory Map interface issues a Slave Error. • 0 = No Slave Error • 1 = Slave Error Detected				Not Started	
29	**Decode Error**	decode_error_test	This error occurs if the address request points to an invalid address. • 0 = No Decode Error • 1 = Decode Error Detected				Not Started	
64-bit Addressing								
30	**MM2S_SA_MSB**	sa_msb_test	DMA Supports a 64-bit source address when it's configured for a 64-bit address space.				Not Started	
31	**MM2S_SA_MSB**	da_msb_test	DMA Supports a 64-bit destination address when it's configured for a 64-bit address space.				Not Started	
Length Register								
32	**MM2S_LENGTH**	mm2s_length_test	Indicates the number of bytes to transfer for the MM2S channel. Writing a non-zero value to this register starts the MM2S transfer.				Not Started	
33	**S2MM_LENGTH**	s2mm_length_test	Indicates the number of bytes to transfer for the S2MM channel. Writing a non-zero value to this register starts the S2MM transfer. **Note:** S2MM_LENGTH >= Largest Packet Received on AXI4-Stream				Not Started	