

Module: R4: Computer Architecture**Section: Pipelining & Hazards Task: Pipelining & Hazards****Task****Pipelining & Hazards****➤ Question 1:****a. Average CPI:*****For Version A:***

$$CPI_{avg} = (\%age_A \times CPI_A) + (\%age_B \times CPI_B) + (\%age_C \times CPI_C) + (\%age_D \times CPI_D)$$

$$CPI_{avg} = (2 \times 0.4) + (3 \times 0.25) + (3 \times 0.25) + (7 \times 0.1) = 3$$

For Version B:

$$CPI_{avg} = (\%age_A \times CPI_A) + (\%age_B \times CPI_B) + (\%age_C \times CPI_C) + (\%age_D \times CPI_D) + (\%age_E \times CPI_E) + (\%age_F \times CPI_F) + (\%age_G \times CPI_G)$$

$$CPI_{avg} = (2 \times 0.15) + (2 \times 0.15) + (4 \times 0.1) + (6 \times 0.1) + (1 \times 0.1) + (2 \times 0.2) + (2 \times 0.2) = 2.5$$

b. MIPS:***For Version A:***

$$MIPS = \frac{frequency}{CPI \times 10^6}$$

$$MIPS = \frac{600 \times 10^6}{3 \times 10^6} = 200 \text{ MIPS}$$

For Version B:

$$MIPS = \frac{frequency}{CPI \times 10^6}$$

$$MIPS = \frac{700 \times 10^6}{2.5 \times 10^6} = 280 \text{ MIPS}$$

c. Design Choice:

Processor B with 700 MHz and 280 MIPS is better than processor A with 600 MHz and 200 MIPS.

Here's why:

- **Clock Speed:** Processor B has a higher clock speed (700 MHz) compared to Processor A (600 MHz). This means that process B can execute more cycles per second, which generally leads to better performance.
- **MIPS:** Processor B also has a higher MIPS (Million Instructions Per Second) value (280 MIPS) compared to Processor A (200 MIPS). This means that the Processor B can theoretically execute more instructions per second, which can lead to better performance.

➤ Question 2:**a. Non-Pipelined Machine:**

It takes a total of 48 cycles as shown by the table below:

Non-pipelined Machine																																																														
	Cycles	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48													
0	MUL R3 , R1 , R2	F	D	E	E	E	E	E	E	W																																																				
1	ADD R5 , R4 , R3									F	D	E	E	E	E	W																																														
2	ADD R6 , R4 , R1																F	D	E	E	E	E	W																																							
3	MUL R7 , R8 , R9																									F	D	E	E	E	E	E	E	W																												
4	ADD R4 , R3 , R7																																			F	D	E	E	E	E	W																				
5	MUL R10 , R5 , R6																																																						F	D	E	E	E	E	E	W

b. A pipelined machine with five adders and five multipliers without data forwarding:

It takes a total of 28 cycles as shown by the table below:

A pipelined machine with five adders and five multipliers without data forwarding																													
	Cycles	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
0	MUL R3 , R1 , R2	F	D	E1	E2	E3	E4	E5	E6	W																			
1	ADD R5 , R4 , R3		F	D	-	-	-	-	-	-	D	E1	E2	E3	E4	W													
2	ADD R6 , R4 , R1			F	-	-	-	-	-	-	D	E1	E2	E3	E4	W													
3	MUL R7 , R8 , R9										F	D	E1	E2	E3	E4	E5	E6	W										
4	ADD R4 , R3 , R7											F	D	-	-	-	-	-	-	D	E1	E2	E3	E4	W				
5	MUL R10 , R5 , R6																			F	D	E1	E2	E3	E4	E5	E6	W	

c. A pipelined machine with five adders and five multipliers with data forwarding:

It takes a total of 26 cycles as shown by the table below:

A pipelined machine with five adders and five multipliers with data forwarding																											
	Cycles	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
0	MUL R3 , R1 , R2	F	D	E1	E2	E3	E4	E5	E6	W																	
1	ADD R5 , R4 , R3		F	D	-	-	-	-	-	E1	E2	E3	E4	W													
2	ADD R6 , R4 , R1			F	-	-	-	-	-	D	E1	E2	E3	E4	W												
3	MUL R7 , R8 , R9										F	D	E1	E2	E3	E4	E5	E6	W								
4	ADD R4 , R3 , R7											F	D	-	-	-	-	-	E1	E2	E3	E4	W				
5	MUL R10 , R5 , R6												F	-	-	-	-	-	-	D	E1	E2	E3	E4	E5	E6	W

d. A pipelined machine with one adder and one multipliers without data forwarding:

It takes a total of 32 cycles as shown by the table below:

A pipelined machine with one adder and one multiplier without data forwarding																																	
	Cycles	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0	MUL R3 , R1 , R2	F	D	E1	E2	E3	E4	E5	E6	W																							
1	ADD R5 , R4 , R3		F	D	-	-	-	-	-	D	E1	E2	E3	E4	W																		
2	ADD R6 , R4 , R1			F	-	-	-	-	-	D	-	-	-	E1	E2	E3	E4	W															

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