

**Module: R4: Computer Architecture**  
**Section: Caches Task: Memory Accesses**

## Task 2

### Memory Accesses

### Scenario 3

#### 1. Program Parameters:

```

22 #####
23 # You MAY change the code below this section
24 main:  li a0, 128    # array size in BYTES (power of 2 < array size)
25        li a1, 1      # step size  (power of 2 > 0)
26        li a2, 1      # rep count  (int > 0)
27        li a3, 0      # 0 - option 0, 1 - option 1
28 # You MAY change the code above this section

```

#### 2. L1 Cache Parameters:

Registers   Memory <b>Cache</b> VDB	
Cache Levels	2
Block Size (Bytes)	8
Number of Blocks	8
Associativity	1
Cache Size (Bytes)	64
Enable?	Enables current selected level of the cache.
<div style="border: 1px solid black; padding: 2px; display: inline-block;">Direct Mapped <span style="float: right;">▼</span></div>	
<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="border: 1px solid black; padding: 2px; display: inline-block;">LRU <span style="float: right;">▼</span></div> <div style="border: 1px solid black; padding: 2px; display: inline-block;">L1 <span style="float: right;">▼</span></div> </div>	

#### 3. L2 Cache Parameters:

	Registers	Memory	Cache	VDB
Cache Levels	<input type="text" value="2"/>			
Block Size (Bytes)	<input type="text" value="8"/>			
Number of Blocks	<input type="text" value="16"/>			
Associativity	<input type="text" value="1"/>			
Cache Size (Bytes)	<input type="text" value="128"/>			
<input type="button" value="Enable?"/>	Enables current selected level of the cache.			
<input type="button" value="Direct Mapped"/>				
<input type="button" value="LRU"/> <input type="button" value="L2"/>				

➤ **Questions:**

**1. What is the hit rate of the L1 cache? The L2 cache? Overall?**

**Hit Rate of L1:** Hit Rate of L1 Cache is 50% (mhmhmh) i.e. 0.50 in decimals.

**Hit Rate of L2:** Hit Rate of L2 Cache is 0% (mmmmm) i.e. 0.00 in decimals.

**Overall Hit Rate:**  $0.50 + 0.00 = 0.50$  (same as L1 cache). Since all the miss accesses in L1 will also be misses in L2 cache, so overall hit rate will be the same as L1 Cache.

**2. How many accesses do we have to the L1 cache total? How many of them are misses?**

Total accesses to the L1 cache are 32 and 50% is the hit rate which means half of the 32 accesses are misses. So there are a total 16 misses in L1 cache.

**3. How many accesses do we have to the L2 cache total?**

Total accesses to the L2 cache are 16 since we'll only be accessing L2 cache when there is a miss in L1 cache. Since there are 16 misses in L1 cache, hence, the total number of accesses to L2 are 16 as well. (L2

accesses = L1 Misses)

**4. What program parameter would allow us to increase the L2 hit rate, but keep the L1 hit rate the same?**

We can improve the hit rate for L2 cache by increasing the repcount. Changing this parameter will keep the L1 hit rate the same as previously (0.50) but the hit rate for L2 cache will increase.

For example, by setting the repcount=2, the L2 hit rate increase from 0.0 to 0.50. And for repcount=4, the hit rate for L2 cache will be 0.75 while hit rate for L1 cache is still 0.50.

**5. Do our L1 and L2 hit rates decrease (-), stay the same (=), or increase (+) as we (1) increase the number of blocks in L1, or (2) increase the L1 block size?**

■ **Increasing the no. of blocks in L1**

Increasing the number of blocks in L1 cache will potentially decrease the hit rate as we have now less space in a single block to store our data, therefore the hit rate for L1 will decrease (-). While the hit rate for L2 will be the increase. (+)

■ **Increasing the size of blocks in L1**

Increasing the block size in L1 cache will also increase the hit rate as we have more space now to store our data, therefore the hit rate for L1 will improve (+). While the hit rate for L2 will be the same (=) as previous.