**Module: R5: RV-fpga**
**Section:** RISC-V VeeR Core **Task:** Final Assessment

# Final Assessment

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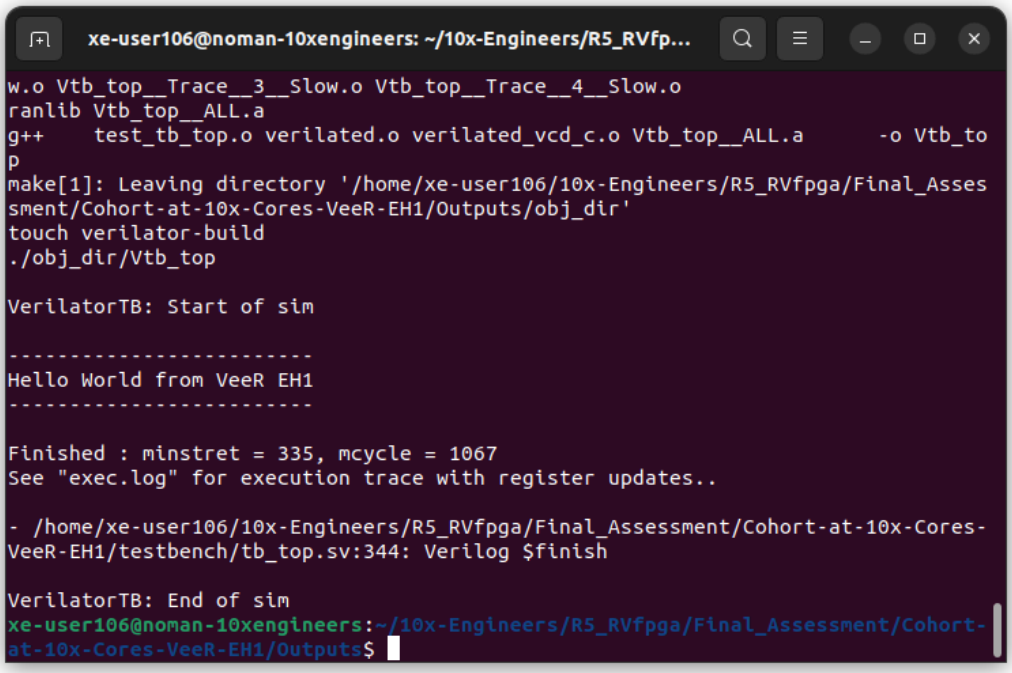
➢ **Hello World Program:**

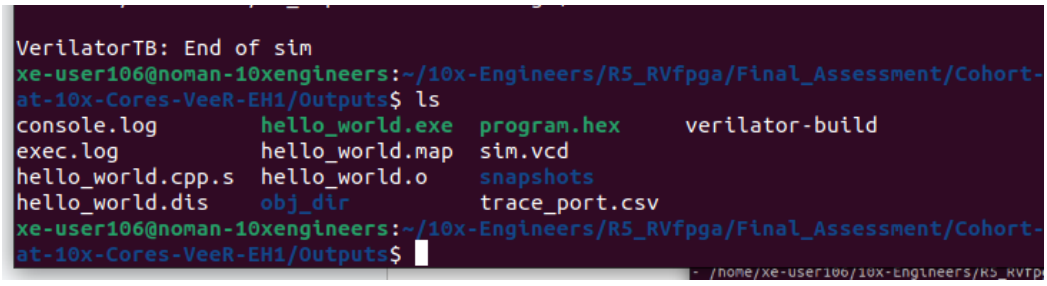
- **Command:**

```
make -f ${RV_ROOT}/tools/Makefile
```

- **Terminal Output:**




Here are the files that has been generated:




➢ **How to run an Example Test Program:**

- **Steps:**
  1. Make a directory for the generated output files. E.g.

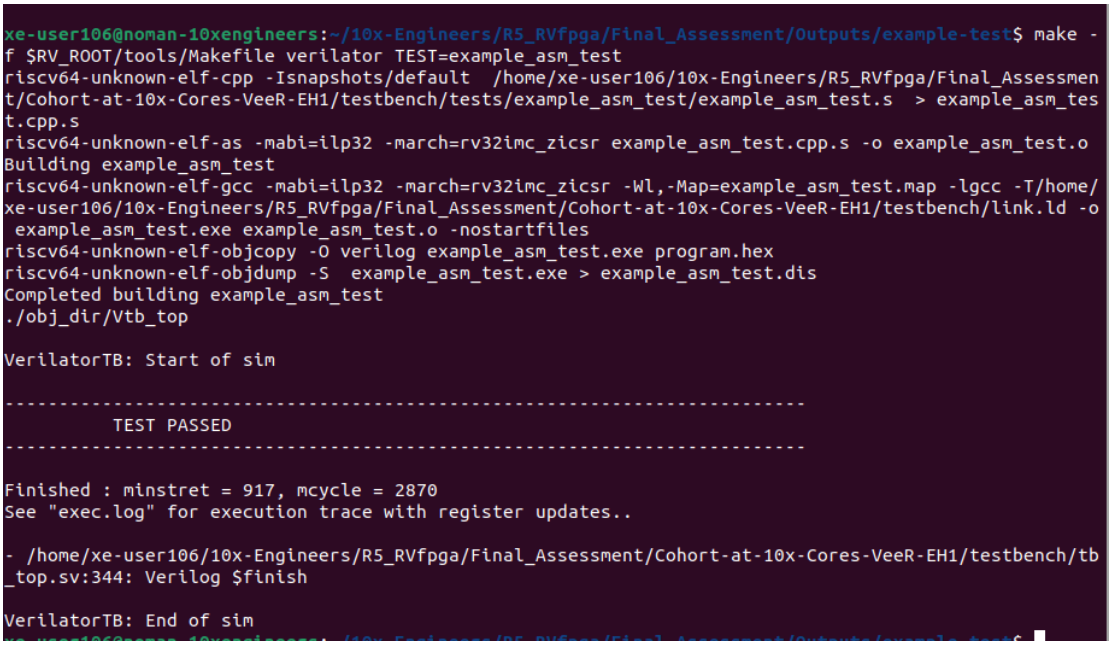
`mkdir temp`

2. Change the directory as following:
   `cd temp`

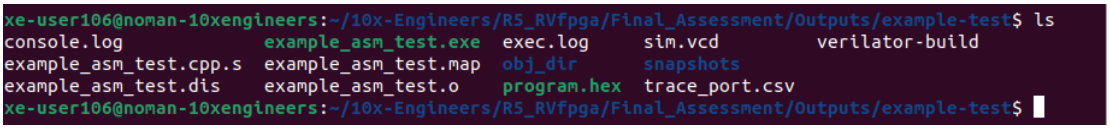
3. Use the following command to run the test example program:

```
make -f $RV_ROOT/tools/Makefile verilator TEST=example_asm_test
```

- **Terminal Output:**




Here are the files that has been generated:




- **Makefile Explanation:**
  1. **Command:**

     ```
     make -f $RV_ROOT/tools/Makefile verilator
     TEST=example_asm_test
     ```

  2. **Purpose:**
     This command runs the verilator target from the specified Makefile, while setting the TEST variable to **example_asm_test**.

  3. **Environment Check:**

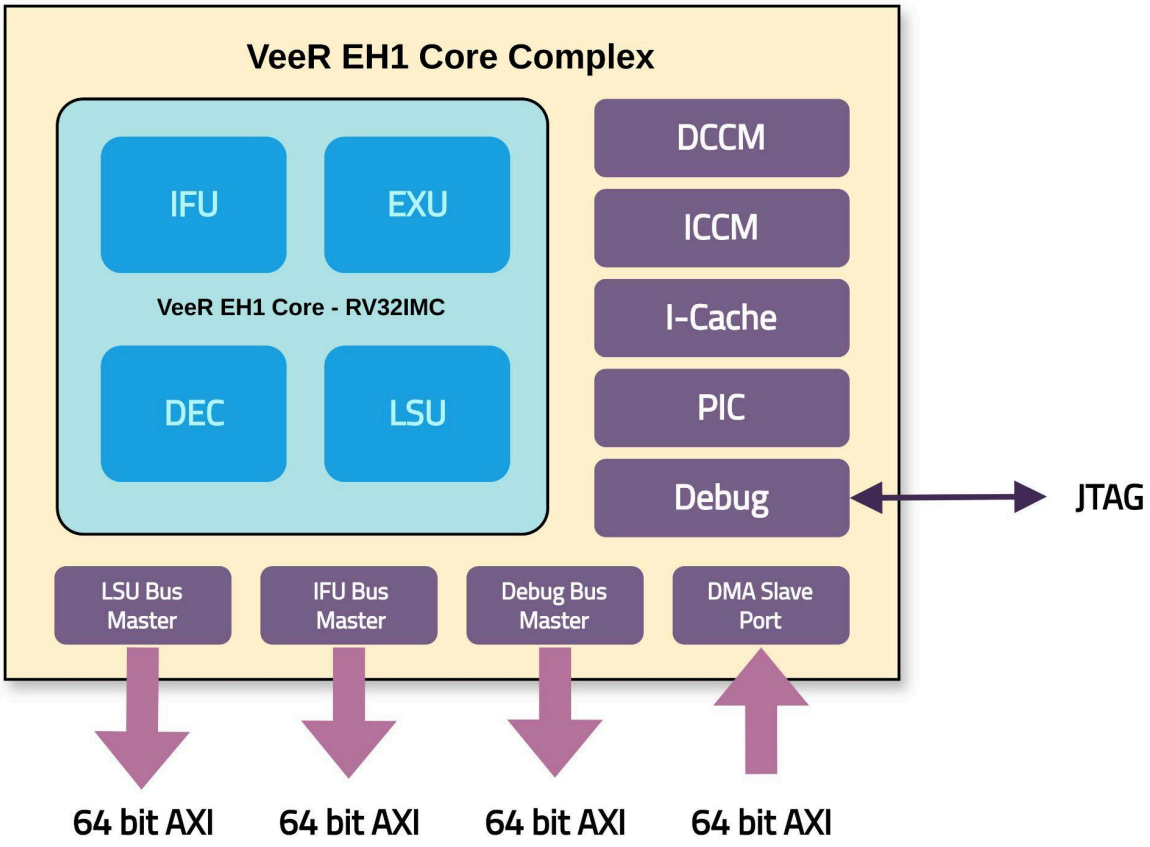
The Makefile checks if the **RV_ROOT** environment variable is set correctly. If it doesn't point to a valid directory, the process will stop with an error.

4. **Building the Test Program:**
   The Makefile will look for a RISC-V GCC toolchain (riscv64-unknown-elf-gcc). If found, it compiles the **example_asm_test** file into a hex file (**program.hex**). If the toolchain is not found, it uses a precompiled hex file instead.

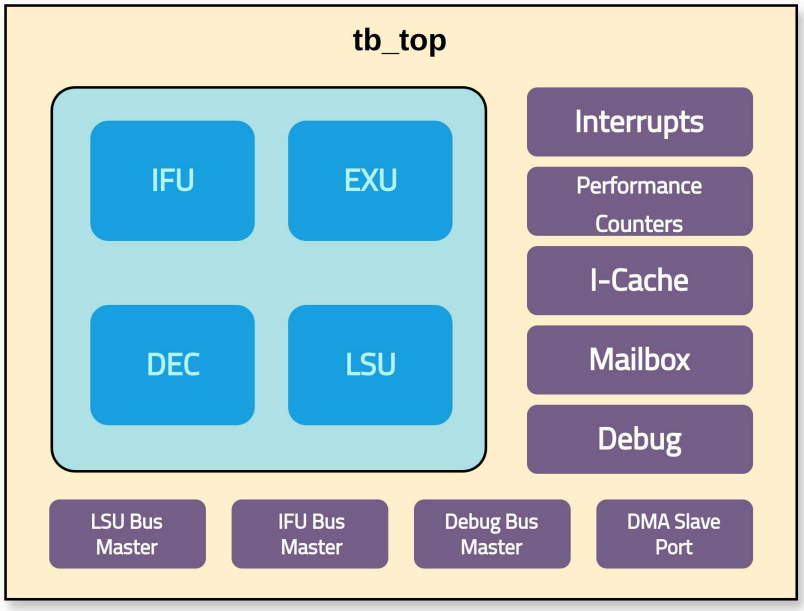
5. **Verilator Build:**
   The verilator-build target is executed, which compiles the Verilog source files using Verilator. It prepares the necessary files for simulation.

6. **Running the Simulation:**
   The verilator target is then executed. It runs the Verilator simulation with the compiled hex file (program.hex). The simulation will produce output based on the **example_asm_test program**.

➢ **Block Diagram of VeeR EH1 core complex:**




➢ **Block Diagram of Testbench Top File:**



- **Testplans:**
  The testplans can be found at the following link: TESTPLAN