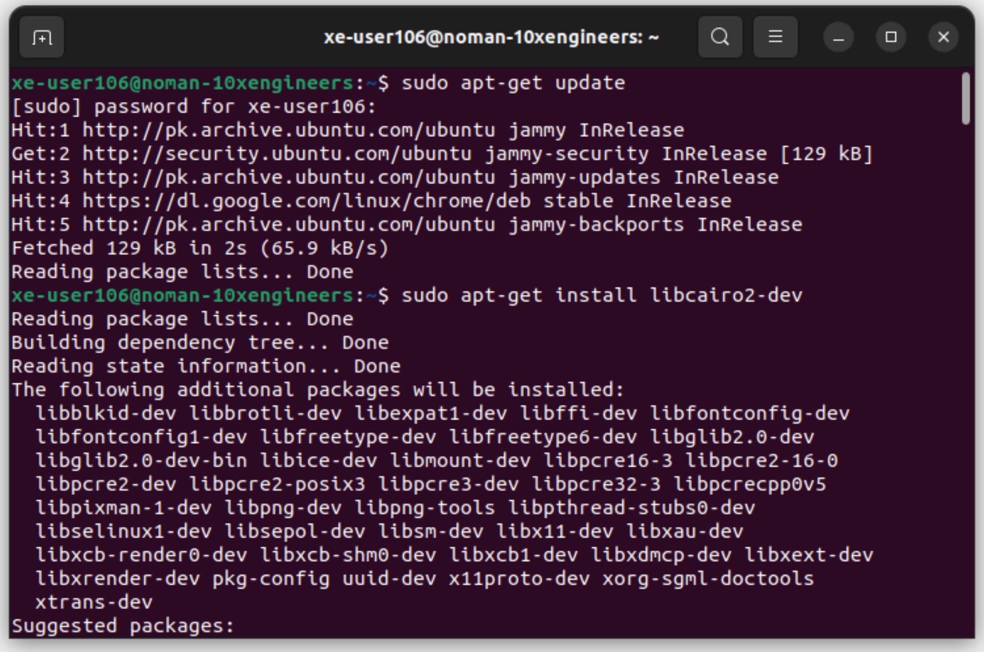
Module: R5: RV-fpga
Section: Installations **Task:** Tools

Task 1.3

RVfpga-Pipeline

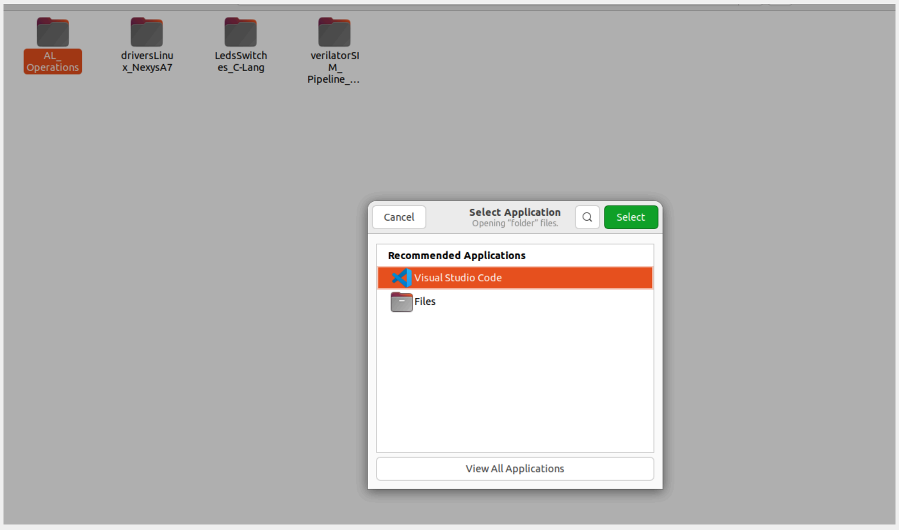
- ➢ **Testing:**
  - ■ **RVfpga-Pipeline**
    1. In order to build this, we need to install the following packages:

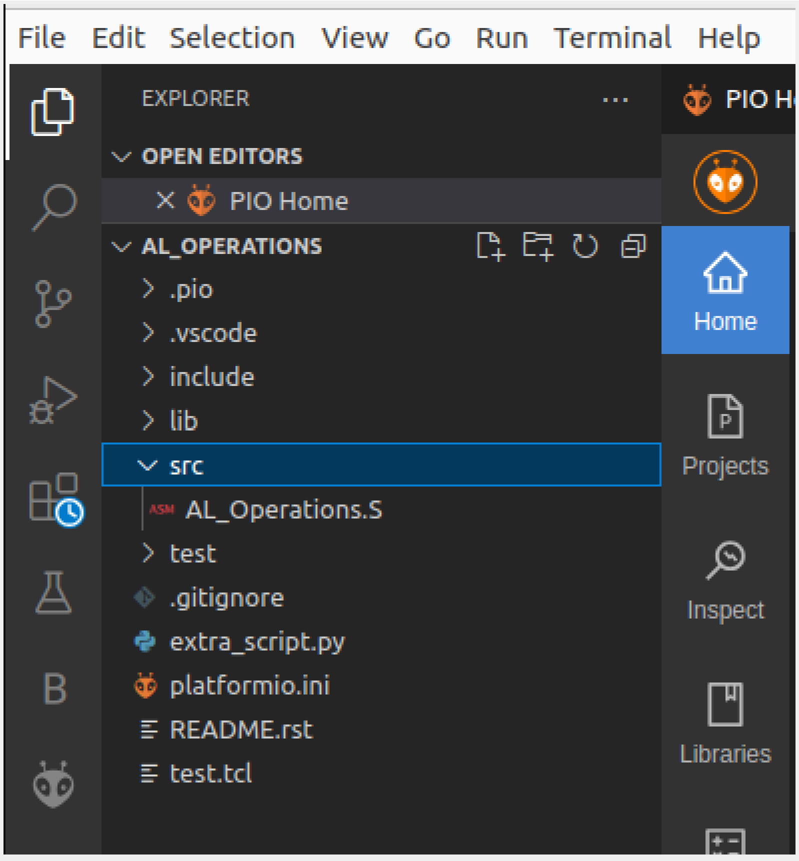
```
sudo apt-get update
sudo apt-get install libcairo2-dev
sudo apt-get install libgtk-3-dev
```



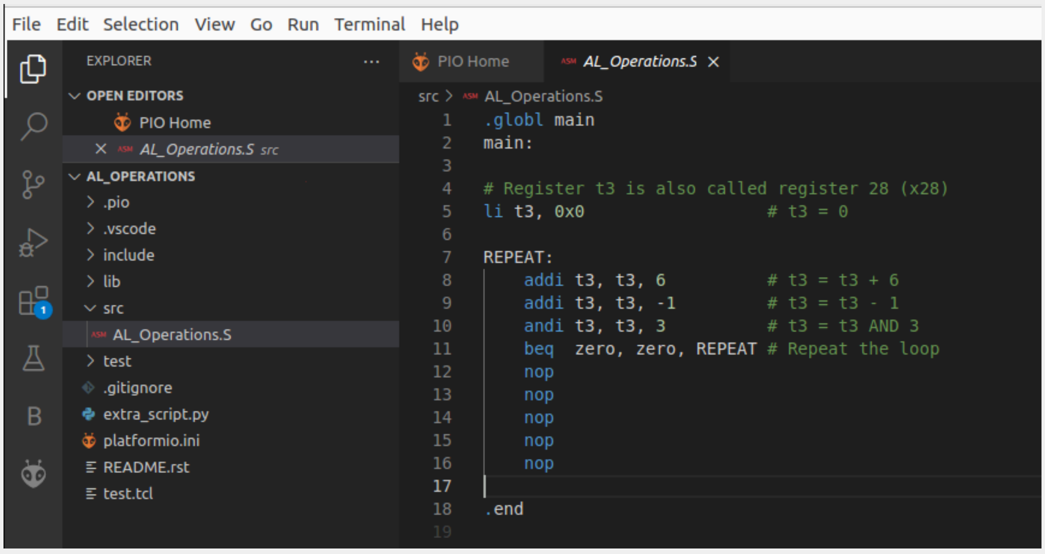
```
xe-user106@noman-10xengineers:~$ sudo apt-get update
[sudo] password for xe-user106:
Hit:1 http://pk.archive.ubuntu.com/ubuntu jammy InRelease
Get:2 http://security.ubuntu.com/ubuntu jammy-security InRelease [129 kB]
Hit:3 http://pk.archive.ubuntu.com/ubuntu jammy-updates InRelease
Hit:4 https://dl.google.com/linux/chrome/deb stable InRelease
Hit:5 http://pk.archive.ubuntu.com/ubuntu jammy-backports InRelease
Fetched 129 kB in 2s (65.9 kB/s)
Reading package lists... Done
xe-user106@noman-10xengineers:~$ sudo apt-get install libcairo2-dev
Reading package lists... Done
Building dependency tree... Done
Reading state information... Done
The following additional packages will be installed:
  libblkid-dev libbrotli-dev libexpat1-dev libffi-dev libfontconfig-dev
  libfontconfig1-dev libfreetype-dev libfreetype6-dev libglib2.0-dev
  libglib2.0-dev-bin libice-dev libmount-dev libpcre16-3 libpcre2-16-0
  libpcre2-dev libpcre2-posix3 libpcre3-dev libpcre32-3 libpcrecpp0v5
  libpixman-1-dev libpng-dev libpng-tools libpthread-stubs0-dev
  libselinux1-dev libsepol-dev libsm-dev libx11-dev libxau-dev
  libxcb-render0-dev libxcb-shm0-dev libxcb1-dev libxdmcp-dev libxext-dev
  libxrender-dev pkg-config uuid-dev x11proto-dev xorg-sgml-doctools
  xtrans-dev
Suggested packages:
```

2. Open the specified folder of example program in VS Code:





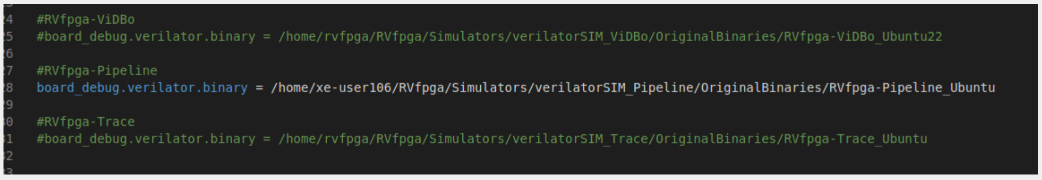
3. PlatformIO will now open this program, which includes three assembly arithmetic-logic instructions (addition, subtraction, and logical and) on the same register, t3 (also called x28), within an infinite loop. We can view the program by expanding the src folder and double-clicking on **AL_Operations.S**.



```
.globl main
main:

# Register t3 is also called register 28 (x28)
li t3, 0x0                    # t3 = 0

REPEAT:
    addi t3, t3, 6            # t3 = t3 + 6
    addi t3, t3, -1           # t3 = t3 - 1
    andi t3, t3, 3            # t3 = t3 AND 3
    beq  zero, zero, REPEAT # Repeat the loop
    nop
    nop
    nop
    nop
    nop

.end
```

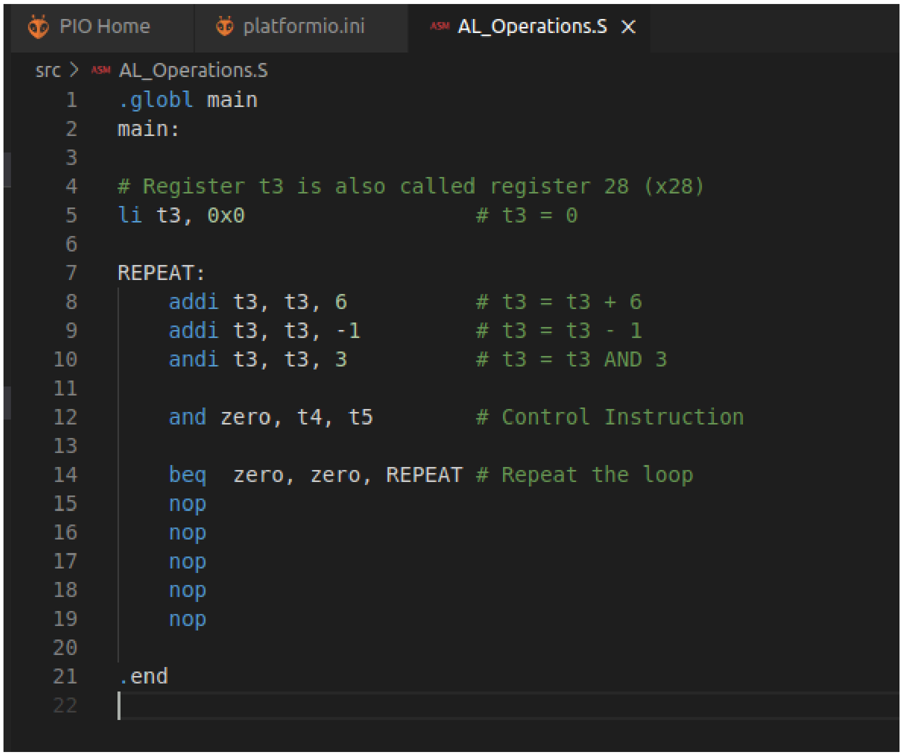
4. Open file **platformio.ini**. Then, established the path to the provided RVfpga-Pipeline simulator binary by editing the following line (replaced [Path-To-RVfpga] with the appropriate path in my system:

```
board_debug.verilator.binary =
/home/xe-user106/RVfpga/Simulators/verilatorSIM_Pipeline/Ori
ginalBinaries/RVfpga-Pipeline_Ubuntu
```



```
#RVfpga-ViDBo
#board_debug.verilator.binary = /home/rvfpga/RVfpga/Simulators/verilatorSIM_ViDBo/OriginalBinaries/RVfpga-ViDBo_Ubuntu22

#RVfpga-Pipeline
board_debug.verilator.binary = /home/xe-user106/RVfpga/Simulators/verilatorSIM_Pipeline/OriginalBinaries/RVfpga-Pipeline_Ubuntu

#RVfpga-Trace
#board_debug.verilator.binary = /home/rvfpga/RVfpga/Simulators/verilatorSIM_Trace/OriginalBinaries/RVfpga-Trace_Ubuntu
```

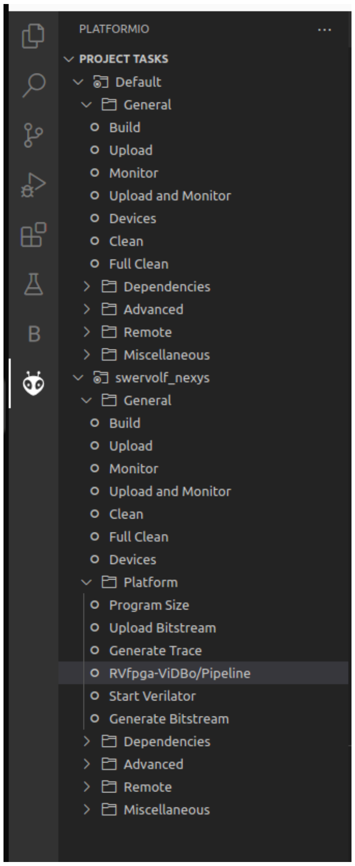
5. Insert the control instruction in order to stop the execution at some point.



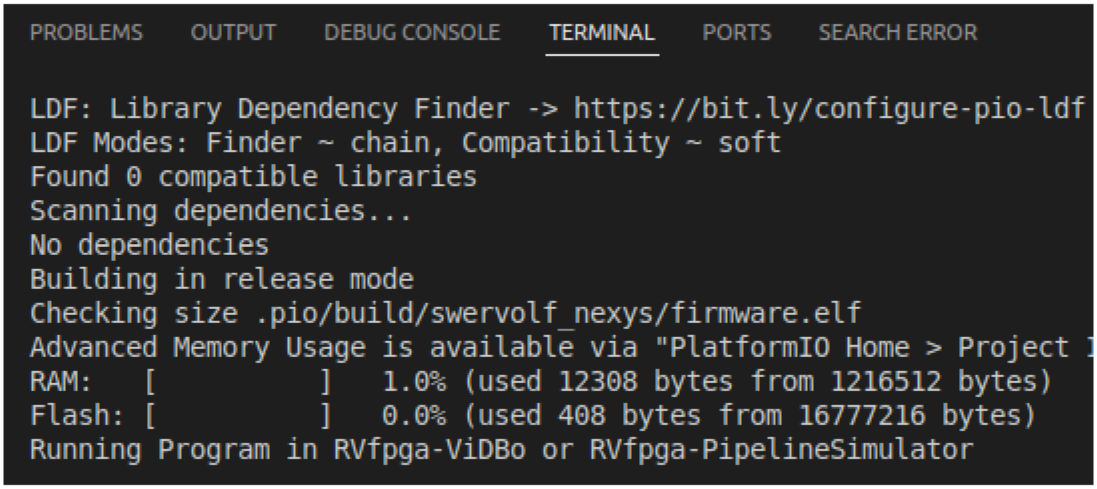
```
.globl main
main:

# Register t3 is also called register 28 (x28)
li t3, 0x0                  # t3 = 0

REPEAT:
    addi t3, t3, 6          # t3 = t3 + 6
    addi t3, t3, -1         # t3 = t3 - 1
    andi t3, t3, 3          # t3 = t3 AND 3

    and zero, t4, t5        # Control Instruction

    beq  zero, zero, REPEAT # Repeat the loop
    nop
    nop
    nop
    nop
    nop

.end
```

6. Executed the RVfpga-Pipeline simulator from PlatformIO:
   - Click on the PlatformIO button on the left side.
   - Expand Project Tasks > env:swervolf_nexys > Platform and clicked on **RVfpga-ViDBo/Pipeline**.
   - We have to provide execution rights to the binary by running command

```
chmod +x RVfpga-Pipeline_Ubuntu
```

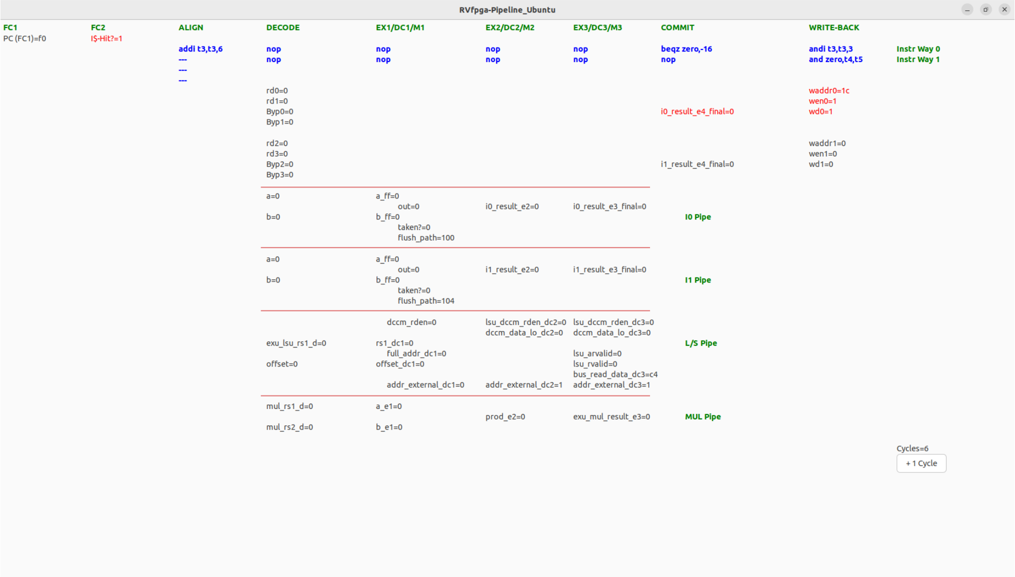


This first compiles the program and then launches the Verilator simulation of the RVfpga SoC running this program.



```
LDF: Library Dependency Finder -> https://bit.ly/configure-pio-ldf
LDF Modes: Finder ~ chain, Compatibility ~ soft
Found 0 compatible libraries
Scanning dependencies...
No dependencies
Building in release mode
Checking size .pio/build/swervolf_nexys/firmware.elf
Advanced Memory Usage is available via "PlatformIO Home > Project I
RAM:   [          ]   1.0% (used 12308 bytes from 1216512 bytes)
Flash: [          ]   0.0% (used 408 bytes from 16777216 bytes)
Running Program in RVfpga-ViDBo or RVfpga-PipelineSimulator
```

7. A new window will open that shows the SweRV EH1 pipeline with a selection of signals for each of the 9 stages.



```
FC1         FC2         ALIGN         DECODE              EX1/DC1/M1            EX2/DC2/M2            EX3/DC3/M3              COMMIT                WRITE-BACK
PC (FC1)=f0 I$-Hit?=1

                        addi t3,t3,6  nop                 nop                   nop                   nop                     beqz zero,-16         andi t3,t3,3      Instr Way 0
                        ---           nop                 nop                   nop                   nop                     nop                   and zero,t4,t5    Instr Way 1
                        ---
                        ---

                                      rd0=0                                                                                                         waddr0=1c
                                      rd1=0                                                                                                         wen0=1
                                      Byp0=0                                                                                  i0_result_e4_final=0  wd0=1
                                      Byp1=0

                                      rd2=0                                                                                                         waddr1=0
                                      rd3=0                                                                                                         wen1=0
                                      Byp2=0                                                                                  i1_result_e4_final=0  wd1=0
                                      Byp3=0

                                      a=0                 a_ff=0
                                                              out=0                 i0_result_e2=0        i0_result_e3_final=0
                                      b=0                 b_ff=0                                                                  I0 Pipe
                                                              taken?=0
                                                              flush_path=100

                                      a=0                 a_ff=0
                                                              out=0                 i1_result_e2=0        i1_result_e3_final=0
                                      b=0                 b_ff=0                                                                  I1 Pipe
                                                              taken?=0
                                                              flush_path=104

                                                            dccm_rden=0             lsu_dccm_rden_dc2=0   lsu_dccm_rden_dc3=0
                                                                                    dccm_data_lo_dc2=0    dccm_data_lo_dc3=0
                                      exu_lsu_rs1_d=0     rs1_dc1=0                                                                   L/S Pipe
                                                            full_addr_dc1=0                               lsu_arvalid=0
                                      offset=0            offset_dc1=0                                    lsu_rvalid=0
                                                                                                          bus_read_data_dc3=c4
                                                            addr_external_dc1=0     addr_external_dc2=1   addr_external_dc3=1

                                      mul_rs1_d=0         a_e1=0
                                                                                    prod_e2=0             exu_mul_result_e3=0         MUL Pipe
                                      mul_rs2_d=0         b_e1=0

                                                                                                                                                                      Cycles=6
```