Module: R5: RV-fpga
Section: RISC-V VeeR Core **Task:** CoreMark

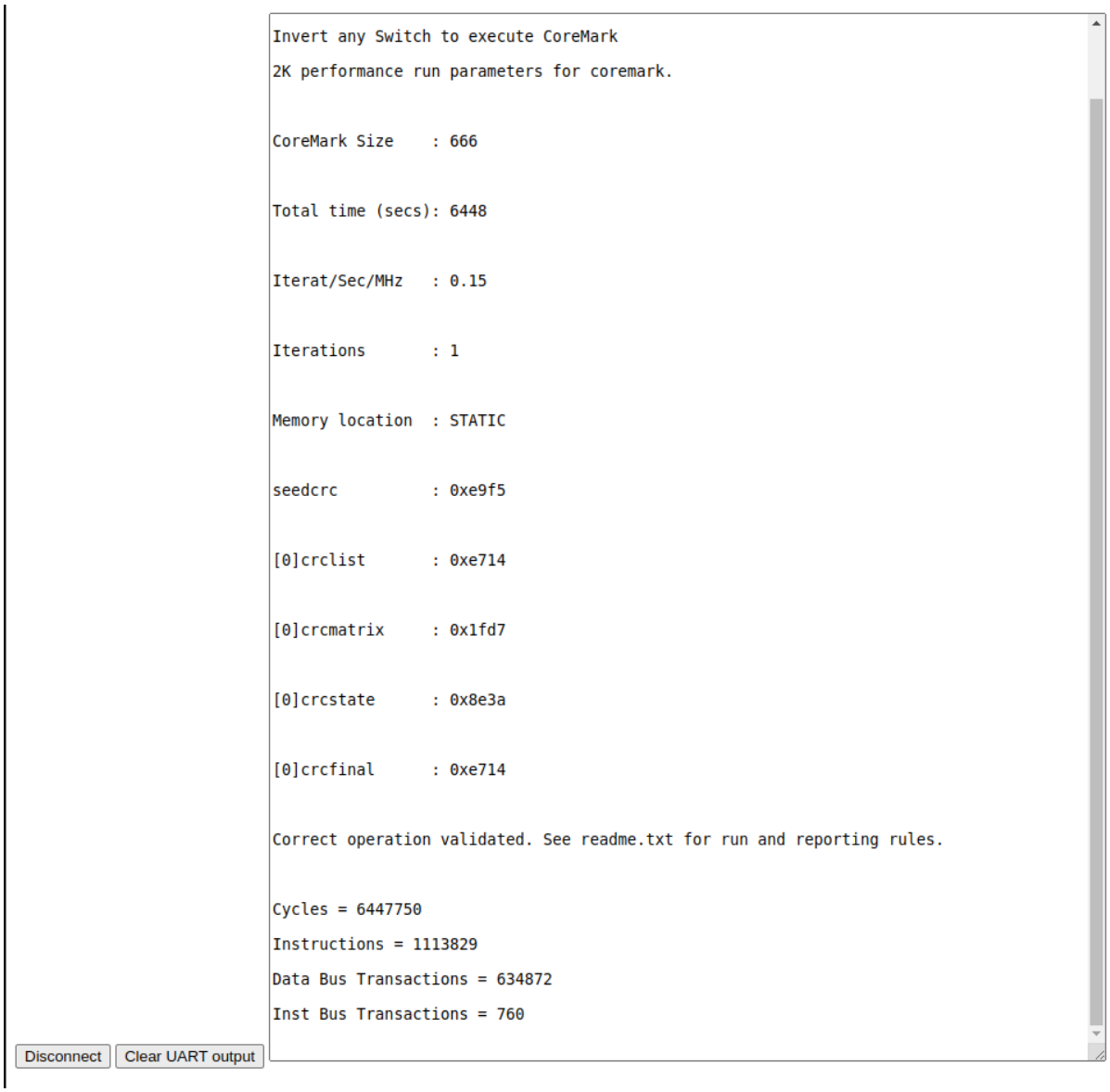
CoreMark

➢ **Benchmarking:**

Objective

The objective is to measure the core's efficiency in handling typical embedded system tasks, including list processing, matrix manipulation, and state machine execution. By conducting this benchmark, we seek to quantify the computational power of the SweRV EH1 core in terms of CoreMark iterations per second.

Running on RVfpga-ViDBo:



Summary

The CoreMark size was 666, and the total execution time was 6448 seconds, resulting in an Iterations per Second per MHz (Iterat/Sec/MHz) value of 0.15. The test utilized static memory, and all operations were validated as correct, as indicated by the CRC values generated during the test (e.g., crclist: 0xe714). The test required 6,447,750 cycles and 1,113,829 instructions, with 634,872 data bus transactions and 760 instruction bus transactions. These metrics provide insight into the computational efficiency and bus transaction activity of the core when executing typical embedded tasks.