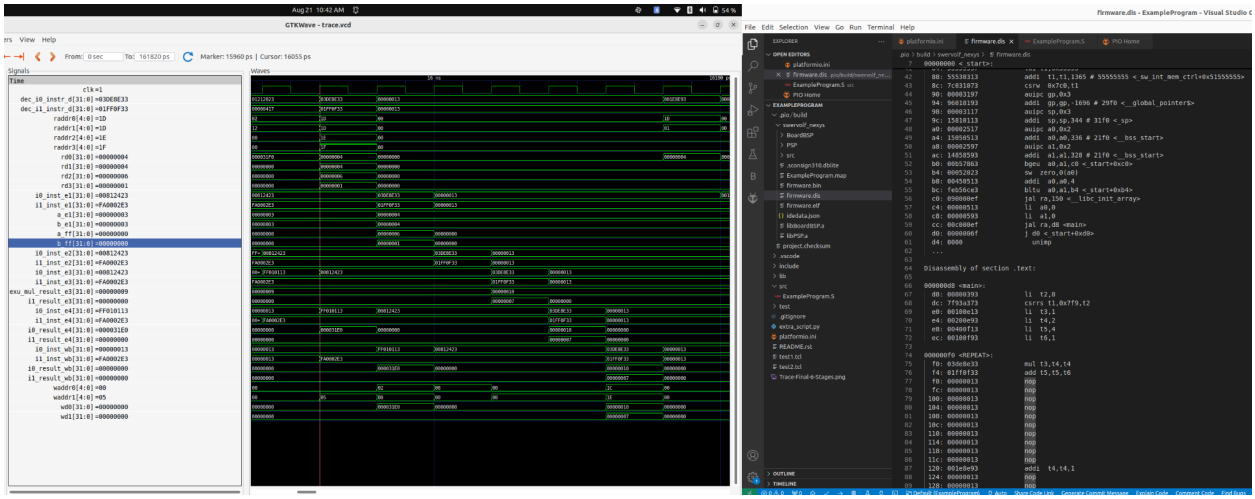
Module: R5: RV-fpga

Section: RISC-V VeeR Core **Task:** Example Program

Example Program

RVfpga-Trace and in RVfpga-Pipeline

➢ **RVfpga-Trace:**



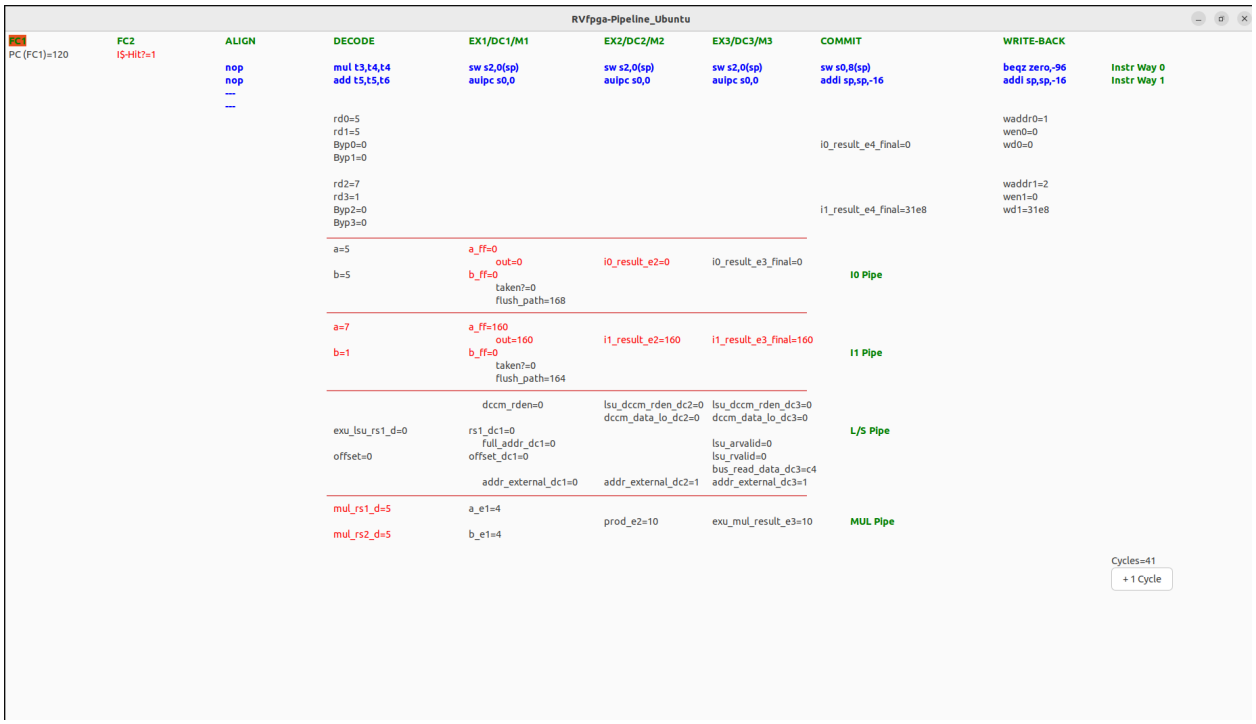
➢ **RVfpga-Pipeline:**

Then change the path for the RVfpga-Pipeline in platform.ini file to point to the right directory:

platformio.ini

```
board = swervolf_nexys
framework = wd-riscv-sdk

monitor_speed = 115200

debug_tool = whisper


#RVfpga-Nexys
board_build.bitstream_file = /home/rvfpga/RVfpga/src/rvfpganexys.bit


#RVfpga-ViDBo
#board_debug.verilator.binary = /home/xe-user106/RVfpga/Simulators/verilatorSIM_ViDBo/OriginalBinaries/RVfpga-ViDBo_Ubuntu22

#RVfpga-Pipeline
board_debug.verilator.binary = /home/xe-user106/RVfpga/Simulators/verilatorSIM_Pipeline/OriginalBinaries/RVfpga-Pipeline_Ubuntu

#RVfpga-Trace
#board_debug.verilator.binary = /home/xe-user106/RVfpga/Simulators/verilatorSIM_Trace/OriginalBinaries/RVfpga-Trace_Ubuntu


build_unflags = -Wa,-march=rv32imac -march=rv32imac
build_flags = -Wa,-march=rv32im -march=rv32im
extra_scripts = extra_script.py
```

Run the RVfpga-ViDBo/Pipeline:


RVfpga-Pipeline_Ubuntu
FC1
PC (FC1)=120
FC2
I$-Hit?=1
ALIGN
DECODE
EX1/DC1/M1
EX2/DC2/M2
EX3/DC3/M3
COMMIT
WRITE-BACK
nop
nop

---
mul t3,t4,t4
add t5,t5,t6
sw s2,0(sp)
auipc s0,0
sw s2,0(sp)
auipc s0,0
sw s2,0(sp)
auipc s0,0
sw s0,8(sp)
addi sp,sp,-16
beqz zero,-96
addi sp,sp,-16
Instr Way 0
Instr Way 1
rd0=5
rd1=5
Byp0=0
Byp1=0
i0_result_e4_final=0
waddr0=1
wen0=0
wd0=0
rd2=7
rd3=1
Byp2=0
Byp3=0
i1_result_e4_final=31e8
waddr1=2
wen1=0
wd1=31e8
a=5
b=5
a_ff=0
out=0
b_ff=0
taken?=0
flush_path=168
i0_result_e2=0
i0_result_e3_final=0
I0 Pipe
a=7
b=1
a_ff=160
out=160
b_ff=0
taken?=0
flush_path=164
i1_result_e2=160
i1_result_e3_final=160
I1 Pipe
exu_lsu_rs1_d=0
offset=0
dccm_rden=0
rs1_dc1=0
full_addr_dc1=0
offset_dc1=0
addr_external_dc1=0
lsu_dccm_rden_dc2=0
dccm_data_lo_dc2=0
addr_external_dc2=1
lsu_dccm_rden_dc3=0
dccm_data_lo_dc3=0
lsu_arvalid=0
lsu_rvalid=0
bus_read_data_dc3=c4
addr_external_dc3=1
L/S Pipe
mul_rs1_d=5
mul_rs2_d=5
a_e1=4
b_e1=4
prod_e2=10
exu_mul_result_e3=10
MUL Pipe
Cycles=41
+ 1 Cycle