

Module: R5: RV-fpga**Section: RISC-V VeeR Core Task: Final Assessment****Final Assessment****➤ Hello World Program:****■ Command:**

```
make -f ${RV_ROOT}/tools/Makefile
```

■ Terminal Output:

```
xe-user106@noman-10xengineers: ~/10x-Engineers/R5_RVfp...
w.o Vtb_top__Trace__3__Slow.o Vtb_top__Trace__4__Slow.o
ranlib Vtb_top__ALL.a
g++ test_tb_top.o verilated.o verilated_vcd_c.o Vtb_top__ALL.a -o Vtb_top
make[1]: Leaving directory '/home/xe-user106/10x-Engineers/R5_RVfpga/Final_Assessment/Cohort-at-10x-Cores-VeeR-EH1/Outputs/obj_dir'
touch verilator-build
./obj_dir/Vtb_top

VerilatorTB: Start of sim

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Hello World from VeeR EH1
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Finished : minstret = 335, mcycle = 1067
See "exec.log" for execution trace with register updates..

- /home/xe-user106/10x-Engineers/R5_RVfpga/Final_Assessment/Cohort-at-10x-Cores-VeeR-EH1/testbench/tb_top.sv:344: Verilog $finish

VerilatorTB: End of sim
xe-user106@noman-10xengineers:~/10x-Engineers/R5_RVfpga/Final_Assessment/Cohort-at-10x-Cores-VeeR-EH1/Outputs$
```

Here are the files that has been generated:

```
VerilatorTB: End of sim
xe-user106@noman-10xengineers:~/10x-Engineers/R5_RVfpga/Final_Assessment/Cohort-at-10x-Cores-VeeR-EH1/Outputs$ ls
console.log      hello_world.exe  program.hex      verilator-build
exec.log         hello_world.map  sim.vcd
hello_world.cpp.s hello_world.o    snapshots
hello_world.dis  obj_dir         trace_port.csv
xe-user106@noman-10xengineers:~/10x-Engineers/R5_RVfpga/Final_Assessment/Cohort-at-10x-Cores-VeeR-EH1/Outputs$
```

➤ How to run an Example Test Program:**■ Steps:**

1. Make a directory for the generated output files. E.g.

```
mkdir temp
```

2. Change the directory as following:

```
cd temp
```

3. Use the following command to run the test example program:

```
make -f $RV_ROOT/tools/Makefile verilator TEST=example_asm_test
```

■ Terminal Output:

```
xe-user106@noman-10xengineers:~/10x-Engineers/R5_RVfpga/Final_Assessment/Outputs/example-test$ make -f $RV_ROOT/tools/Makefile verilator TEST=example_asm_test
riscv64-unknown-elf-cpp -Isnapshots/default /home/xe-user106/10x-Engineers/R5_RVfpga/Final_Assessment/Cohort-at-10x-Cores-VeeR-EH1/testbench/tests/example_asm_test/example_asm_test.cpp.s > example_asm_test.cpp.s
riscv64-unknown-elf-as -mabi=ilp32 -march=rv32imc_zicsr example_asm_test.cpp.s -o example_asm_test.o
Building example_asm_test
riscv64-unknown-elf-gcc -mabi=ilp32 -march=rv32imc_zicsr -Wl,-Map=example_asm_test.map -lgcc -T/home/xe-user106/10x-Engineers/R5_RVfpga/Final_Assessment/Cohort-at-10x-Cores-VeeR-EH1/testbench/link.ld -o example_asm_test.exe example_asm_test.o -nostartfiles
riscv64-unknown-elf-objcopy -O verilog example_asm_test.exe program.hex
riscv64-unknown-elf-objdump -S example_asm_test.exe > example_asm_test.dis
Completed building example_asm_test
./obj_dir/Vtb_top

VerilatorTB: Start of sim

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TEST PASSED
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Finished : minstret = 917, mcycle = 2870
See "exec.log" for execution trace with register updates..

- /home/xe-user106/10x-Engineers/R5_RVfpga/Final_Assessment/Cohort-at-10x-Cores-VeeR-EH1/testbench/tb_top.sv:344: Verilog $finish

VerilatorTB: End of sim
```

Here are the files that has been generated:

```
xe-user106@noman-10xengineers:~/10x-Engineers/R5_RVfpga/Final_Assessment/Outputs/example-test$ ls
console.log      example_asm_test.exe  exec.log          sim.vcd          verilator-build
example_asm_test.cpp.s  example_asm_test.map  obj_dir          snapshots
example_asm_test.dis  example_asm_test.o    program.hex       trace_port.csv
xe-user106@noman-10xengineers:~/10x-Engineers/R5_RVfpga/Final_Assessment/Outputs/example-test$
```

■ Makefile Explanation:

1. Command:

```
make -f $RV_ROOT/tools/Makefile verilator
TEST=example_asm_test
```

2. Purpose:

This command runs the verilator target from the specified Makefile, while setting the TEST variable to **example_asm_test**.

3. Environment Check:

The Makefile checks if the **RV_ROOT** environment variable is set correctly. If it doesn't point to a valid directory, the process will stop with an error.

4. Building the Test Program:

The Makefile will look for a RISC-V GCC toolchain (riscv64-unknown-elf-gcc). If found, it compiles the **example_asm_test** file into a hex file (**program.hex**). If the toolchain is not found, it uses a precompiled hex file instead.

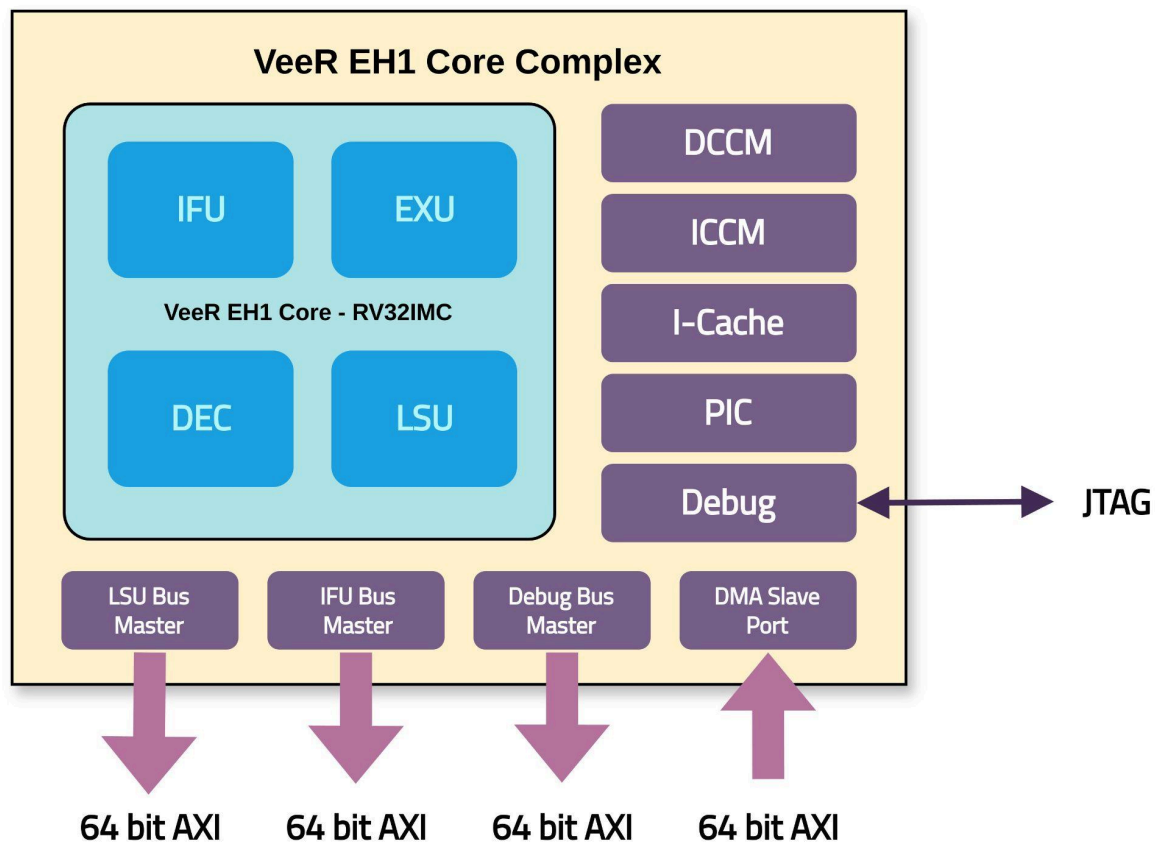
5. Verilator Build:

The verilator-build target is executed, which compiles the Verilog source files using Verilator. It prepares the necessary files for simulation.

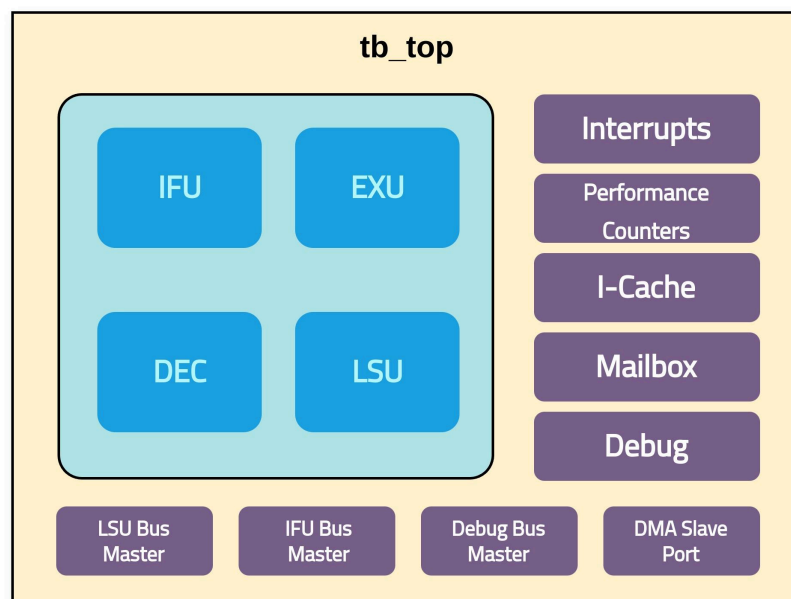
6. Running the Simulation:

The verilator target is then executed. It runs the Verilator simulation with the compiled hex file (program.hex). The simulation will produce output based on the **example_asm_test program**.

➤ Block Diagram of VeeR EH1 core complex:



➤ **Block Diagram of Testbench Top File:**



➤ **Testplans:**

The testplans can be found at the following link: [TESTPLAN](#)