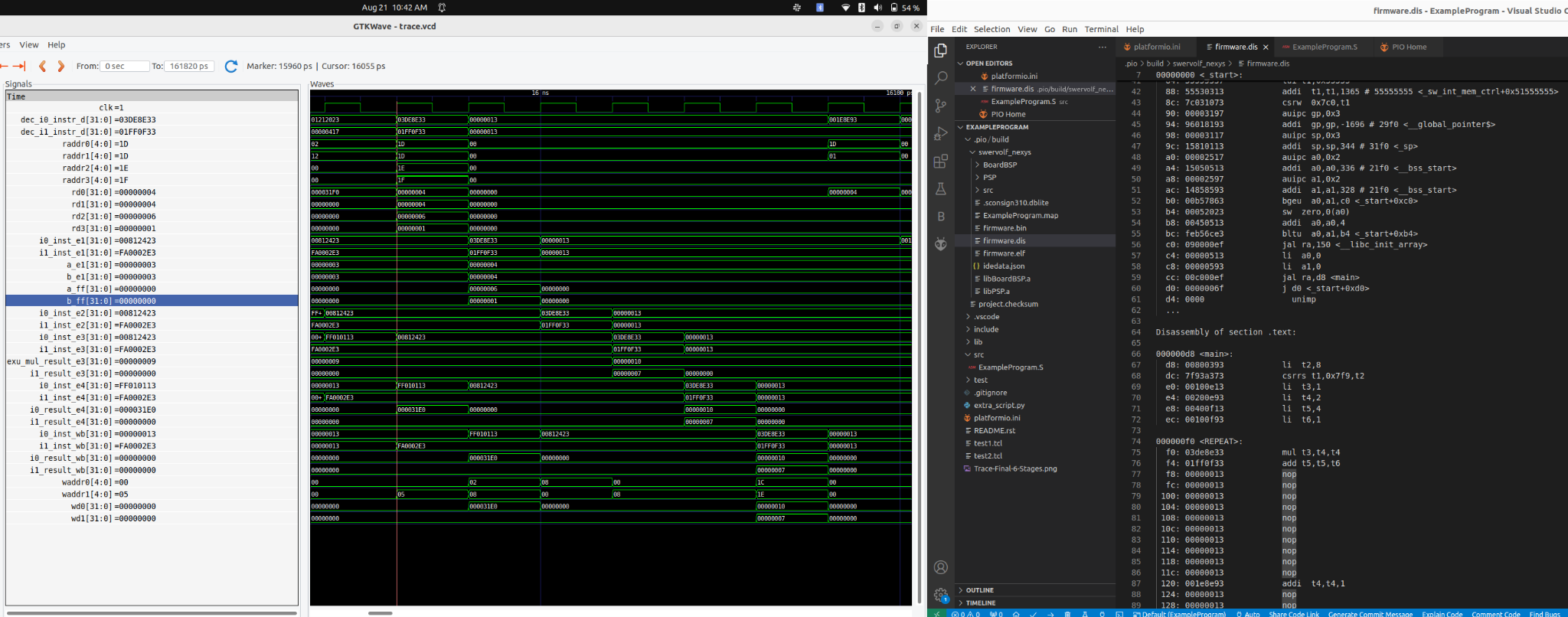
**Module: R5: RV-fpga**

**Section:** RISC-V VeeR Core **Task:** Example Program

**Example Program**

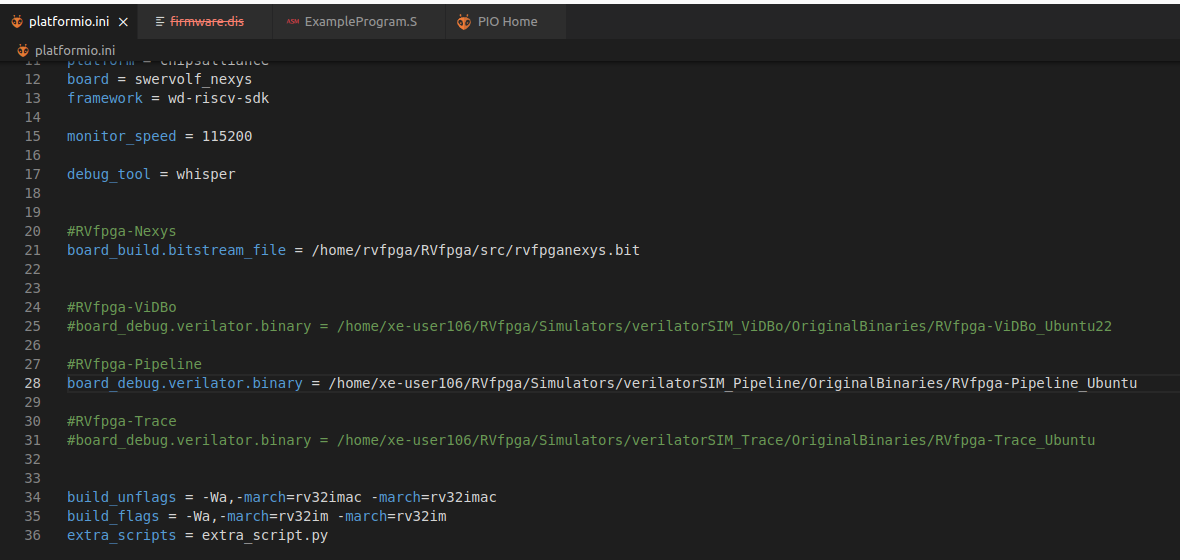
**RVfpga-Trace and in RVfpga-Pipeline**

* **RVfpga-Trace:**

****

* **RVfpga-Pipeline:**

Then change the path for the RVfpga-Pipeline in platform.ini file to point to the right directory:



Run the RVfpga-ViDBo/Pipeline:

