**Module: R5: RV-fpga**

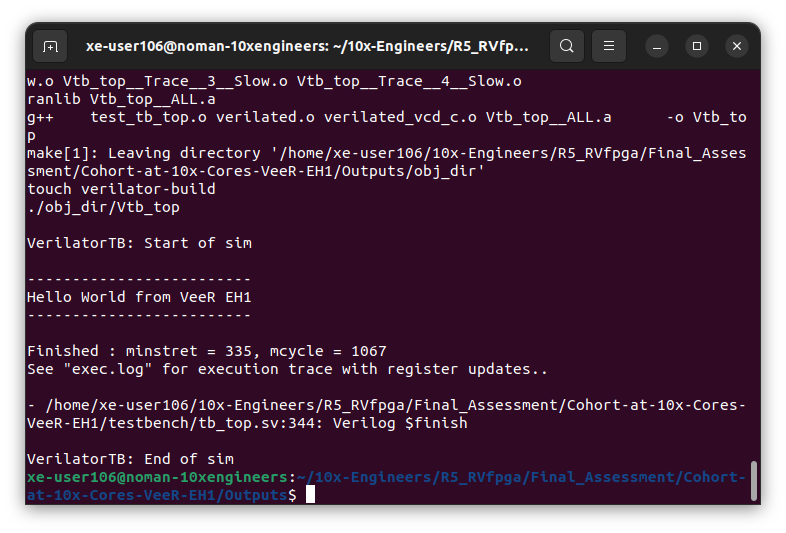
**Section:** RISC-V VeeR Core **Task:** Final Assessment

**Final Assessment**

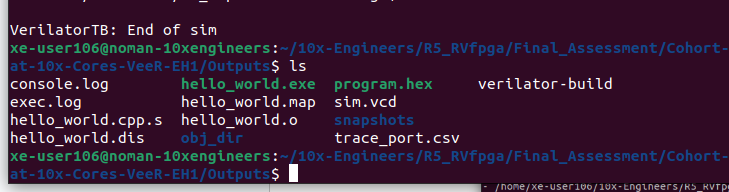
* **Hello World Program:**
  + **Command:**

make -f ${RV\_ROOT}/tools/Makefile

* + **Terminal Output:**

****

Here are the files that has been generated:

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* **How to run an Example Test Program:**
  + **Steps:**
    1. Make a directory for the generated output files. E.g.

**mkdir temp**

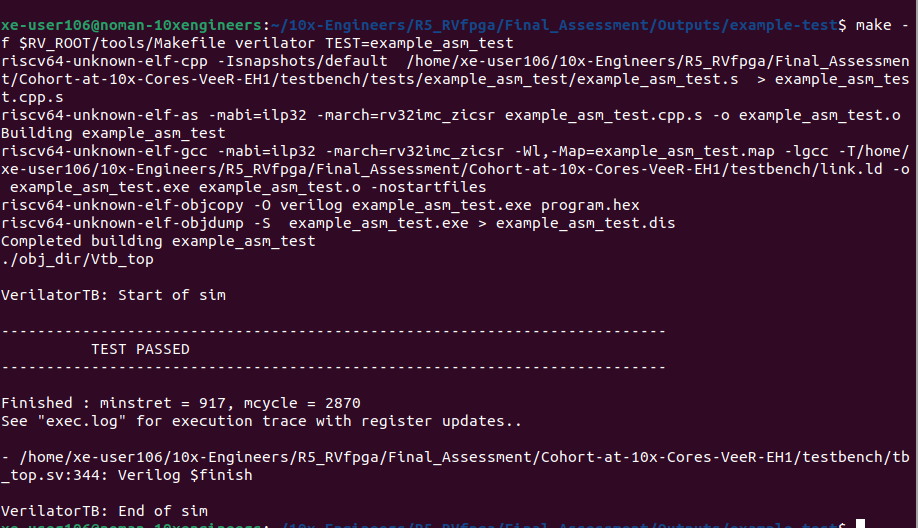
* + 1. Change the directory as following:

**cd temp**

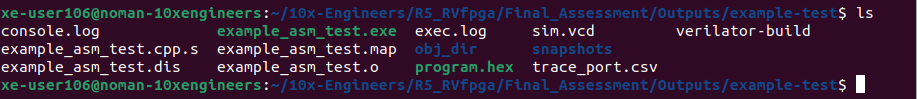
* + 1. Use the following command to run the test example program:

make -f $RV\_ROOT/tools/Makefile verilator TEST=example\_asm\_test

* + **Terminal Output:**

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Here are the files that has been generated:

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* + **Makefile Explanation:**
    1. **Command:**

make -f $RV\_ROOT/tools/Makefile verilator TEST=example\_asm\_test

* + 1. **Purpose:**

This command runs the verilator target from the specified Makefile, while setting the TEST variable to **example\_asm\_test**.

* + 1. **Environment Check:**

The Makefile checks if the **RV\_ROOT** environment variable is set correctly. If it doesn't point to a valid directory, the process will stop with an error.

* + 1. **Building the Test Program:**

The Makefile will look for a RISC-V GCC toolchain (riscv64-unknown-elf-gcc). If found, it compiles the **example\_asm\_test** file into a hex file (**program.hex**). If the toolchain is not found, it uses a precompiled hex file instead.

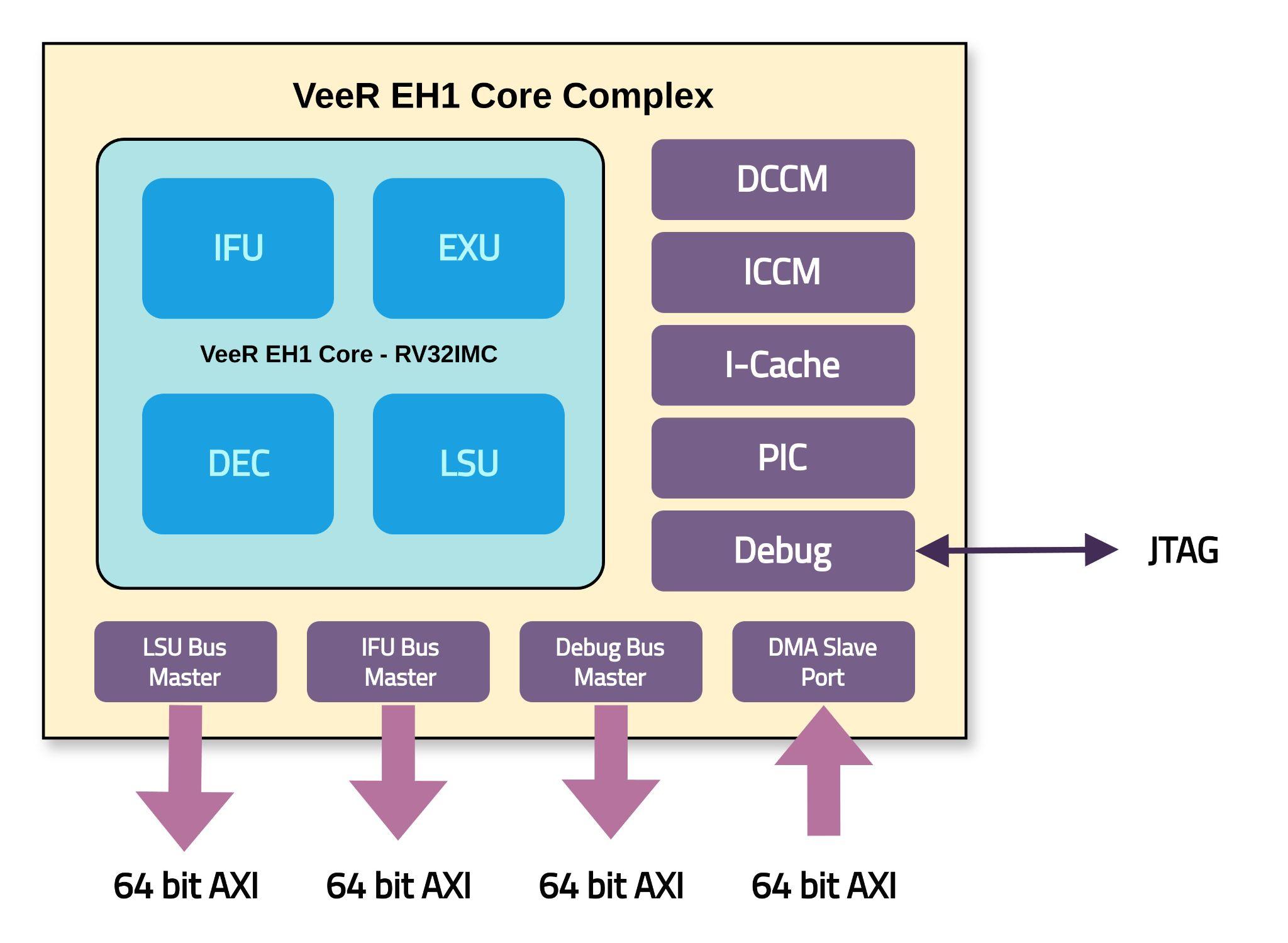
* + 1. **Verilator Build:**

The verilator-build target is executed, which compiles the Verilog source files using Verilator. It prepares the necessary files for simulation.

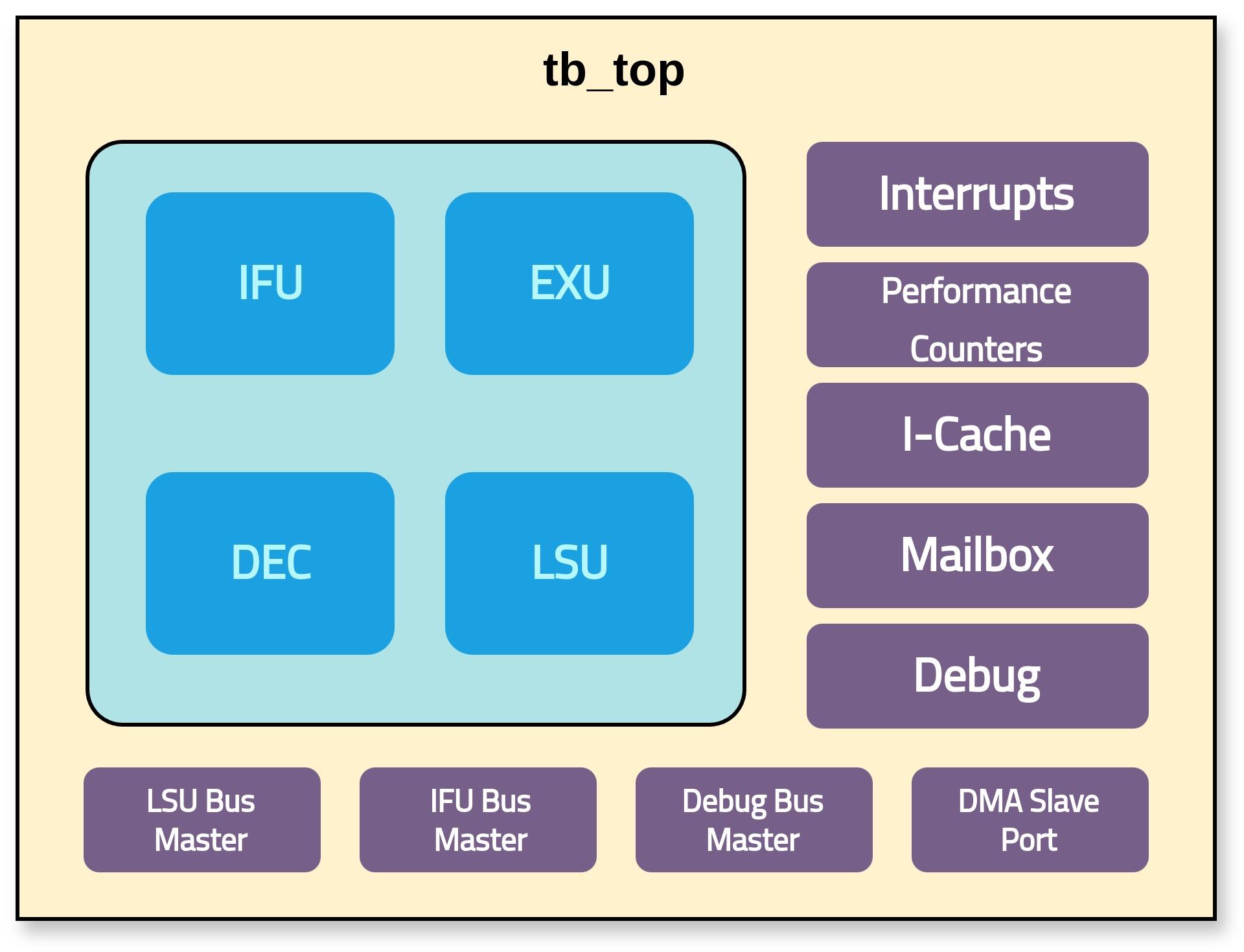
* + 1. **Running the Simulation:**

The verilator target is then executed. It runs the Verilator simulation with the compiled hex file (program.hex). The simulation will produce output based on the **example\_asm\_test program**.

* **Block Diagram of VeeR EH1 core complex:**

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* **Block Diagram of Testbench Top File:**

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* **Testplans:**

The testplans can be found at the following link: [TESTPLAN](https://docs.google.com/spreadsheets/d/17z2MuNscjXZKYsNTLu15YemURzcrsqH-EUcoThfFN2M/edit?usp=sharing)