

Module: SV for Verification
Section: Modules & Classes Task: Or Gate Model

OR Gate Model - [EDA Playground](#)

➤ **DUT:**

```
// Or_Gate Model
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// Dated: Aug 28, 2024

module dut ( input logic A, B,
              output logic E);

    wire C, D;
    and g0(C, A, B);
    not g1(D, B);
    and g2(E, C, D);

endmodule
```

➤ **Testbench:**

```
// Testbench

module tb;
    reg A, B;
    wire E;

    dut m1(.A(A),
           .B(B),
           .E(E));

    initial begin
        A = 0;
        B = 0;
        $display("Inputs: A = %b, B = %b", A, B);
        $display("Output: E = %b", E);

        #40;
        A = 1;

        $display("Inputs: A = %b, B = %b", A, B);
        $display("Output: E = %b", E);

        #20;
        B = 1;
        A = 0;

        $display("Inputs: A = %b, B = %b", A, B);
        $display("Output: E = %b", E);
    end
endmodule
```

```

#20;
A = 1;
B = 1;

$display("Inputs: A = %b, B = %b", A, B);
$display("Output: E = %b", E);

#20;
A = 0;
B = 1;
$display("Inputs: A = %b, B = %b", A, B);
$display("Output: E = %b", E);

$finish;
end

endmodule

```

➤ Output:

```

Log Share
# KERNEL: kernel process initialization done.
# Allocation: Simulator allocated 4667 kB (elbread=427 elab2=4105 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: Inputs: A = 0, B = 0
# KERNEL: Output: E = x
# KERNEL: Inputs: A = 1, B = 0
# KERNEL: Output: E = 0
# KERNEL: Inputs: A = 0, B = 1
# KERNEL: Output: E = 0
# KERNEL: Inputs: A = 1, B = 1
# KERNEL: Output: E = 0
# KERNEL: Inputs: A = 0, B = 1
# KERNEL: Output: E = 0
# RUNTIME: Info: RUNTIME_0068 testbench.sv (43): $finish called.
# KERNEL: Time: 100 ns, Iteration: 0, Instance: /tb, Process: @INITIAL#11_0@.
# KERNEL: stopped at time: 100 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Done

```

[EDA Files](#)