Module: SV for Verification
Section: Modules & Classes **Task:** Or Gate Model

OR Gate Model - EDA Playground

➢ DUT:

```
// Or_Gate Model
// Author: Noman Rafiq
// Dated: Aug 28, 2024

module dut ( input logic A, B,
                output logic E);

  wire C, D;
  and g0(C, A, B);
  not g1(D, B);
  and g2(E, C, D);

endmodule
```

➢ Testbench:

```
// Testbench

module tb;
  reg A, B;
  wire E;

  dut m1(.A(A),
         .B(B),
         .E(E));

  initial begin
    A = 0;
    B = 0;
    $display("Inputs: A = %b, B = %b", A, B);
    $display("Output: E = %b", E);

    #40;
    A = 1;

    $display("Inputs: A = %b, B = %b", A, B);
    $display("Output: E = %b", E);

    #20;
    B = 1;
    A = 0;

    $display("Inputs: A = %b, B = %b", A, B);
    $display("Output: E = %b", E);
```

```
    #20;
    A = 1;
    B = 1;

    $display("Inputs: A = %b, B = %b", A, B);
    $display("Output: E = %b", E);

    #20;
    A = 0;
    B = 1;
    $display("Inputs: A = %b, B = %b", A, B);
    $display("Output: E = %b", E);

    $finish;
  end

endmodule
```

➢ **Output:**

EDA Files