Module: SV for Verification
Section: Getting Started **Task:** Verification Approaches

Verification Approaches

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1. **What are the different approaches to testing in design verification?**
   There are two basic types of verification approaches we can opt for while verifying designs.
   1. Directed-Testing
   2. Constrained-Random Testing

2. **How constrained Random testing is helpful in design verification?**
   One of the main advantages of constrained-random testing is that it often covers a wider space than a directed one. Constrained random testing may also be able to reach areas that were never anticipated, hence, finding unexpected bugs.

3. **How can we cover a corner case missed during constrained random testing?**
   We can cover the missed cases by manually writing directed tests for those cases. You may have to write these few directed test cases that are a very unlikely to be reached by random tests.

4. **What are the different layers of layered testbench? Explain each layer briefly.**
   There are a total of 4 fundamental layers in a layered testbench. Namely:
   1. Signal Layer
   2. Command Layer
   3. Functional Layer
   4. Scenario Layer
   5. Test Layer

   ➢ **Signal Layer:** It is the lowest layer in our testbench which contains design under test and the signals that connect it to testbench.
   ➢ **Command Layer:** This layer drives the DUT's inputs with single commands (e.g., bus read/write) and monitors the outputs, grouping signal transitions into commands.
   ➢ **Functional Layer:** It is the next higher level in line. Comprising the Agent, Scoreboard, and Checker, this layer handles higher-level transactions (e.g., DMA read/write), breaking them into individual transactions and comparing expected results with DUT outputs.

- **Scenario Layer:** Generates various stimuli to test the DUT using constrained-random values.
- **Test Layer:** This is the highest-level layer in our testbench. The test contains the constraints to create the stimuli.