**Module: SV for Verification**
**Section:** Coverage **Task:** Assertions

# Task 1 - EDA Playground

Assertions

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## ➢ Source Code:

- **Design Code:**

```
module SignalDetector(input logic clk, signal_in);

  // Property for checking signal stability

property check_stability_3_cycles;

@(posedge clk)

(signal_in == 1'b1) ##1 $stable(signal_in) ##1 $stable(signal_in);// Check if
signal_in is 1 for 3 consecutive cycles

endproperty

// Detecting rising edge

  assert property(@(posedge clk) $rose(signal_in)) // Check if the signal has gone
from 0 to 1

  else $error("ERROR: Signal Didn't rise @%0t", $time);

  // Detecting falling edge

  assert property(@(posedge clk) $fell(signal_in)) // Check if the signal has gone
from 1 to 0

  else $error("ERROR: Signal Didn't Fall @%0t", $time);

  // Stability Check

  assert property (check_stability_3_cycles)

    else $error("ERROR: signal_in was not stable for 3 consecutive clock cycles
@%0t", $time);

endmodule
```

- **Testbench Code:**

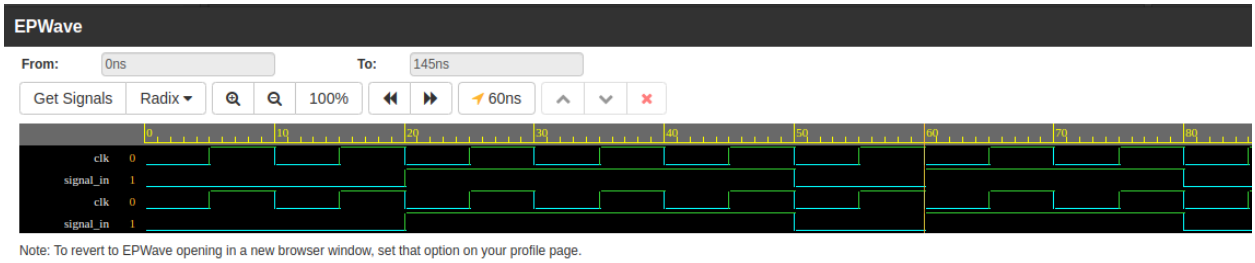
```
module tb;

  reg clk, signal_in;
```

```
  // Module Instantiation
  SignalDetector dut(.clk(clk), .signal_in(signal_in));
  // Clock Generator
  initial begin
    clk = 0;
    forever #5 clk = ~clk;
  end
  // Stimulus
  initial begin
      signal_in = 0;
    $display("@%0t Driven Value:: Signal_in = %0d", $time, signal_in);
      #20ns;
      signal_in = 1;
    $display("@%0t Driven Value:: Signal_in = %0d", $time, signal_in);
      #30ns;
      signal_in = 0;
    $display("@%0t Driven Value:: Signal_in = %0d", $time, signal_in);
      #10ns;
      signal_in = 1;
    $display("@%0t Driven Value:: Signal_in = %0d", $time, signal_in);
      #20ns;
      signal_in = 0;
    $display("@%0t Driven Value:: Signal_in = %0d", $time, signal_in);
  end
  // Dump file
  initial begin
```

```
    $dumpvars;
    $dumpfile("dump.vcd");
    #150;
    $finish;
  end
endmodule
```

## ➢ Simulation Output:




Note: To revert to EPWave opening in a new browser window, set that option on your profile page.

```
Log  Share
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64;  Sep 21 06:01 2024
@0 Driven Value:: Signal_in = 0
"design.sv", 20: tb.dut.unnamed$$_2: started at 5ns failed at 5ns
        Offending '(signal_in == 1'b1)'
Error: "design.sv", 20: tb.dut.unnamed$$_2: at time 5 ns
ERROR: signal_in was not stable for 3 consecutive clock cycles @5
"design.sv", 13: tb.dut.unnamed$$_0: started at 5ns failed at 5ns
        Offending '$rose(signal_in)'
Error: "design.sv", 13: tb.dut.unnamed$$_0: at time 5 ns
ERROR: Signal Didn't rise @5
"design.sv", 20: tb.dut.unnamed$$_2: started at 15ns failed at 15ns
        Offending '(signal_in == 1'b1)'
Error: "design.sv", 20: tb.dut.unnamed$$_2: at time 15 ns
ERROR: signal_in was not stable for 3 consecutive clock cycles @15
"design.sv", 13: tb.dut.unnamed$$_0: started at 15ns failed at 15ns
        Offending '$rose(signal_in)'
Error: "design.sv", 13: tb.dut.unnamed$$_0: at time 15 ns
ERROR: Signal Didn't rise @15
"design.sv", 17: tb.dut.unnamed$$_1: started at 15ns failed at 15ns
        Offending '$fell(signal_in)'
Error: "design.sv", 17: tb.dut.unnamed$$_1: at time 15 ns
ERROR: Signal Didn't Fall @15
@20 Driven Value:: Signal_in = 1
"design.sv", 17: tb.dut.unnamed$$_1: started at 25ns failed at 25ns
        Offending '$fell(signal_in)'
Error: "design.sv", 17: tb.dut.unnamed$$_1: at time 25 ns
ERROR: Signal Didn't Fall @25
"design.sv", 13: tb.dut.unnamed$$_0: started at 35ns failed at 35ns
        Offending '$rose(signal_in)'
Error: "design.sv", 13: tb.dut.unnamed$$_0: at time 35 ns
ERROR: Signal Didn't rise @35
"design.sv", 17: tb.dut.unnamed$$_1: started at 35ns failed at 35ns
        Offending '$fell(signal_in)'
Error: "design.sv", 17: tb.dut.unnamed$$_1: at time 35 ns
ERROR: Signal Didn't Fall @35
"design.sv", 13: tb.dut.unnamed$$_0: started at 45ns failed at 45ns
        Offending '$rose(signal_in)'
Error: "design.sv", 13: tb.dut.unnamed$$_0: at time 45 ns
ERROR: Signal Didn't rise @45
"design.sv", 17: tb.dut.unnamed$$_1: started at 45ns failed at 45ns
        Offending '$fell(signal_in)'
Error: "design.sv", 17: tb.dut.unnamed$$_1: at time 45 ns
```