Module: SV for Verification
Section: Modules & Classes **Task:** Inheritance

Task 2

Inheritance

➢ **Can a parent class access child class variables?**
No, a parent class cannot directly access variables or methods that are defined in its child classes. In SystemVerilog, inheritance is a one-way relationship where the child class inherits properties and methods from the parent class, but the parent class does not have knowledge of the child class's properties and methods.

Hence, The parent class does not and cannot access child class-specific variables directly. The design of inheritance is such that child classes build upon the parent class, but the reverse is not true.

➢ **What is the difference between “new ()” and “new []”?**

- **new( ):**
  It is also called a class constructor that initializes a class object. When an object is created, for example,

  ```
  Packet p = new;
  ```

  the system executes the new function associated with the class:

  ```
  class Packet;

  integer command;

  function new();
  command = IDLE;
  endfunction

  Endclass
  ```

  As shown above, new is now being used in two very different contexts with very different semantics. The variable declaration creates an object of class Packet. In the course of creating this instance, the new() function is invoked, in which any specialized initialization required can be done.

- **new[ ]:**
  The new constructor sets the size of a dynamic array and initializes its elements. It may appear in place of the right-hand side expression of variable declaration

assignments and blocking procedural assignments when the left-hand side indicates a dynamic array.