Module: SV for Verification
Section: Arrays **Task:** Associative Arrays

Task

Associative Arrays - Link to EDA Project

- **Processor Memory:**
  - **Code Snippet:**

```
// Author: Noman Rafiq
// Dated: Sep 02, 2024

typedef bit[23:0] word; // Create a 24-bit word type
typedef bit[19:0] address; // Create a 20-bit address-space type

module tb;
  address PC; // Declare PC that holds address
  word mem[address];       // Declare memory for program
  word ISR[address]; // Declare ISR
  bit rst;

  initial begin

    if (rst) begin

  // reset condition
  PC = 0; // PC starts at 0x0
  end

  else begin
      PC = 20'h400; // Set PC for main
    mem[PC] = 24'h123456; // Fill memory at 0x400

    PC = PC + 1; // Increment PC
    mem[PC] = 24'h789ABC; // Fill memory at 0x401

    PC = 20'hFFFFF; // Set PC for ISR
    mem[PC] = 24'h0F1E2D; // ISR = return from Interrupt

    // Diplay Elements
    foreach (mem[i]) $display("Array Elements: mem[%0x] = %0x", i,
mem[i]);

    // Diplay Number of Elements
    $display("Number of Elements: %0d", mem.size());
```

```
  end
  end

  initial begin
    rst = 1;
    #30 rst = 0;
  end

endmodule
```

➢ **Output:**

```
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64;  Sep  2 08:02 2024
Array Elements: mem[400] = 123456
Array Elements: mem[401] = 789abc
Array Elements: mem[fffff] = f1e2d
Number of Elements: 3
          V C S   S i m u l a t i o n   R e p o r t
Time: 30 ns
CPU Time:      0.440 seconds;       Data structure size:   0.0Mb
Mon Sep  2 08:02:39 2024
Done
```