test id	hdd section	test name	test status	description or objective of test	stimulus geneation procedure	test passes when	test fails when	checking procedure	assertion description
								Lleing Cimulation	
								Using Simulation	
								PS: Both the testbench and	
								<b>DUT Memories have been</b>	
						During Reset, Slave		initialized to "DEADBEEF"	
						must ensure that		upon reset. Hence, all the	
						HREADYOUT is HIGH		addresses will have the same	
				In the reset mode, transfer mode is changed		and memory is	HREADYOUT is not	word unless written	
				to IDLE and nothing can be written or read		initialized to provided	High and if Memory is	something (upon de-	
test_001		reset_test	Pass	unless reset is de-asserted.	Apply clock, HRESET=0	known state.	not initialized.	assertion)	
					Apply clock,				
					HTRANS=2b'10,				
					HWRITE= 0,			The testbench read the	
					HRESET=1,			memory and compare the	
					HADDR= Address of Memory,	HRDATA gives the		dummy Memory's output	
					HSIZE= inside {0,1, 2}	correct Data from the	HRDATA does not	with DUT's output when	
					HBURST=3B000,	address with HRESP = 0	provide the correct	stimulus is given to	
test_002		rd_test	Pass	Basic Read Data with no wait signal.	HPROT=4b0001	(OKAY SIGNAL)	data from the address	Scoreboard.	
					Apply clock,				
					HTRANS=2b'10,				
					HWRITE= 0,			Write the same DATA in the	
					HRESET=1,			dummy memory at the same	
					HADDR= Address of Memory,	LINA/DATA:	When HWDATA is not	address. Then, read the value	
				Danie Muiting (Manuel Circul) Data to Manuel III	HSIZE= inside {0,1, 2}	HWDATA is written on a	written in the memory	at the provided address of the	
tost 002		ur tost	Dass	Basic Writing (Word Sized) Data to Memory without any wait states.	HBURST=3B000, HPROT=4b0001	memory at the given address	correctly at the required address	original memory and compare with the dummy memory.	
test_003		wr_test	Pass	Without any wait states.	Apply clock,	audress	required address	with the duffilly memory.	
					Арріу сіоск,				
				It is an alternate <b>Word</b> Write/Read test with	HTRANS = 2'd2				
				incrementing addresses. Firstly, an address is	HWRITE = 1 and 0 (W/R),			Write the HWDATA to some	
				written to and then the value is read from the		HRDATA gives DATA		address and then check the	
				same address to cross-check if the values	HADDR= Managed using rd_ptr and wr_ptr,	equal to the Value		HRDATA value at the same	
				have been correctly written to DUT. Address	HSIZE= 3'b010	which was written	Read Data is not equal	address in the next clock	
				is updated in the end so that we write to a	HBURST=3B000,	I .	to the Written Data at	cycles to verify. You can check	
test_004		word_wr_rd_test	Pass	different location next time.	HPROT=4b0001	address.	a specified address.	this using Simulation.	

	<u> </u>				A south of a str	1	1	T T	
					Apply clock,				
				It is an alternate <b>Halfword</b> Write/Read test	LITDANG - 2'42				
				<u> </u>	HTRANS = 2'd2 HWRITE = 1 and 0 (W/R),			Write the HWDATA to some	
				with incrementing addresses. Firstly, an address is written to and then the value is	HRESET=1,	HDDATA gives DATA		address and then check the	
				read from the same address to cross-check if	1	HRDATA gives DATA equal to the Value		HRDATA value at the same	
					HADDR= Managed using rd_ptr and wr_ptr,	which was written	Dood Data is not acual	address in the next clock	
				the values have been correctly written to	HSIZE= 3'b001,		Read Data is not equal		
tost OOF		alforous our and toot	Doca	DUT. Address is updated in the end so that	HBURST=3B000, HPROT=4b0001	earlier, to the same	to the Written Data at	cycles to verify. You can check	
test_005		alfword_wr_rd_test	Pass	we write to a different location next time.		address.	a specified address.	this using Simulation.	
					Apply clock,				
				It is an alternate <b>Dute</b> Muite/Dood test with	LITRANC 2142				
				It is an alternate <b>Byte</b> Write/Read test with	HTRANS = 2'd2			Write the HWDATA to some	
				incrementing addresses. Firstly, an address is	HWRITE = 1 and 0 (W/R),	LIDDATA circa DATA			
				written to and then the value is read from the	1	HRDATA gives DATA		address and then check the	
				same address to cross-check if the values	HADDR= Managed using rd_ptr and wr_ptr,	equal to the Value	Doed Date is set as a	HRDATA value at the same	
				have been correctly written to DUT. Address	HSIZE= 3'b000,	which was written	Read Data is not equal	address in the next clock	
				is updated in the end so that we write to a	HBURST=3B000,	earlier, to the same	to the Written Data at	cycles to verify. You can check	
test_006	D'	yte_wr_rd_test	Pass	different location next time.	HPROT=4b0001	address.	a specified address.	this using Simulation.	
					Apply clock,				
								Write the HWDATA to a	
				It is a random Write/Read test with randomly	HWRITE = 1 and 0 (W/R),	HRDATA gives DATA		random address and then	
				generated addresses. Multiple W/R	HRESET=1,	equal to the Value		check the HRDATA value if the	
				operations are performed and then values	HSIZE= inside {0,1, 2}	which was written	Read Data is not equal	same address appears again.	
				(write & read) are cross-checked if an address		earlier to the same	to the Written Data at	You can check this using	
test_007	ra	andom_wr_rd_test	Pass	is shared between both operations.	HPROT=4b0001	address.	a specified address.	Simulation.	
					Apply clock,				
						DUT provides Okay			
					HWRITE = 1 and 0 (W/R),	Response (HRESP = 0) to			
					HRESET=1,	IDLE Transfers and waits			
				Tests DUT's Response upon inserting IDLE		for HREADY to be	1 '		
				Cycles and also performs a NONSEQ waited	HBURST=3'B000,	asserted to provide	Response to IDLE		
test_008	w	/aited_transfer_test	Pass	Write Transfer Operation	HPROT=4b0001	valid DATA.	Transfers.	Using Simulation	
					Apply clock,				
					HWRITE = 1 and 0 (W/R),			Write HWDATA on 4 different	
					HRESET=1,			addresses and then switch to	
					HSIZE= 3'd2	The HRDATA from DUT		Reading mode and repeat the	
					HBURST=3'b010,	on each address should		Reading process on each	
					HPROT=4b0001	be equal to the	HRDATA is not Equal to	address one by one and cross-	
				Performs a Wr/Rd BURST test where address	HREADY = 1	HWDATA written to that	HWDATA on particular	check with the reference	
test_009	w	rap4_burst_test.sv	Pass	is aligned on 16 Bytes Boundary.	HADDR = 0x38, 0x3C, 0x30, 0x34	particular address.	address.	model.	
_				Cycles and also performs a NONSEQ waited Write Transfer Operation  Performs a Wr/Rd BURST test where address	HPROT=4b0001  Apply clock,  HWRITE = 1 and 0 (W/R),  HRESET=1,  HSIZE= 3'd2  HBURST=3'b010,  HPROT=4b0001  HREADY = 1	asserted to provide valid DATA.  The HRDATA from DUT on each address should be equal to the HWDATA written to that	Transfers.  HRDATA is not Equal to HWDATA on particular	Write HWDATA on 4 different addresses and then switch to Reading mode and repeat the Reading process on each address one by one and crosscheck with the reference	

				Apply clock,  HWRITE = 1 and 0 (W/R),  HRESET=1,			Write HWDATA on 4 different addresses and then switch to	
				HSIZE= 3'd2 HBURST=3'b011, HPROT=4b0001	The HRDATA from DUT on each address should be equal to the	HRDATA is not Equal to	Reading mode and repeat the Reading process on each address one by one and cross-	
			Performs a Wr/Rd BURST test where address	HREADY = 1	HWDATA written to that	HWDATA on particular	check with the reference	
test_010	incr4_burst_test.sv	Pass	is incrementing in each beat.	HADDR = 0x38, 0x3C, 0x40, 0x44	particular address.	address.	model.	
			Charles the functionality of colories hit for		No read and write operation is done by	If clave newformer and		
tost 011	slave selection test sv	Dace	Checks the functionality of selection bit for HSEL	HSEL=0	slave. HRDATA is giving default value.	If slave performs any function.	Using simulation	
test_011	slave_selection_test.sv	Pass	NJEL	NSEL=0	default value.	Turiction.	Osing simulation	
	<u> </u> 							