

Module: SV for Verification**Section: Threads & Interprocess Communication Task: Events****Task 1 - [EDA Link](#)****Events****➤ Code:**

The code has some syntactical errors, after resolving the issues, the final code will look like as follows:

```
// Author: Noman Rafiq
// Dated: Sep 09, 2024

program automatic events;
event e1, e2;
task trigger(event local_event, input time wait_time);
    #wait_time;
    ->local_event;
endtask

initial begin
    fork
        trigger(e1, 10ns);
    begin
        wait(e1.triggered);
        $display("%0t: e1 triggered", $time);
    end
    join
end

initial begin
    fork
        trigger(e2, 20ns);
    begin
        wait(e2.triggered);
        $display("%0t: e2 triggered", $time);
    end
    join
end

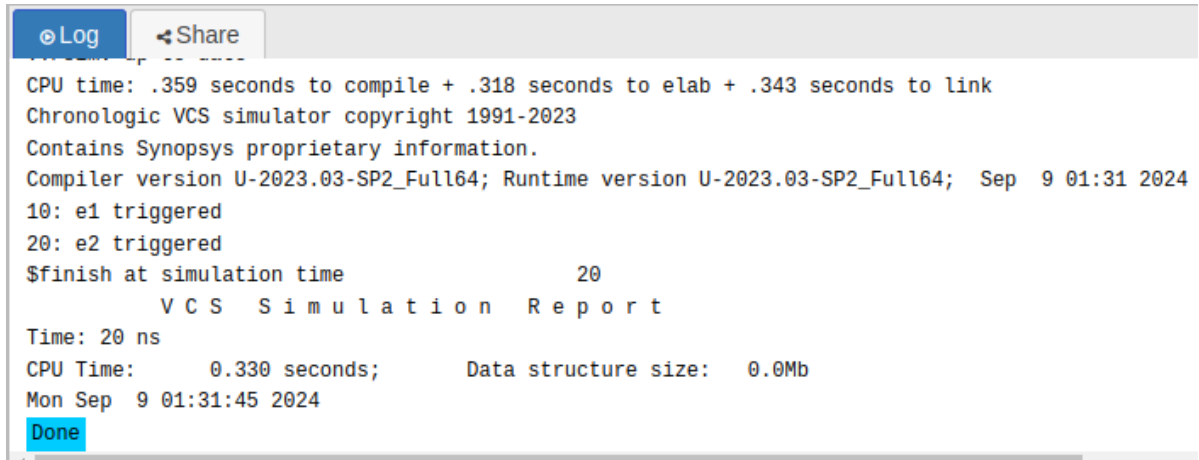
endprogram
```

➤ Expected Output:

This SystemVerilog code demonstrates the use of events and concurrent execution using the **fork-join** construct. Two events, **e1** and **e2**, are triggered after delays of 10ns and 20ns respectively, using the **trigger** task. The code waits for each event to be triggered before printing a message indicating the time at which the event occurred. The expected output would be that at 10ns, the

message for **e1** is printed, and at 20ns, the message for **e2** is printed, showing concurrent event handling and synchronization.

➤ **Actual Output:**



```
Log Share
-----
CPU time: .359 seconds to compile + .318 seconds to elab + .343 seconds to link
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03-SP2_Full64; Runtime version U-2023.03-SP2_Full64; Sep 9 01:31 2024
10: e1 triggered
20: e2 triggered
$finish at simulation time 20
VCS Simulation Report
Time: 20 ns
CPU Time: 0.330 seconds; Data structure size: 0.0Mb
Mon Sep 9 01:31:45 2024
Done
```