test id	hdd section	test name	test status	description or objective of test	stimulus geneation procedure	test passes when	test fails when	checking procedure	assertion description
test_001		reset_test	Pass	In the reset mode, transfer mode is changed to IDLE and nothing can be written or read unless reset is de-asserted.	Apply clock, HRESET=0	During Reset, Slave must ensure that HREADYOUT is HIGH and memory is initialized to provided known state.	HREADYOUT is not High and if Memory is not initialized.	Using Simulation **PS: Both the testbench and DUT Memories have been initialized to "DEADBEEF" upon reset. Hence, all the addresses will have the same word unless written something (upon de-assertion)**	
test_002		rd_test	Pass	Basic Read Data with no wait signal.	Apply clock, HTRANS=2b'10, HWRITE= 0, HRESET=1, HADDR= Address of Memory, HSIZE= inside {0,1, 2} HBURST=3B000, HPROT=4b0001	HRDATA gives the correct Data from the address with HRESP = 0 (OKAY SIGNAL)	HRDATA does not provide the correct data from the address	The testbench read the memory and compare the dummy Memory's output with DUT's output when stimulus is given to Scoreboard.	
test_003		wr_test	Pass	Basic Writing (Word Sized) Data to Memory without any wait states.	Apply clock, HTRANS=2b'10, HWRITE= 0, HRESET=1, HADDR= Address of Memory, HSIZE= inside {0,1, 2} HBURST=3B000, HPROT=4b0001	HWDATA is written on a memory at the given address	When HWDATA is not written in the memory correctly at the required address	Write the same DATA in the dummy memory at the same address. Then, read the value at the provided address of the original memory and compare with the dummy memory.	
test_004		word_wr_rd_test	Pass	It is an alternate **Word** Write/Read test with incrementing addresses. Firstly, an address is written to and then the value is read from the same address to cross-check if the values have been correctly written to DUT. Address is updated in the end so that we write to a different location next time.	Apply clock, HTRANS = 2'd2 HWRITE = 1 and 0 (W/R), HRESET=1, HADDR= Managed using rd_ptr and wr_ptr, HSIZE= 3'b010 HBURST=3B000, HPROT=4b0001	HRDATA gives DATA equal to the Value which was written earlier, to the same address.	Read Data is not equal to the Written Data at a specified address.	Write the HWDATA to some address and then check the HRDATA value at the same address in the next clock cycles to verify. You can check this using Simulation.	

test_005		halfword_wr_rd_test	Pass	It is an alternate **Halfword** Write/Read test with incrementing addresses. Firstly, an address is written to and then the value is read from the same address to cross-check if the values have been correctly written to DUT. Address is updated in the end so that we write to a different location next time.	Apply clock, HTRANS = 2'd2 HWRITE = 1 and 0 (W/R), HRESET=1, HADDR= Managed using rd_ptr and wr_ptr, HSIZE= 3'b001, HBURST=3B000, HPROT=4b0001	HRDATA gives DATA equal to the Value which was written earlier, to the same address.	Read Data is not equal to the Written Data at a specified address.	Write the HWDATA to some address and then check the HRDATA value at the same address in the next clock cycles to verify. You can check this using Simulation.	
test_006		byte_wr_rd_test	Pass	It is an alternate **Byte** Write/Read test with incrementing addresses. Firstly, an address is written to and then the value is read from the same address to cross-check if the values have been correctly written to DUT. Address is updated in the end so that we write to a different location next time.	Apply clock, HTRANS = 2'd2 HWRITE = 1 and 0 (W/R), HRESET=1, HADDR= Managed using rd_ptr and wr_ptr, HSIZE= 3'b000, HBURST=3B000, HPROT=4b0001	HRDATA gives DATA equal to the Value which was written earlier, to the same address.	Read Data is not equal to the Written Data at a specified address.	Write the HWDATA to some address and then check the HRDATA value at the same address in the next clock cycles to verify. You can check this using Simulation.	
test_007		random_wr_rd_test	Pass	It is a random Write/Read test with randomly generated addresses. Multiple W/R operations are performed and then values (write & read) are cross-checked if an address is shared between both operations.	Apply clock, HWRITE = 1 and 0 (W/R), HRESET=1, HSIZE= inside {0,1, 2} HBURST=3'B000, HPROT=4b0001	HRDATA gives DATA equal to the Value which was written earlier to the same address.	Read Data is not equal to the Written Data at a specified address.	Write the HWDATA to a random address and then check the HRDATA value if the same address appears again. You can check this using Simulation.	
test_008		waited_transfer_test	Pass	Tests DUT's Response upon inserting **IDLE** Cycles and also performs a NONSEQ **waited Write Transfer Operation**	Apply clock, HWRITE = 1 and 0 (W/R), HRESET=1, HSIZE= 3'd2 HBURST=3'B000, HPROT=4b0001	DUT provides Okay Response **(HRESP = 0)** to IDLE Transfers and waits for HREADY to be asserted to provide valid DATA.	DUT provides Error Response to IDLE Transfers.	Using Simulation	
test_009		wrap4_burst_test.sv	Pass	Performs a Wr/Rd BURST test where address is aligned on 16 Bytes Boundary.	Apply clock, HWRITE = 1 and 0 (W/R), HRESET=1, HSIZE= 3'd2 HBURST=3'b010, HPROT=4b0001 HREADY = 1 HADDR = 0x38, 0x3C, 0x30, 0x34	The HRDATA from DUT on each address should be equal to the HWDATA written to that particular address.	HRDATA is not Equal to HWDATA on particular address.	Write HWDATA on 4 different addresses and then switch to Reading mode and repeat the Reading process on each address one by one and cross-check with the reference model.	

test_010		incr4_burst_test.sv	Pass	Performs a Wr/Rd BURST test where address is incrementing in each beat.	Apply clock, HWRITE = 1 and 0 (W/R), HRESET=1, HSIZE= 3'd2 HBURST=3'b011, HPROT=4b0001 HREADY = 1 HADDR = 0x38, 0x3C, 0x40, 0x44	The HRDATA from DUT on each address should be equal to the HWDATA written to that particular address.	HRDATA is not Equal to HWDATA on particular address.	Write HWDATA on 4 different addresses and then switch to Reading mode and repeat the Reading process on each address one by one and cross-check with the reference model.	
test_011		slave_selection_test.sv	Pass	Checks the functionality of selection bit for HSEL	HSEL=0	No read and write operation is done by slave. HRDATA is giving default value.	If slave performs any function.	Using simulation	