

Verification Architecture for Ibex Core

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Agenda

- Introduction to Verification Architecture
- Interface Details
- Sanity Checks Implemented
- Test Cases Covered
- Summary and Q&A

Introduction to Verification Architecture

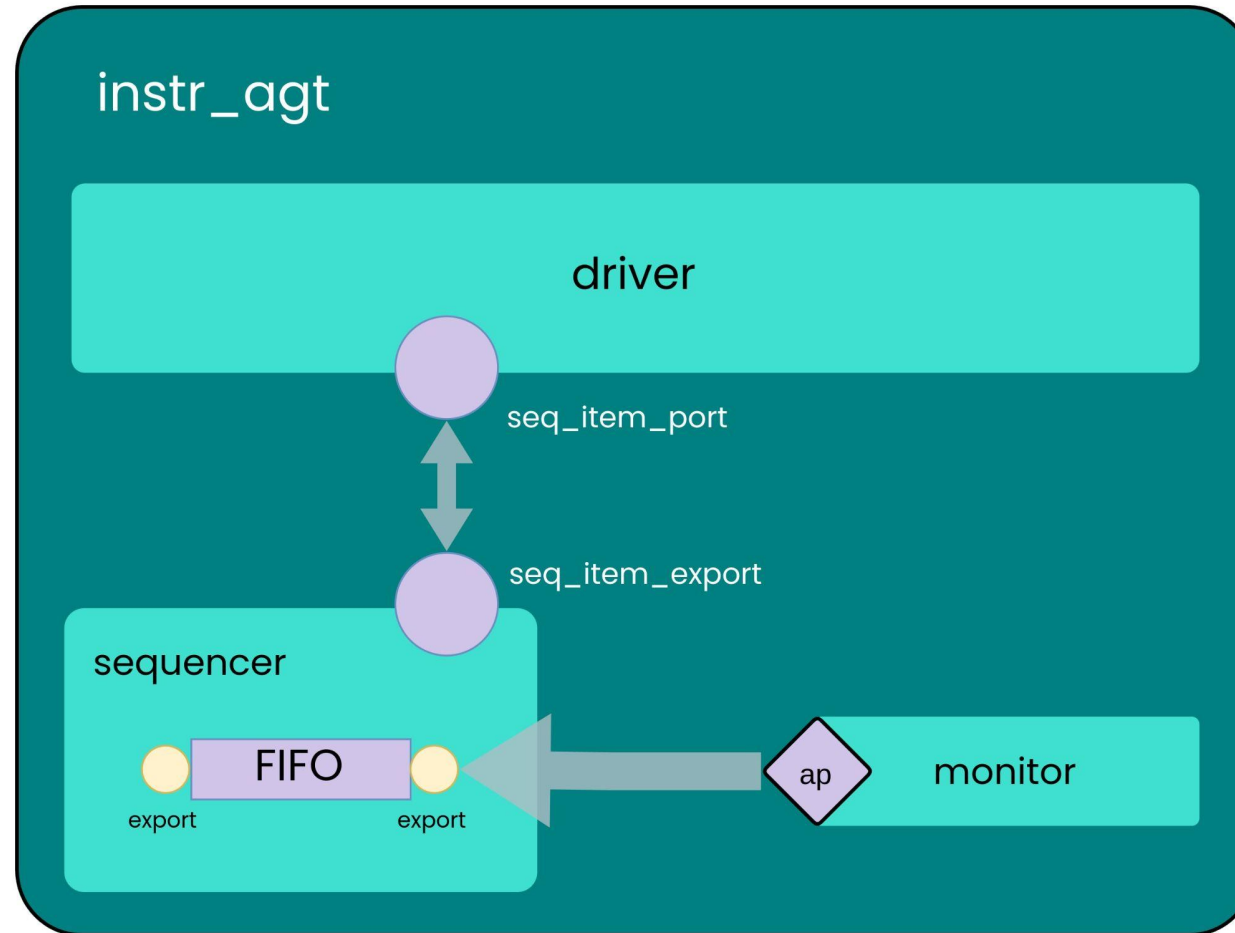
Key Interfaces

- **dut_probe_intf:** Monitors core status and controls fetch enable signals.
- **instr_mem_intf:** Manages fetch unit signals for instruction requests.
- **data_mem_intf:** Handles Load Store Unit (LSU) signals for data operations.

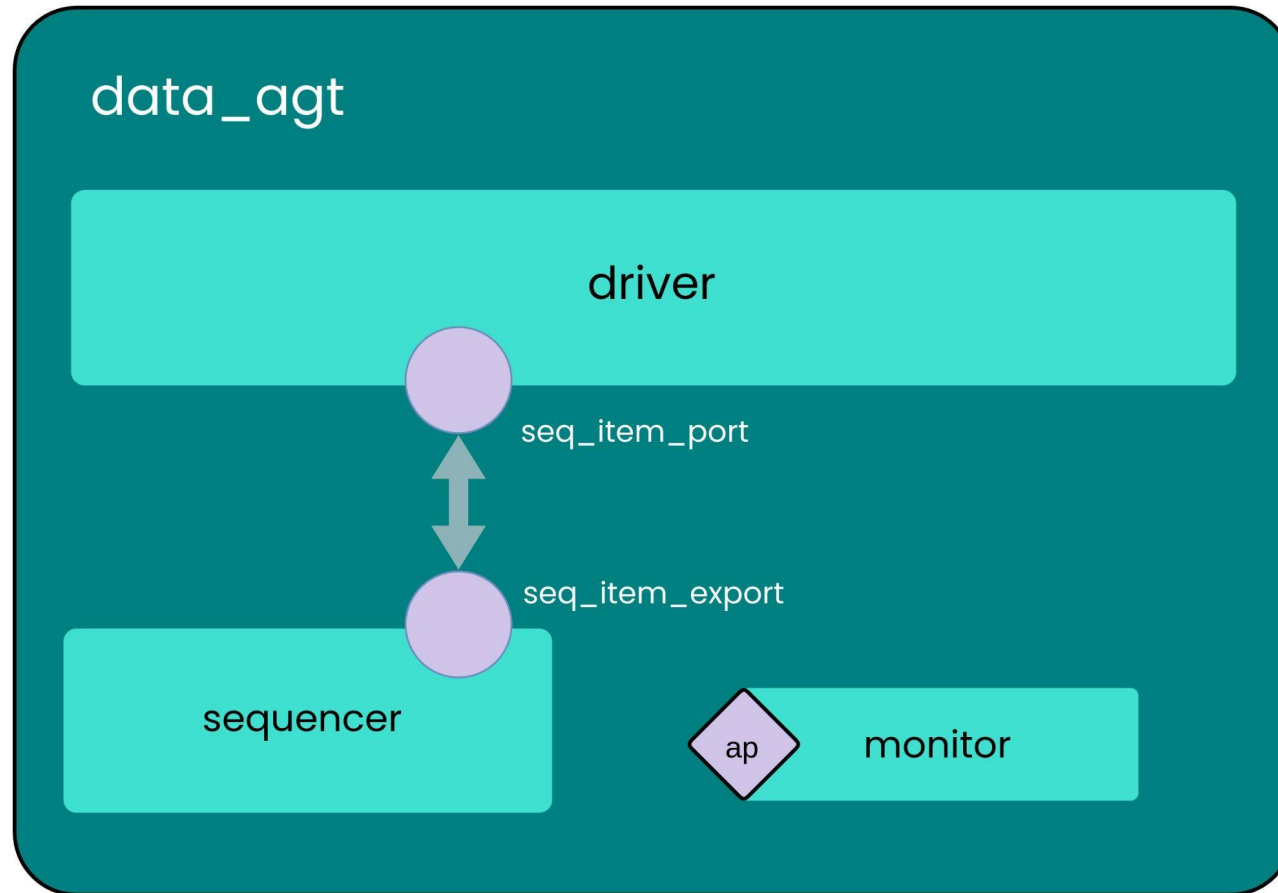
Memory Model

- Serves instruction and data requests.
- Fetch unit and LSU collaborate for instruction execution and load/store operations.

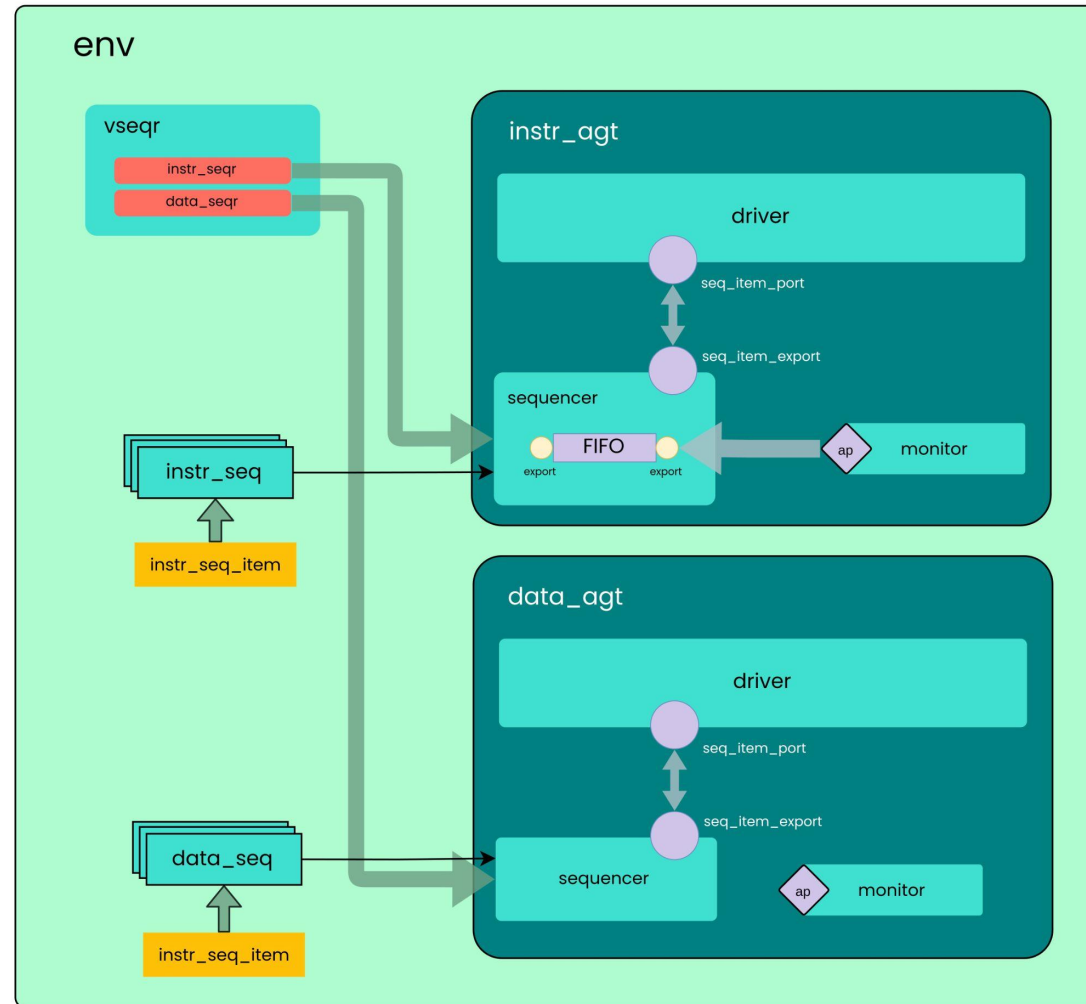
Instruction Agent



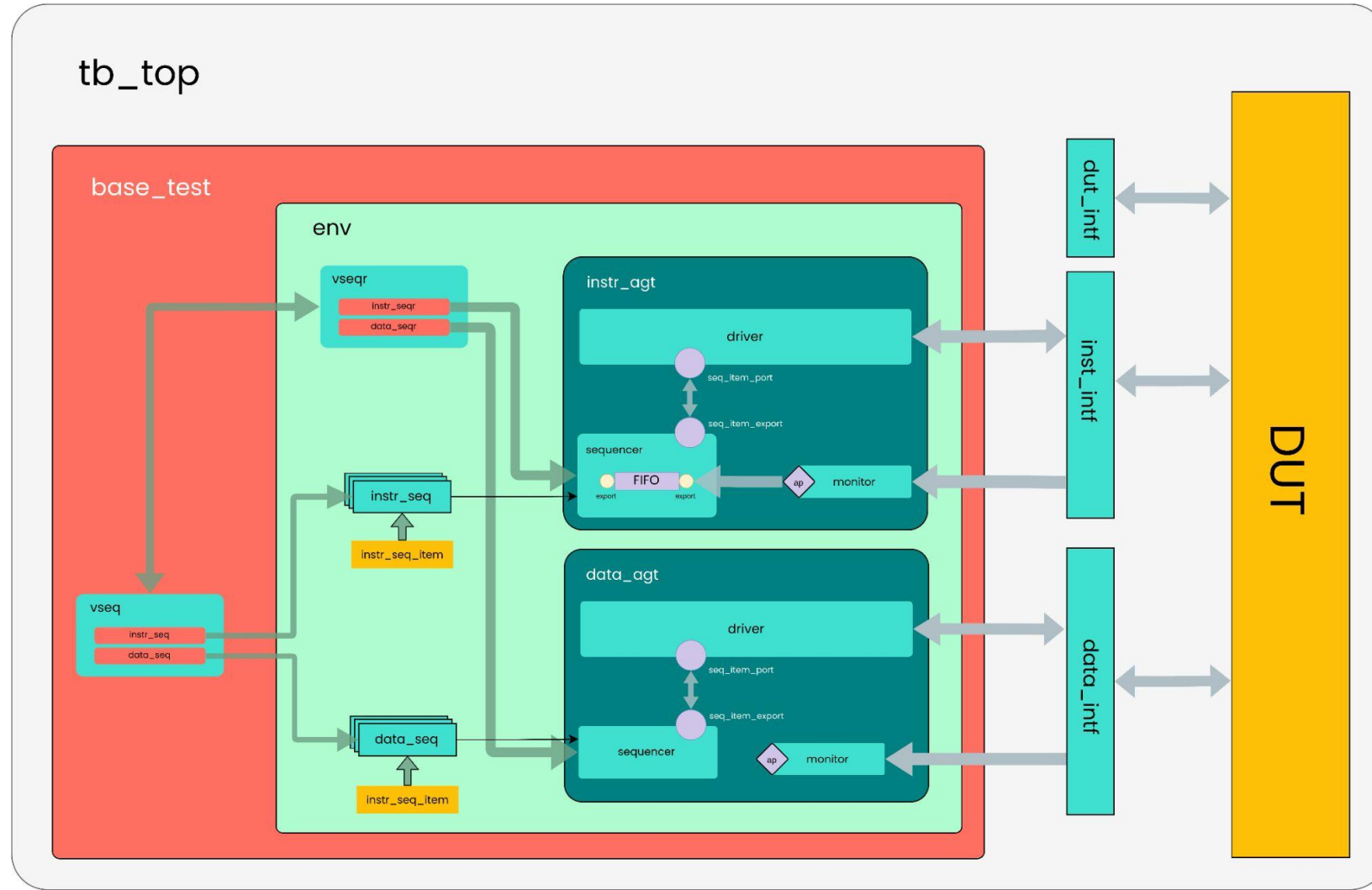
Data Agent



Environment



Top Module:



Interface Details

Instruction Interface:

- **Driver:** Reads transactions from the sequencer FIFO and drives signals to the DUT.
- **Monitor:** Observes DUT's instruction fetches and sends data to the analysis port.

Data Interface:

- **Driver:** Drives LSU-related signals using slave-sequence method.
- **Monitor:** Monitors load/store requests and forwards data to analysis components.

Sanity Checks

Sanity Checks:

- Ensures **fetch_enable** is functional.
- Verified correct instruction data retrieval using `core_trace.log`.
- Waveform confirms proper load/store transactions are driven and monitored.

Testcases Covered

Testcases:

Testcases (.bin)	
add	sb
sub	sh
xor	sw
or	beq
and	bne
sll	blt
srl	bge
sra	bltu
slt	jal
sltu	lui
addi	riscv_arithmetic_basic_test_0
xori	riscv_arithmetic_basic_test_1
ori	
lh	
lhu	
lw	

Thank you!