Module: UVM-1
Section: UVM Concepts **Task:** TLM

TLM
Task 2

➢ Task 1:

```
19  virtual task put(transaction trans);
20    // Add some Delay (Task 1)
21    #40;
22
23    `uvm_info(get_type_name(),$sformatf(" Received trans on IMP Port"),UVM_LOW)
24    `uvm_info(get_type_name(),$sformatf(" Printing trans, \n %s",trans.sprint()),UVM_LOW)
25  endtask
26
```

```
⊙Log   ◁Share

trans    transaction  -      @395
  addr   integral     4      'h9
  wr_rd  integral     1      'h0
  wdata  integral     8      'hf5
--------------------------------
UVM_INFO component_a.sv(28) @ 0: uvm_test_top.comp_a [component_a]  Before calling port put method
UVM_INFO component_b.sv(23) @ 40: uvm_test_top.comp_b [component_b]  Received trans on IMP Port
UVM_INFO component_b.sv(24) @ 40: uvm_test_top.comp_b [component_b]  Printing trans,
  --------------------------------
Name      Type         Size  Value
--------------------------------
trans     transaction  -      @395
  addr    integral     4      'h9
  wr_rd   integral     1      'h0
  wdata   integral     8      'hf5
--------------------------------
```

➢ Task 2:

```
⊙Log   ◁Share
    subComp_b   sub_comp_b_a            -    @406
    trans_end   uvm_blocking_put_imp    -    @415
    trans_mid   uvm_blocking_put_export -    @396
  comp_b_a      sub_comp_b_a            -    @377
    trans_end   uvm_blocking_put_imp    -    @386
--------------------------------
UVM_INFO component_a.sv(25) @ 0: uvm_test_top.comp_a [component_a]  tranaction randomized
--------------------------------
Name    Type         Size  Value
--------------------------------
trans    transaction  -    @433
  addr   integral     4    'h9
  wr_rd  integral     1    'h0
  wdata  integral     8    'hf5
--------------------------------
UVM_INFO component_a.sv(28) @ 0: uvm_test_top.comp_a [component_a]  Before calling port put method
UVM_INFO sub_comp_b_a.sv(24) @ 0: uvm_test_top.comp_b.subComp_b [sub_comp_b_a]  Received trans on IMP Port
UVM_INFO sub_comp_b_a.sv(25) @ 0: uvm_test_top.comp_b.subComp_b [sub_comp_b_a]  Printing trans,
  --------------------------------
Name    Type         Size  Value
--------------------------------
trans    transaction  -    @433
  addr   integral     4    'h9
  wr_rd  integral     1    'h0
  wdata  integral     8    'hf5
--------------------------------

UVM_INFO component_a.sv(30) @ 0: uvm_test_top.comp_a [component_a]  After  calling port put method
UVM_INFO /apps/vcsmx/vcs/U-2023.03-SP2//etc/uvm-1.2/src/base/uvm_objection.svh(1276) @ 0: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO /apps/vcsmx/vcs/U-2023.03-SP2//etc/uvm-1.2/src/base/uvm_report_server.svh(904) @ 0: reporter [UVM/REPORT/SERVER]
--- UVM Report Summary ---
```

➢ **Task 3:**

```
--------------------------------
Name      Type        Size  Value
--------------------------------
trans     transaction  -     @444
  addr    integral    4     'h9
  wr_rd   integral    1     'h0
  wdata   integral    8     'hf5
--------------------------------
UVM_INFO component_a.sv(28) @ 0: uvm_test_top.comp_a [component_a]  Before calling port put method
UVM_INFO component_a.sv(30) @ 0: uvm_test_top.comp_a [component_a]  After  calling port put method
UVM_INFO component_b.sv(24) @ 0: uvm_test_top.comp_b [component_b]  Received Transaction from FIFO
--------------------------------
Name      Type        Size  Value
--------------------------------
trans     transaction  -     @444
  addr    integral    4     'h9
  wr_rd   integral    1     'h0
  wdata   integral    8     'hf5
--------------------------------
UVM_INFO /apps/vcsmx/vcs/U-2023.03-SP2//etc/uvm-1.2/src/base/uvm_objection.svh(1276) @ 0: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO /apps/vcsmx/vcs/U-2023.03-SP2//etc/uvm-1.2/src/base/uvm_report_server.svh(904) @ 0: reporter [UVM/REPORT/SERVER]
--- UVM Report Summary ---

** Report counts by severity
UVM_INFO :    7
UVM_WARNING :    0
UVM_ERROR :    0
UVM_FATAL :    0
** Report counts by id
[RNTST]     1
[TEST_DONE]    1
[UVM/RELNOTES]    1
[component_a]    3
[component_b]    1
```