Module: UVM-1
Guide for testing IBEX Soc

Guide for using UVM Testbench
IBEX Core

➢ **Introduction:**

This guide will walk you through the steps required to test different RISC-V assembly programs using the IBEX core. Follow the steps carefully to ensure proper setup and execution.

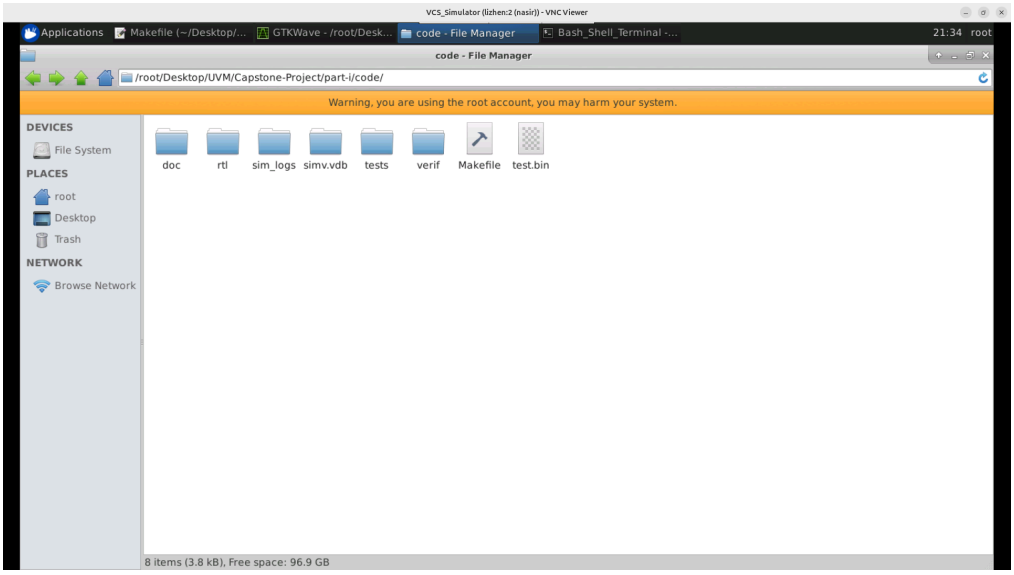
Step 1: Download the Required Files

1. Download the “**code.tar.xz**” files provided.
2. Ensure the download is complete and the files are not corrupted.

Step 2: Extract the Files

1. Locate the downloaded “**code.tar.xz**” file in your system.
2. Extract the contents of the tar file to the appropriate path.

3. Verify that the files are correctly extracted to the specified directory. A screenshot is attached for reference.



Step 3: Navigate to the Parent Directory

1. Navigate into the “home Directory of the downloaded files”.

```
cd /path-to-code-directory/
```

2. Open a terminal in this “code” directory to prepare for the next steps.

Step 4: Run the Make Command for Compilation
1. In the terminal, enter the following command to test a specific RISC-V binary file:

```
make tb-compile
```

```
root@lizhen:~/Desktop/UVM/Capstone-Project/part-i/code# make tb-compile
mkdir -p out/
mkdir -p out/seed-2412022147
mkdir -p out/seed-2412022147/INCA_libs
mkdir -p out/seed-2412022147/test
vcs \
        -sverilog \
        -ntb_opts uvm-1.2 \
        -debug_access+all \
        -cm line+cond+tgl+branch+assert \
        verif/bus_params_pkg.sv \
        verif/riscv_signature_pkg.sv \
        verif/mem_model_pkg.sv \
        +incdir+verif \
        verif/instr_mem_intf.sv \
        verif/data_mem_intf.sv \
        verif/UVCs/instr_UVC/instr_mem_pkg.sv \
        +incdir+verif/UVCs/instr_UVC \
        verif/UVCs/data_UVC/data_mem_pkg.sv \
        +incdir+verif/UVCs/data_UVC \
        +incdir+verif/UVCs/env_UVC \
        rtl/ibex_top_tracing.sv \
        +incdir+rtl \
        verif/tb_top.sv \
        +incdir+verif
                        Chronologic VCS (TM)
         Version L-2016.06_Full64 -- Mon Dec  2 21:47:45 2024
               Copyright (c) 1991-2016 by Synopsys Inc.
                        ALL RIGHTS RESERVED
```

Step 5: Run Make Sim Command for Simulation
In the terminal, enter the following command to start simulation:

```
make sim +bin=$path-to-binary-file
```

Please note that the path-to-binary-files has to be provided via common-line to test a specific program. In our environment, the binaries are located inside “**tests**” directory.

For instance, if we want to test a randomly generated assembly test. The ***make sim*** command will look like this:

```
make sim +bin=tests/asm_tests/riscv_arithmetic_basic_test_0.bin
+UVM_TIMEOUT=99999999999,NO
```

For randomly generated tests, we need to add a maximum **UVM_TIMEOUT** so that the simulator doesn't stop our simulation.

Step 6: Testcase Legend

Refer to the legend below for the appropriate binary names to use in the "**+bin=**" field:

Testcases (.bin)	
add	sb
sub	sh
xor	sw
or	beq
and	bne
sll	blt
srl	bge
sra	bltu
slt	jal
sltu	lui
addi	riscv_arithmetic_basic_test_0
xori	riscv_arithmetic_basic_test_1
ori	
lh	
lhu	
lw	

Final Notes:

Follow these steps closely, and you'll be able to test various RISC-V binaries effectively.