Module: UVM-2
Project

Project - Source Code (V1.1 to V1.2)

➢ Control Sequence:

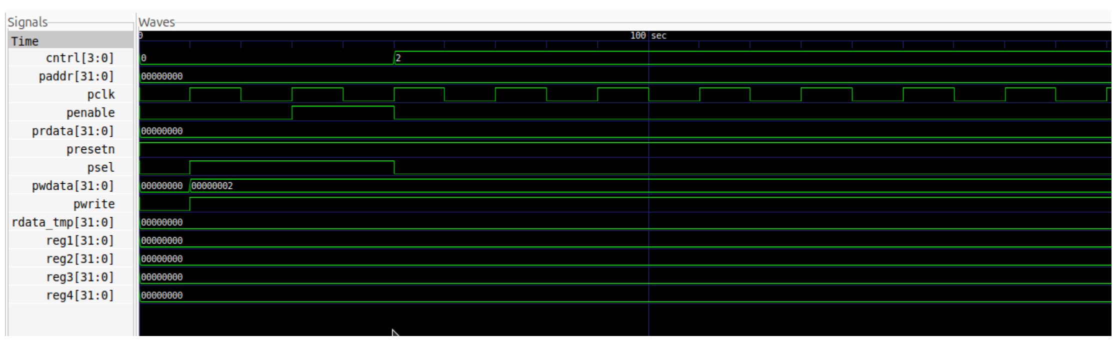
ctrl_wr

b. Checking Desired Value with get( ):

- **Console Output:**

```
UVM_INFO @ 0: reporter [RNTST] Running test test...
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO project.sv(127) @ 30: uvm_test_top.env.agent_inst.d [DRV] Mode : Write WDATA : 2 ADDR : 0
UVM_INFO project.sv(532) @ 50: uvm_test_top.env.agent_inst.seqr@@cwr [WRITE]  Desired Value = 2, Mirrored Value = 0
UVM_INFO project.sv(207) @ 70: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 2 ADDR : 0
UVM_INFO project.sv(241) @ 70: uvm_test_top.env.s [SCO] DATA Stored Addr : 0 Data :2
----------------------------------------------------------------
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_objection.svh(1270) @ 250: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_report_server.svh(894) @ 250: reporter [UVM/REPORT/SERVER]
--- UVM Report Summary ---

** Report counts by severity
UVM_INFO :   13
UVM_WARNING :    0
UVM_ERROR :    0
UVM_FATAL :    0
** Report counts by id
[DRV]     1
[MON]     1
[RNTST]     1
[SCO]     1
[TEST_DONE]     1
[UVM/CONFIGDB/SPELLCHK]     6
[UVM/RELNOTES]     1
[WRITE]     1

$finish called from file "/usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_root.svh", line 527.
$finish at simulation time                  250
           V C S   S i m u l a t i o n   R e p o r t
```

- **Waveform:**

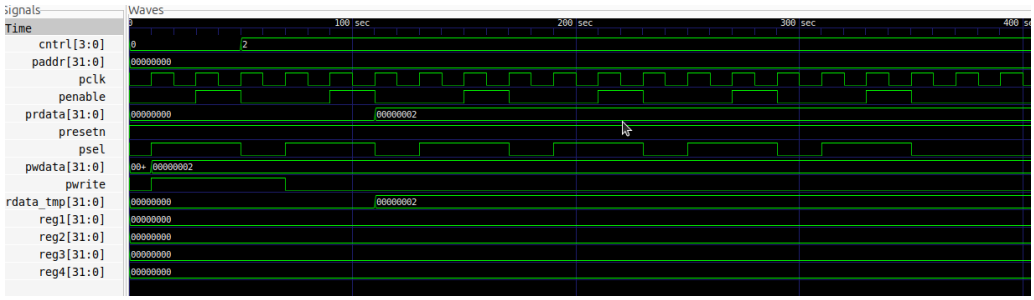


c. Setting Desired Value with set( ):

- **Console Output:**

```
l_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] inc
l_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] inc
l_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] inc
RV] Mode : Write WDATA : 2 ADDR : 0
@@cwr [WRITE]  Desired Value = 2, Mirrored Value = 0
@@cwr [SET::15]  Desired Value = 15, Mirrored Value = 0
ON] Mode : Write WDATA : 2 ADDR : 0
ored Addr : 0 Data :2
-
RV] Mode : Read WDATA : 2 ADDR : 0 RDATA : 0
```

- **Waveform:**

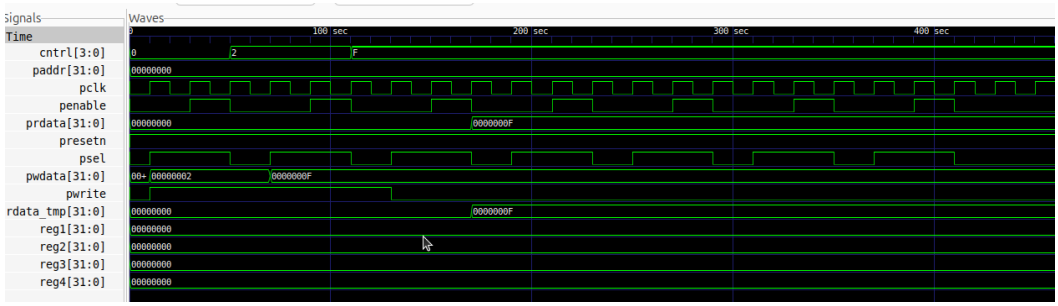


d. Writing Desired Value to DUT with update( ):

- **Console Output:**

```
nv.agent_inst.m [MON] Mode : Write WDATA : 2 ADDR : 0
nv.s [SCO] DATA Stored Addr : 0 Data :2
-----------------
nv.agent_inst.d [DRV] Mode : Write WDATA : 15 ADDR : 0
env.agent_inst.seqr@@cwr [UPDATE()]  Desired Value = 2, Mirrored Value = 2
env.agent_inst.m [MON] Mode : Write WDATA : 15 ADDR : 0
env.s [SCO] DATA Stored Addr : 0 Data :15
-----------------
env.agent_inst.d [DRV] Mode : Read WDATA : 15 ADDR : 0 RDATA : 0
```

- **Waveform:**



f. Purpose of each method:

- **get( ):** Retrieves the desired value of the register from the UVM register model. This value reflects what the testbench expects, not necessarily the actual value in the DUT.

- **set( ):** Sets the desired value field of the register in the UVM model. It does not directly affect the DUT but prepares the model for updates or checks.

- **update ( ):** Writes the desired value from the UVM model to the DUT register, ensuring the DUT reflects the intended state defined by the testbench.

f. Code:

```
class ctrl_wr extends uvm_sequence;
`uvm_object_utils(ctrl_wr)

 reg_block regmodel;
function new (string name = "ctrl_wr");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] wdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

     wdata = $urandom();

     regmodel.cntrl_inst.write(status, wdata);
     // Check 'dv' and 'mv' Values
                  dv = regmodel.cntrl_inst.get();             // Get Desired Value
                  mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("WRITE", $sformatf(" Desired Value = %0d, Mirrored Value = %0d ", dv, mv),
UVM_NONE)

     // Set the Desired value
     regmodel.cntrl_inst.set(15);                // Set the Value to be 15
     // Check again
                  dv = regmodel.cntrl_inst.get();             // Get Desired Value
                  mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("SET::15", $sformatf(" Desired Value = %0d, Mirrored Value = %0d ", dv, mv),
UVM_NONE)

     // Update the Value to DUT
     regmodel.cntrl_inst.update(status);          // Write the Value to DUT
     // Check again
                  dv = regmodel.cntrl_inst.get();              // Get Desired Value
                  mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("UPDATE()", $sformatf(" Desired Value = %0d, Mirrored Value = %0d ", dv,
mv), UVM_NONE)
 endtask
endclass
```

➢ **Predict( ) method:**

a. Difference between predict( ) & mirror( ):

Predict Method:

- **Purpose:** Updates the mirrored value of a register in the UVM register model based on observed activity on the DUT.
- **Trigger:** Typically called by monitors or predictors when a register operation (read/write) is detected on the bus.
- **Behavior:** It does not initiate any physical access; it simply reflects the updated state of the register.
- **Use Case:** A predictor observes a write operation to a register and uses **`predict`** to update the mirrored value accordingly.

Mirror Method:

- **Purpose:** Compares or synchronizes the mirrored value in the UVM register model with the actual value in the DUT.
- **Trigger:** Can initiate a physical access (read) to retrieve the DUT's current value and update the mirrored value.
- **Behavior:** Provides the option to verify whether the mirrored value and the DUT value are consistent.
- **Use Case:** Verifying that the current state of the register in the DUT matches the expected mirrored value.

Summary:

- **`predict`:** Passive, updates the UVM model without DUT access.
- **`mirror`:** Active, ensures consistency between the UVM model and the DUT.

e. Write(4’h5) and Predict(4’h3):

Output:

```
tc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_c
tc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_c
_top.env.agent_inst.d [DRV] Mode : Write WDATA : 5 ADDR : 0
_top.env.agent_inst.seqr@@cwr [WRITE::5]  Desired Value = 5, Mirrored Value = 0
_top.env.agent_inst.seqr@@cwr [PREDICT::3]  Desired Value = 3, Mirrored Value = 3
_top.env.agent_inst.m [MON] Mode : Write WDATA : 5 ADDR : 0
_top.env.s [SCO] DATA Stored Addr : 0 Data :5
------------------------
```

f. Mirror(UVM_CHECK):

Output:

```
UVM_INFO project.sv(127) @ 30: uvm_test_top.env.agent_inst.d [DRV] Mode : Write WDATA : 5 ADDR : 0
UVM_INFO project.sv(535) @ 50: uvm_test_top.env.agent_inst.seqr@@cwr [WRITE::5]  Desired Value = 5, Mirrored Value = 0
UVM_INFO project.sv(541) @ 50: uvm_test_top.env.agent_inst.seqr@@cwr [PREDICT::3]  Desired Value = 3, Mirrored Value = 3
UVM_INFO project.sv(207) @ 70: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 5 ADDR : 0
UVM_INFO project.sv(241) @ 70: uvm_test_top.env.s [SCO] DATA Stored Addr : 0 Data :5
----------------------------------------------------------------
UVM_INFO project.sv(141) @ 90: uvm_test_top.env.agent_inst.d [DRV] Mode : Read WDATA : 5 ADDR : 0 RDATA : 0
UVM_ERROR /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/reg/uvm_reg.svh(3042) @ 110: reporter [RegModel] Register "regmodel.cntrl_inst" value read from DUT (0x0000000000000000) does not mat
ch mirrored value (0x0000000000000003)
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/reg/uvm_reg.svh(3055) @ 110: reporter [RegModel] Field cntrl (regmodel.cntrl_inst[3:0]) mismatch read=4'h0 mirrored=4'h3
UVM_INFO project.sv(547) @ 110: uvm_test_top.env.agent_inst.seqr@@cwr [MIRROR]  Desired Value = 5, Mirrored Value = 5
UVM_INFO project.sv(213) @ 130: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(249) @ 130: uvm_test_top.env.s [SCO] Test Passed -> Addr : 0 Data :5
----------------------------------------------------------------
UVM_INFO project.sv(141) @ 150: uvm_test_top.env.agent_inst.d [DRV] Mode : Read WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(213) @ 190: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(249) @ 190: uvm_test_top.env.s [SCO] Test Passed -> Addr : 0 Data :5
----------------------------------------------------------------
UVM_INFO project.sv(141) @ 210: uvm_test_top.env.agent_inst.d [DRV] Mode : Read WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(213) @ 250: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(249) @ 250: uvm_test_top.env.s [SCO] Test Passed -> Addr : 0 Data :5
----------------------------------------------------------------
UVM_INFO project.sv(141) @ 270: uvm_test_top.env.agent_inst.d [DRV] Mode : Read WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(213) @ 310: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(249) @ 310: uvm_test_top.env.s [SCO] Test Passed -> Addr : 0 Data :5
----------------------------------------------------------------
UVM_INFO project.sv(141) @ 330: uvm_test_top.env.agent_inst.d [DRV] Mode : Read WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(213) @ 370: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(249) @ 370: uvm_test_top.env.s [SCO] Test Passed -> Addr : 0 Data :5
----------------------------------------------------------------
UVM_INFO project.sv(141) @ 390: uvm_test_top.env.agent_inst.d [DRV] Mode : Read WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(213) @ 430: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 5 ADDR : 0 RDATA : 5
UVM_INFO project.sv(249) @ 430: uvm_test_top.env.s [SCO] Test Passed -> Addr : 0 Data :5
----------------------------------------------------------------
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_objection.svh(1270) @ 610: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_report_server.svh(894) @ 610: reporter [UVM/REPORT/SERVER]
--- UVM Report Summary ---
```

The error occurs because the predicted value in the UVM model was set to **`4'h3`**, without reflecting the actual state of the register inside the DUT. When the **`mirror()`** method is called, it reads the current value from the DUT's register and compares it to the mirrored value in the UVM model using the **`UVM_CHECK`** option. If a mismatch is detected between the DUT value and the mirrored value, **`UVM_CHECK`** reports an error. After reporting the error, the mirrored value in the UVM model is updated to match the DUT's register value.

g. Observation:

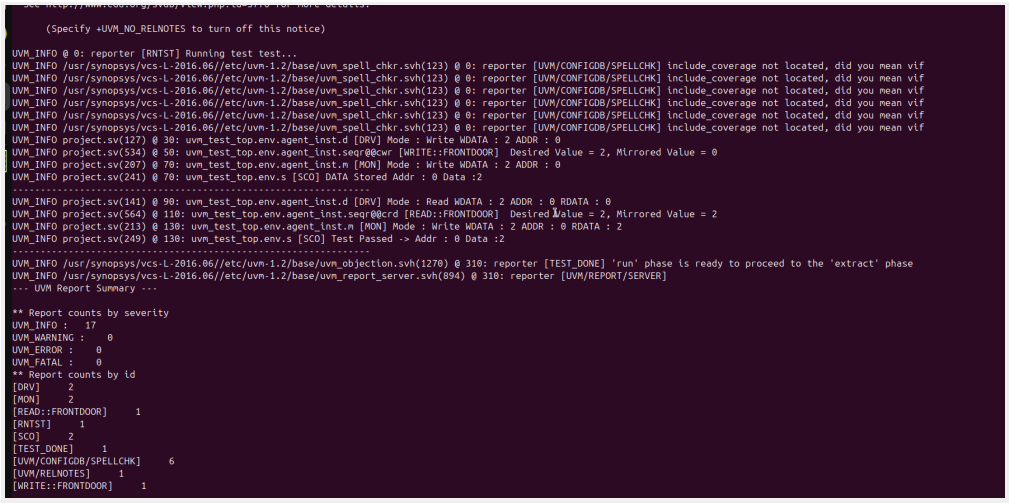
First, a constant value of **`4'h5`** is written to the DUT using the **`write()`** method. Next, the predicted value in the UVM model is set to **`4'h3`**, which updates the mirrored value field in the model. When the **`mirror()`** method is invoked with the **`UVM_CHECK`** option, it detects a mismatch between the mirrored value in the model and the actual value in the DUT.

This mismatch triggers an error report. After reporting the error, the **`mirror()`** method updates the mirrored value in the UVM model to match the actual value in the DUT.

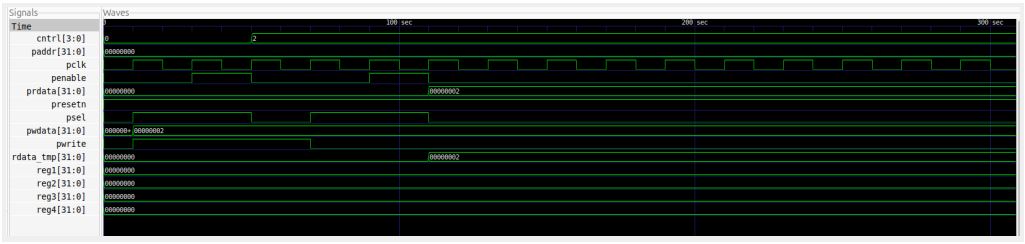
➢ FRONT_DOOR Access:

a. FRONTDOOR Wr/Rd using ctrl_wr and ctrl_rd Sequences:

- **Output:**



- **Waveform:**



- **Code:**

```
//////////////////// WRITE Sequence ////////////////////////////
class ctrl_wr extends uvm_sequence;
`uvm_object_utils(ctrl_wr)

 reg_block regmodel;
function new (string name = "ctrl_wr");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] wdata;
```

```
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

     wdata = $urandom();

     regmodel.cntrl_inst.write(status, wdata, UVM_FRONTDOOR);

     //Check 'dv' and 'mv' Values
                dv = regmodel.cntrl_inst.get();                         //
Get Desired Value
                mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("WRITE::FRONTDOOR", $sformatf(" Desired Value = %0d,
Mirrored Value = %0d ", dv, mv), UVM_NONE)

 endtask
endclass

//////////////////// READ Sequence ////////////////////////////
class ctrl_rd extends uvm_sequence;
`uvm_object_utils(ctrl_rd)

 reg_block regmodel;

function new (string name = "ctrl_rd");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] rdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

   //////working with control
   regmodel.cntrl_inst.read(status, rdata, UVM_FRONTDOOR);

     //Check 'dv' and 'mv' Values
                dv = regmodel.cntrl_inst.get();                         //
Get Desired Value
                mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("READ::FRONTDOOR", $sformatf(" Desired Value = %0d,
Mirrored Value = %0d ", dv, mv), UVM_NONE)

 endtask


endclass
```

➢ **BACKDOOR Access:**

a. Backdoor Access in UVM:

Backdoor access allows direct interaction with DUT signals using the simulator's database, bypassing the bus protocol. Write operations deposit values directly onto register signals, and read operations sample their current values. While this method avoids triggering control logic connected to the bus, it enables efficient signal manipulation without interfering with design transitions.

Benefits

- ➢ Backdoor access takes zero simulation time, as it avoids bus transactions.
- ➢ Useful for quickly verifying or initializing specific register states.
- ➢ Speeds up verification by complementing the standard frontdoor protocol checks.

b. HDL Paths:

- **Code:**

```
////////////////////////////////////////////////////////////////
//
// HDL Path for BACKDOOR ACCESS
//
add_hdl_path("dut");
cntrl_inst.add_hdl_path_slice ( "cntrl",      // Name of the Physical Register in DUT
                                0,            // lsb position
                                4             // size = 4 bits
                              );
// reg1
reg1_inst.add_hdl_path_slice  ( "reg1",       // Name of the Physical Register in DUT
                                0,            // lsb position
                                32            // size = 32 bits
                              );

// reg2
reg2_inst.add_hdl_path_slice  ( "reg2",       // Name of the Physical Register in DUT
                                0,            // lsb position
                                32            // size = 32 bits
                              );

// reg3
reg3_inst.add_hdl_path_slice  ( "reg3",       // Name of the Physical Register in DUT
                                0,            // lsb position
                                32            // size = 32 bits
                              );

// reg4
reg4_inst.add_hdl_path_slice  ( "reg4",       // Name of the Physical Register in DUT
                                0,            // lsb position
                                32            // size = 32 bits
                              );
```

c. BACKDOOR WRITE:

- **Output:**

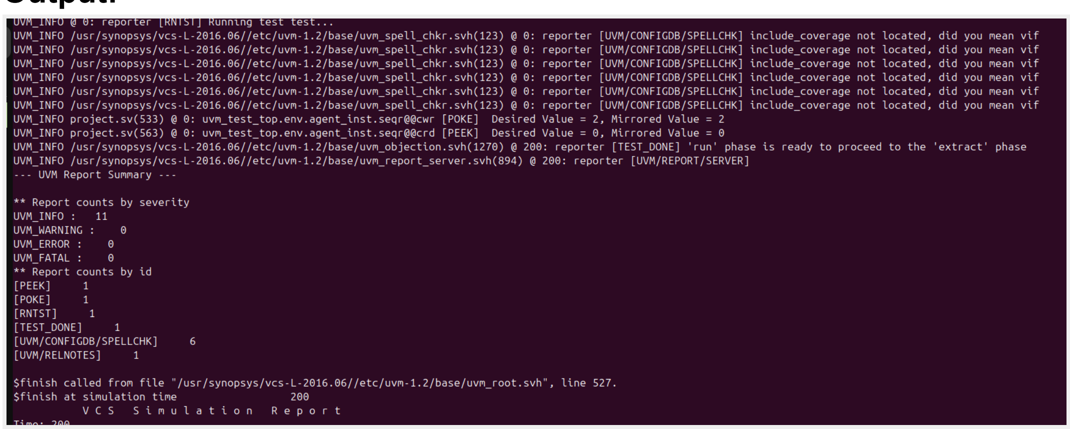
```
      (Specify +UVM_NO_RELNOTES to turn off this notice)

UVM_INFO @ 0: reporter [RNTST] Running test test...
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO project.sv(533) @ 0: uvm_test_top.env.agent_inst.seqr@@cwr [WRITE::BACKDOOR]  Desired Value = 2, Mirrored Value = 2
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_objection.svh(1270) @ 200: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_report_server.svh(894) @ 200: reporter [UVM/REPORT/SERVER]
--- UVM Report Summary ---

** Report counts by severity
UVM_INFO :   10
UVM_WARNING :    0
UVM_ERROR :    0
UVM_FATAL :    0
** Report counts by id
[RNTST]     1
[TEST_DONE]     1
[UVM/CONFIGDB/SPELLCHK]     6
[UVM/RELNOTES]     1
[WRITE::BACKDOOR]     1

$finish called from file "/usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_root.svh", line 527.
$finish at simulation time                 200
           V C S   S i m u l a t i o n   R e p o r t
Time: 200
```

- **Code:**

```
class ctrl_wr extends uvm_sequence;
`uvm_object_utils(ctrl_wr)

 reg_block regmodel;
function new (string name = "ctrl_wr");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] wdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

     wdata = $urandom();

     regmodel.cntrl_inst.write(status, wdata, UVM_BACKDOOR);

     //Check 'dv' and 'mv' Values
              dv = regmodel.cntrl_inst.get();
// Get Desired Value
              mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("WRITE::BACKDOOR", $sformatf(" Desired Value =
%0d, Mirrored Value = %0d ", dv, mv), UVM_NONE)

 endtask
endclass
```

d. Peek/Poke Methods:

- **Output:**



```
UVM_INFO @ 0: reporter [RNTST] Running test test...
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO project.sv(533) @ 0: uvm_test_top.env.agent_inst.seqr@@cwr [POKE]  Desired Value = 2, Mirrored Value = 2
UVM_INFO project.sv(563) @ 0: uvm_test_top.env.agent_inst.seqr@@crd [PEEK]  Desired Value = 0, Mirrored Value = 0
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_objection.svh(1270) @ 200: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_report_server.svh(894) @ 200: reporter [UVM/REPORT/SERVER]
--- UVM Report Summary ---

** Report counts by severity
UVM_INFO :   11
UVM_WARNING :    0
UVM_ERROR :    0
UVM_FATAL :    0
** Report counts by id
[PEEK]     1
[POKE]     1
[RNTST]     1
[TEST_DONE]     1
[UVM/CONFIGDB/SPELLCHK]     6
[UVM/RELNOTES]     1

$finish called from file "/usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_root.svh", line 527.
$finish at simulation time                 200
           V C S   S i m u l a t i o n   R e p o r t
Time: 200
```

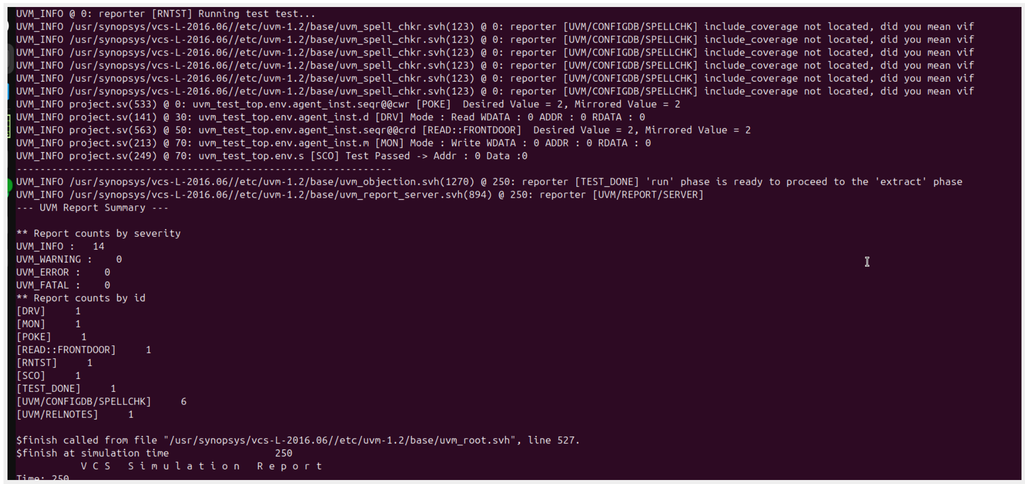
- **Code:**

```
class ctrl_wr extends uvm_sequence;
```

```
`uvm_object_utils(ctrl_wr)

 reg_block regmodel;
function new (string name = "ctrl_wr");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] wdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

     wdata = $urandom();

     regmodel.cntrl_inst.poke(status, wdata);

     //Check 'dv' and 'mv' Values
               dv = regmodel.cntrl_inst.get();
// Get Desired Value
               mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("POKE", $sformatf(" Desired Value = %0d, Mirrored
Value = %0d ", dv, mv), UVM_NONE)

 endtask
endclass


////////////////////////////////////////////////////////////////
/////////
//////////////////read data from control reg


class ctrl_rd extends uvm_sequence;
`uvm_object_utils(ctrl_rd)

 reg_block regmodel;

function new (string name = "ctrl_rd");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] rdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

   //////working with control
   regmodel.cntrl_inst.peek(status, rdata);

     //Check 'dv' and 'mv' Values
               dv = regmodel.cntrl_inst.get();
// Get Desired Value
               mv = regmodel.cntrl_inst.get_mirrored_value();
```

e. Poke & FRONTDOOR READ:

- **Output:**



```
UVM_INFO @ 0: reporter [RNTST] Running test test...
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_spell_chkr.svh(123) @ 0: reporter [UVM/CONFIGDB/SPELLCHK] include_coverage not located, did you mean vif
UVM_INFO project.sv(533) @ 0: uvm_test_top.env.agent_inst.seqr@@cwr [POKE]  Desired Value = 2, Mirrored Value = 2
UVM_INFO project.sv(141) @ 30: uvm_test_top.env.agent_inst.d [DRV] Mode : Read WDATA : 0 ADDR : 0 RDATA : 0
UVM_INFO project.sv(563) @ 50: uvm_test_top.env.agent_inst.seqr@@crd [READ::FRONTDOOR]  Desired Value = 2, Mirrored Value = 2
UVM_INFO project.sv(213) @ 70: uvm_test_top.env.agent_inst.m [MON] Mode : Write WDATA : 0 ADDR : 0 RDATA : 0
UVM_INFO project.sv(249) @ 70: uvm_test_top.env.s [SCO] Test Passed -> Addr : 0 Data :0
----------------------------------------------------------------
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_objection.svh(1270) @ 250: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
UVM_INFO /usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_report_server.svh(894) @ 250: reporter [UVM/REPORT/SERVER]
--- UVM Report Summary ---

** Report counts by severity
UVM_INFO :   14
UVM_WARNING :    0
UVM_ERROR :    0
UVM_FATAL :    0
** Report counts by id
[DRV]     1
[MON]     1
[POKE]     1
[READ::FRONTDOOR]     1
[RNTST]     1
[SCO]     1
[TEST_DONE]     1
[UVM/CONFIGDB/SPELLCHK]     6
[UVM/RELNOTES]     1

$finish called from file "/usr/synopsys/vcs-L-2016.06//etc/uvm-1.2/base/uvm_root.svh", line 527.
$finish at simulation time                 250
           V C S   S i m u l a t i o n   R e p o r t
Time: 250
```

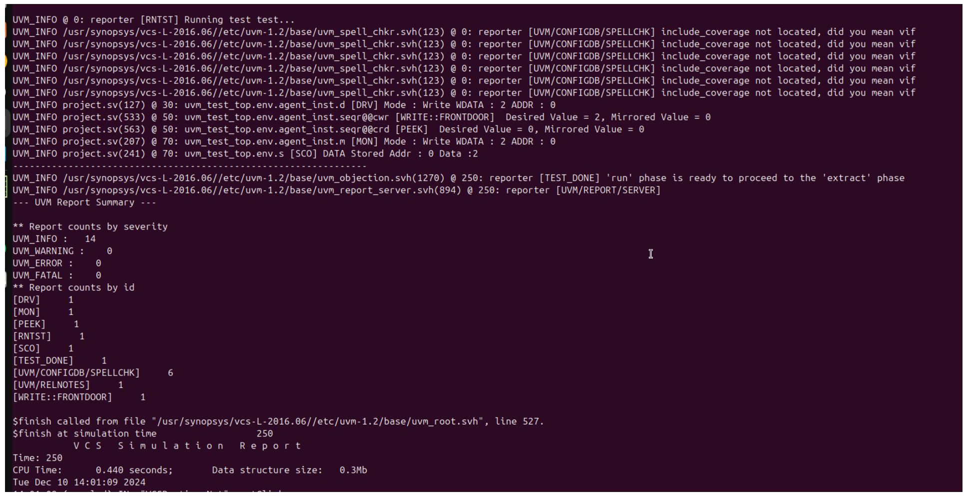
- **Code:**

```
class ctrl_wr extends uvm_sequence;
`uvm_object_utils(ctrl_wr)

 reg_block regmodel;
function new (string name = "ctrl_wr");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] wdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

     wdata = $urandom();

     regmodel.cntrl_inst.poke(status, wdata);

     //Check 'dv' and 'mv' Values
              dv = regmodel.cntrl_inst.get();
// Get Desired Value
              mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("POKE", $sformatf(" Desired Value = %0d, Mirrored
Value = %0d ", dv, mv), UVM_NONE)
```

```
 endtask
endclass


////////////////////////////////////////////////////////////////
/////////
//////////////////read data from control reg


class ctrl_rd extends uvm_sequence;
`uvm_object_utils(ctrl_rd)

 reg_block regmodel;

function new (string name = "ctrl_rd");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] rdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

   //////working with control
   regmodel.cntrl_inst.read(status, rdata, UVM_FRONTDOOR);

     //Check 'dv' and 'mv' Values
               dv = regmodel.cntrl_inst.get();
// Get Desired Value
               mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("READ::FRONTDOOR", $sformatf(" Desired Value =
%0d, Mirrored Value = %0d ", dv, mv), UVM_NONE)

 endtask
endclass
```

f. FRONTDOOR Write & PEEK:

- **Output:**



- **Code:**

```
class ctrl_wr extends uvm_sequence;
`uvm_object_utils(ctrl_wr)

 reg_block regmodel;
function new (string name = "ctrl_wr");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] wdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

     wdata = $urandom();

     regmodel.cntrl_inst.write(status, wdata, UVM_FRONTDOOR);

     //Check 'dv' and 'mv' Values
               dv = regmodel.cntrl_inst.get();
// Get Desired Value
               mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("WRITE::FRONTDOOR", $sformatf(" Desired Value =
%0d, Mirrored Value = %0d ", dv, mv), UVM_NONE)

 endtask
endclass


////////////////////////////////////////////////////////////////
/////////
/////////////////read data from control reg
```

```
class ctrl_rd extends uvm_sequence;
`uvm_object_utils(ctrl_rd)

 reg_block regmodel;

function new (string name = "ctrl_rd");
  super.new(name);
endfunction

task body;
  uvm_status_e   status;
  bit [3:0] rdata;
  bit [3:0] dv, mv;     // Desired Value & Mirrored Values

   //////working with control
   regmodel.cntrl_inst.peek(status, rdata);

     //Check 'dv' and 'mv' Values
              dv = regmodel.cntrl_inst.get();
// Get Desired Value
              mv = regmodel.cntrl_inst.get_mirrored_value();
     `uvm_info("PEEK", $sformatf(" Desired Value = %0d, Mirrored
Value = %0d ", dv, mv), UVM_NONE)

 endtask
endclass
```