**Module: UVM-2**

**Register Abstraction Layer**

**RAL**

Assignment 03

* **Register Block:**

| **Reg Block** |
| --- |
| class reg\_blk extends uvm\_reg\_block;    // Factory Registration  `uvm\_object\_utils(reg\_blk)  // Register instances  cntrl ctrl;  reg1 r1;  reg2 r2;  reg3 r3;  reg4 r4;  // Constructor  function new ( string name = "reg\_blk" );  super.new( name, UVM\_NO\_COVERAGE )  endfunction : new    // Build  function void build();  ctrl = cntrl::type\_id::create("ctrl");  ctrl.build;  ctrl.configure(this);  r1 = reg1::type\_id::create("r1");  r1.build;  r1.configure(this);  r2 = reg2::type\_id::create("r2");  r2.build;  r2.configure(this);  r3 = reg3::type\_id::create("r3");  r3.build;  r3.configure(this);  r4 = reg4::type\_id::create("r4");  r4.build;  r4.configure(this);  // Map  default\_map = create( "default\_map", 0, 4, UVM\_LITTLE\_ENDIAN, 1 )  default\_map.add\_reg( ctrl, 'h0, "RW" );  default\_map.add\_reg( r1, 'h4, "RW" );  default\_map.add\_reg( r2, 'h8, "RW" );  default\_map.add\_reg( r3, 'hC, "RW" );  default\_map.add\_reg( r4, 'h10, "RW" );  endfunction : build  endclass : reg\_blk |