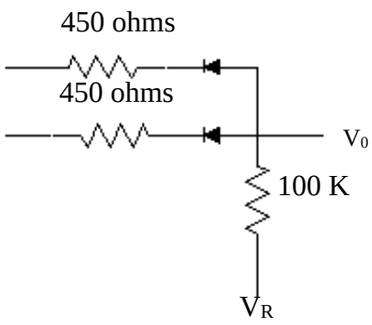
Ahsanullah University of Science and Technology
Department of Computer Science and Engineering
CSE 210: Digital Electronics and Pulse Techniques Sessional

Experiment # 1

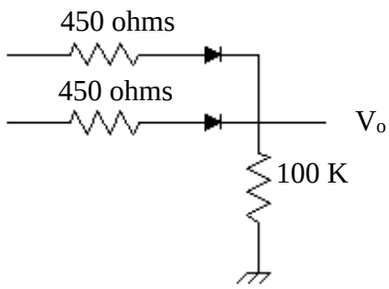
Name of the experiment: Study of DL and DTL gates.

CKT diagram:

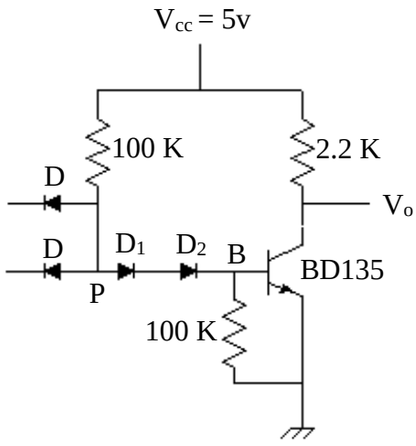
1.



2.



3.



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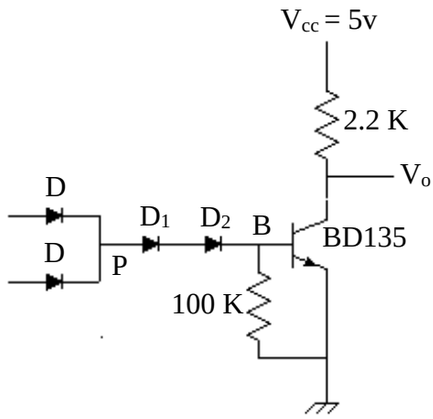


Procedure:

1. For ckt1 and ckt2 measure the output voltage V_o for all possible input combinations.
2. For ckt3 and ckt4 measure V_D, V_{D1}, V_{D2}, V_P, V_{CE} and V_o for all possible inputs. Calculate the $h_{FE(min)}$, NM(0) and NM(1).

Questions:

1. Analyze the ckt1 and ckt2 with the help of truth table for both positive and negative logic. [ck1, ck2]
2. What happens in V_R is more positive than V(1)? [ck1]
3. What happens if not all inputs have the same upper level? [ck1, ck2]
4. Why diode D_2 is used? [ck3, ck4]
5. Can emitter and collector be interchanged? [ck3, ck4]
6. What is the significant of $h_{FE(min)}$? [ck3, ck4]

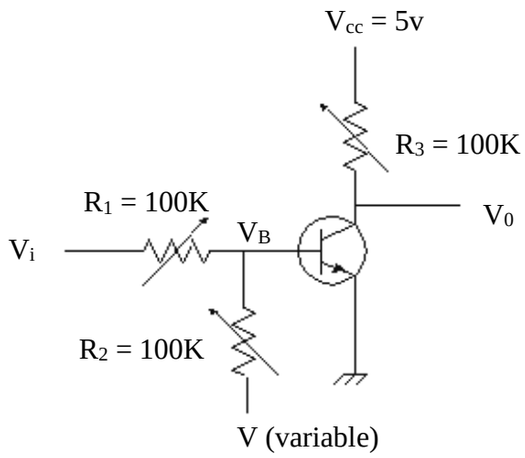
Report:

1. Objective.
2. Circuit diagram.
3. Answer to the questions.
4. Experimental data.
5. Calculations.
6. Discuss the findings.

Experiment #2

Name of the experiment: Study of a transistorized NOT gate.

CKT diagram:



Procedure:

1. Fix the value of R_1, R_2, V and vary R_3; measure V_0 and V_B.
2. Fix the value of R_1, R_3, V and vary R_2; measure V_0 and V_B.
3. Fix the value of R_2, R_3, V and vary R_1; measure V_0 and V_B.
4. Fix the value of R_1, R_2, R_3 and vary V; measure V_0 and V_B.

Questions:

1. Which factor affect the switching speed of a transistor and how?
2. What is the effect of R_1? Can it be very large?
3. Are there any effects of temperature on the circuit?

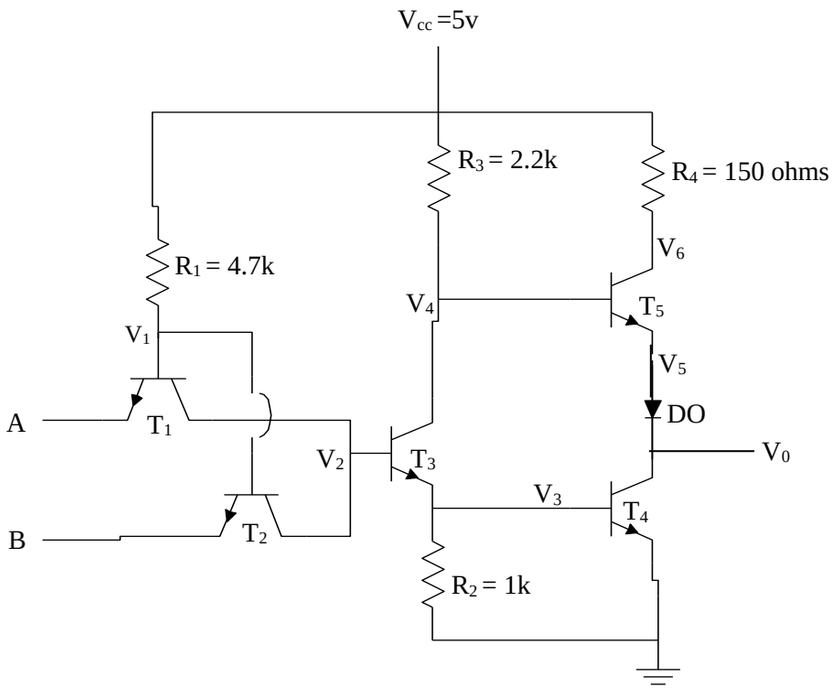
Report:

1. Objective.
2. Circuit diagram.
3. Answer to the questions.
4. Experimental data.
5. Calculations.
6. Discuss the findings.

Experiment # 3

Name of the experiment: Study of a TTL NAND gate with totem-pole output.

Circuit Diagram:



Procedure:

1. Measure the V_0, V_1, V_2, V_3, V_4, V_5 & V_6 for all possible input combinations.
2. Calculate noise margins.

Questions:

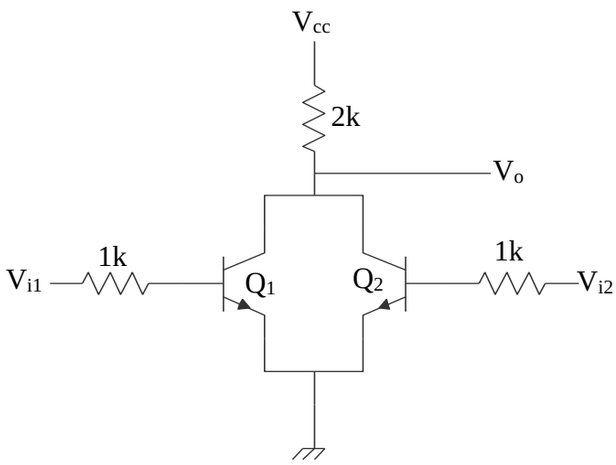
1. Analyze the operation of TTL NAND gate with the experimental data.
2. What are the differences of transistors T_1 & T_2 with that of a multi-emitter transistor? [Hint: Millman Sec 4-7,5-11]
3. What is totem-pole stage? Why it is used in place of passive pull-up resistor? [Hint: Millman Sec 5-12]
4. What is the function of T_3? [Hint: Millman Sec 5-12]
5. Why resistor R_4 is used? [Hint: Millman Sec 5-12]
6. Why diode D0 is used in the circuit? Can it be placed elsewhere? [Hint: Millman Sec 5-12]
7. Why two totem pole gates cannot be wire ANDed? [Hint: Millman pg. 151]
8. What are the features and advantages of TTL gates? [Hint: Millman Sec 5-15]

Report:

1. Objective.
2. Circuit diagram.
3. Answer to the questions.
4. Experimental data.
5. Calculations.
6. Discuss the findings.

Experiment # 4

Name of the experiment: Study of a RTL NOR gate.



Procedure:

1. Measure the output voltage (V_0) for all possible input combinations.
2. Connect the V_{i1} input to ground, vary V_{i2} and measure V_0.
3. Connect the V_{i2} input to ground, vary V_{i1} and measure V_0.

Questions:

1. Analyze the operation of RTL NOR gate with the experimental data.
2. What is the importance of studying the RTL gate? [Hint: Millman pg. 162]
3. Draw the V_0 vs. V_{i1} and V_{i2} curves.

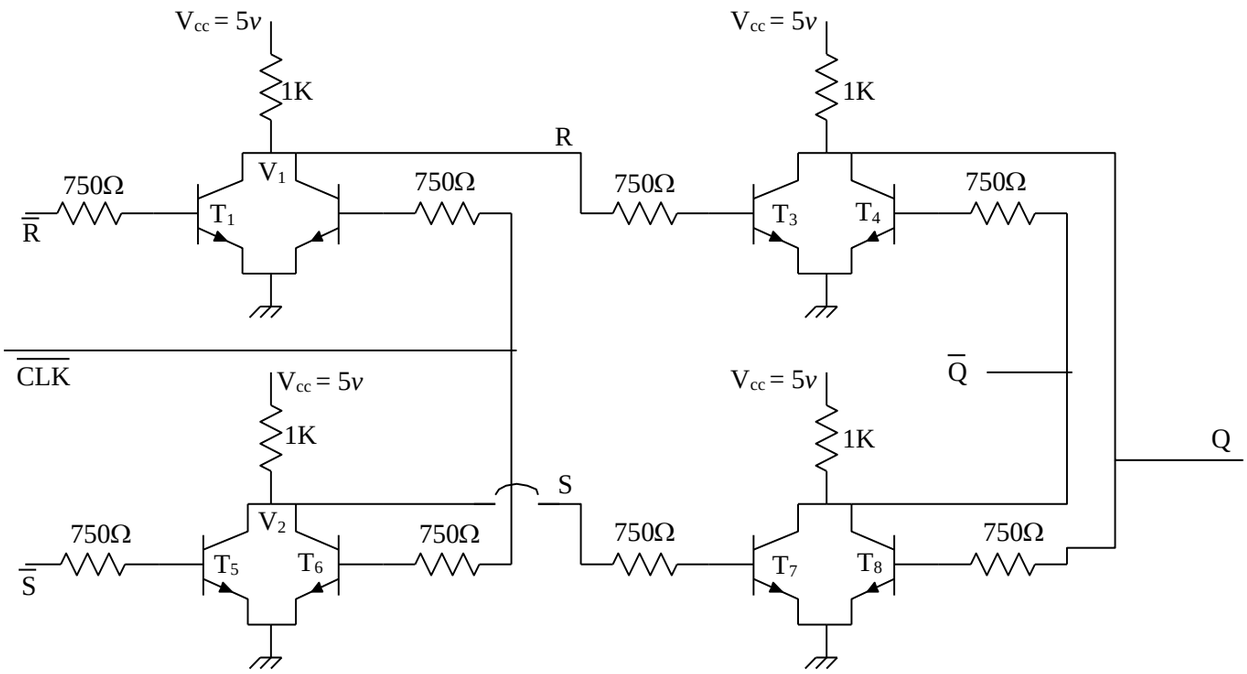
Report:

1. Objective.
2. Circuit diagram
3. Answer to the questions.
4. Experimental data.
5. Calculations.
6. Discuss the findings.

Experiment # 5

Name of the Experiment: Implementation of clocked SR Flip Flop using RTL NOR gates.

Circuit Diagram:



Procedure:

1. Measure the output voltages at Q & $\overline{Q}$ and voltages V_1, V_2 for all possible input (S,R) combinations.

Questions:

1. Analyze the operation of SR FF with the experimental data.
2. What is the race around condition in SR FF? Discuss with respect to the internal circuit.

Report:

1. Objective.
2. Circuit diagram.
3. Answer to the questions.
4. Experimental data.
5. Calculations.
6. Discuss the findings.