

1. Description

1.1. Project

Project Name	robotore_v2
Board Name	custom
Generated with:	STM32CubeMX 6.1.1
Date	07/19/2023

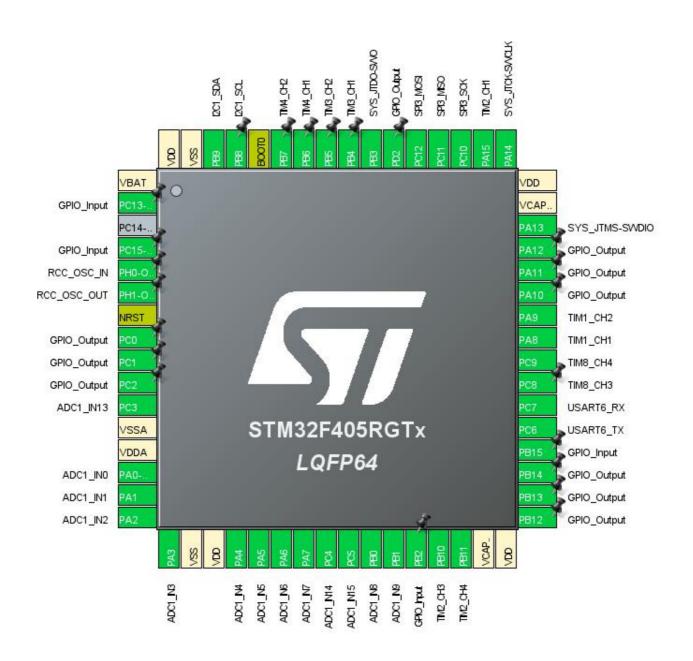
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405RGTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



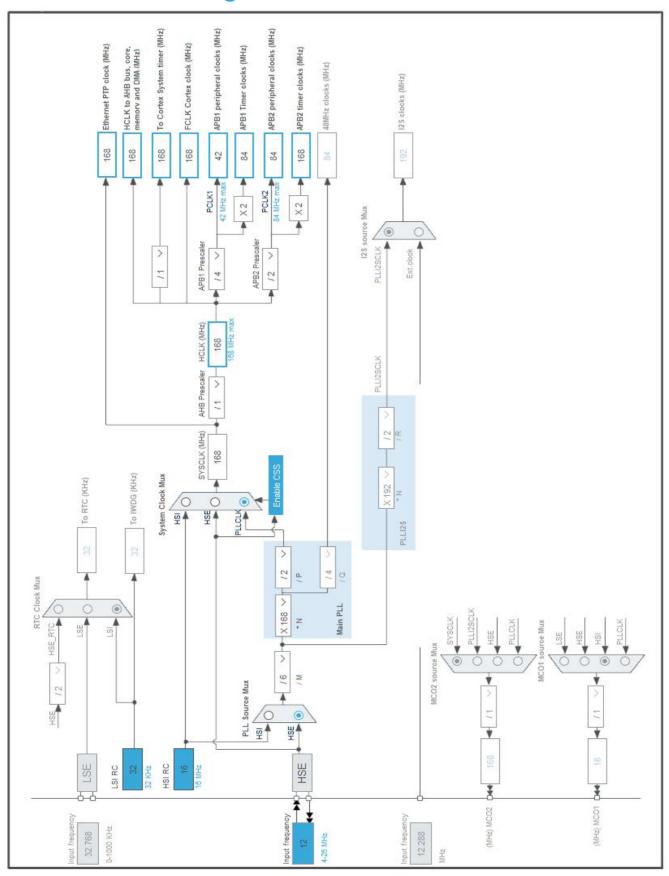
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP64	(function after		Function(s)	
	reset)			
1	VBAT	Power		
2	PC13-ANTI_TAMP *	I/O	GPIO_Input	
4	PC15-OSC32_OUT *	I/O	GPIO_Input	
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Output	
9	PC1 *	I/O	GPIO_Output	
10	PC2 *	I/O	GPIO_Output	
11	PC3	I/O	ADC1_IN13	
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	
15	PA1	I/O	ADC1_IN1	
16	PA2	I/O	ADC1_IN2	
17	PA3	I/O	ADC1_IN3	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
21	PA5	I/O	ADC1_IN5	
22	PA6	I/O	ADC1_IN6	
23	PA7	I/O	ADC1_IN7	
24	PC4	I/O	ADC1_IN14	
25	PC5	I/O	ADC1_IN15	
26	PB0	I/O	ADC1_IN8	
27	PB1	I/O	ADC1_IN9	
28	PB2 *	I/O	GPIO_Input	
29	PB10	I/O	TIM2_CH3	
30	PB11	I/O	TIM2_CH4	
31	VCAP_1	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	
34	PB13 *	I/O	GPIO_Output	
35	PB14 *	I/O	GPIO_Output	
36	PB15 *	I/O	GPIO_Input	
37	PC6	I/O	USART6_TX	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
38	PC7	I/O	USART6_RX	
39	PC8	I/O	TIM8_CH3	
40	PC9	I/O	TIM8_CH4	
41	PA8	I/O	TIM1_CH1	
42	PA9	I/O	TIM1_CH2	
43	PA10 *	I/O	GPIO_Output	
44	PA11 *	I/O	GPIO_Output	
45	PA12 *	I/O	GPIO_Output	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VCAP_2	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15	I/O	TIM2_CH1	
51	PC10	I/O	SPI3_SCK	
52	PC11	I/O	SPI3_MISO	
53	PC12	I/O	SPI3_MOSI	
54	PD2 *	I/O	GPIO_Output	
55	PB3	I/O	SYS_JTDO-SWO	
56	PB4	I/O	TIM3_CH1	
57	PB5	I/O	TIM3_CH2	
58	PB6	I/O	TIM4_CH1	
59	PB7	I/O	TIM4_CH2	
60	воото	Boot		
61	PB8	I/O	I2C1_SCL	
62	PB9	I/O	I2C1_SDA	
63	VSS	Power		
64	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	robotore_v2.4
Project Folder	C:\Users\Owner\STM32CubeIDE\workspace_1.5.1\robotore_v2.4
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_I2C1_Init	I2C1
6	MX_SPI3_Init	SPI3
7	MX_TIM1_Init	TIM1
8	MX_TIM3_Init	TIM3
9	MX_TIM4_Init	TIM4
10	MX_TIM8_Init	TIM8
11	MX_USART6_UART_Init	USART6

Rank	Function Name	Peripheral Instance Name
12	MX_TIM6_Init	TIM6
13	MX_TIM2_Init	TIM2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405RGTx
Datasheet	DS8626_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

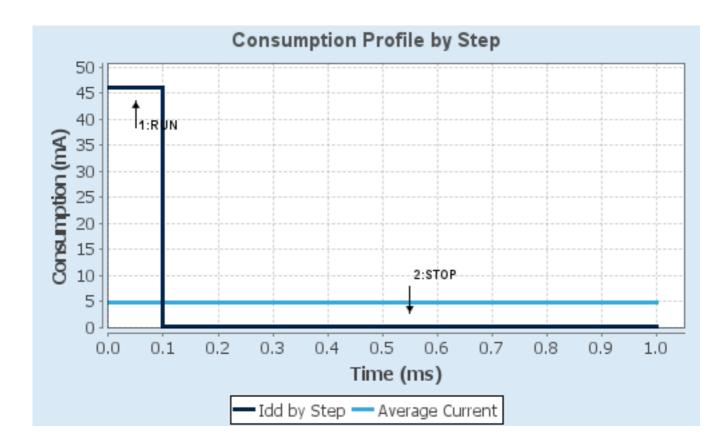
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	168 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	280 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	210.0	0.0
Ta Max	98.02	104.96
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1
mode: IN0
mode: IN1
mode: IN2
mode: IN3
mode: IN4
mode: IN5
mode: IN6

mode: IN7 mode: IN8 mode: IN9 mode: IN13

mode: IN14 mode: IN15

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment
Scan Conversion Mode
Continuous Conversion Mode
Discontinuous Conversion Mode
Disabled

DMA Continuous Requests

Right alignment
Enabled

Enabled

Disabled

Enabled *

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 13 *

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel 9 *
Sampling Time 480 Cycles *

<u>Rank</u> 2 *

Channel 8 *

Sampling Time 480 Cycles *

<u>Rank</u> 3 *

Channel 15 *
Sampling Time 480 Cycles *

<u>Rank</u> **4** *

Channel 14 *
Sampling Time 480 Cycles *

<u>Rank</u> 5 *

Channel Channel 7 *
Sampling Time 480 Cycles *

<u>Rank</u> 6 *

Channel 6 *
Sampling Time 480 Cycles *

<u>Rank</u> 7 *

Channel Channel 5 *
Sampling Time 480 Cycles *

<u>Rank</u> **8** *

Channel 4 *
Sampling Time 480 Cycles *

<u>Rank</u> **9** *

Channel 3 *
Sampling Time 480 Cycles *

Rank 10 *

Channel 2 *
Sampling Time 480 Cycles *

<u>Rank</u> 11 *

Channel 1 *
Sampling Time 480 Cycles *

 Rank
 12 *

 Channel
 Channel 0

 Sampling Time
 480 Cycles *

<u>Rank</u> 13 *

Channel 13 *
Sampling Time 480 Cycles *

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. I2C1 I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode Standard Mode

I2C Clock Speed (Hz) 100000

Slave Features:

Clock No Stretch Mode Disabled

Primary Address Length selection 7-bit

Dual Address Acknowledged Disabled

Primary slave address 0

General Call address detection Disabled

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

Power Parameters:

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.4. SPI3

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate)

Baud Rate 21.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSS Signal Type Software

7.5. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

7.6. TIM1

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)

Counter Mode

Counter Period (AutoReload Register - 16 bits value)

Internal Clock Division (CKD)

No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable

BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 2:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

7.7. TIM2

Channel1: PWM Generation CH1 Channel3: PWM Generation CH3 Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0
Counter Mode Up
Counter Period (AutoReload Register - 32 bits value) 8399 *
Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode PWM mode 1

Pulse (32 bits value) 0

	- ·
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
PWM Generation Channel 3:	
Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
PWM Generation Channel 4:	
Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
7.8. TIM3	
Combined Channels: Encoder Mod	de
7.8.1. Parameter Settings:	
Counter Settings:	
Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Trigger Output (TRGO) Parameters:	
Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)
	Trooper (000 bit from Filmx_201t)
Encoder:	Face des Made TIA
Encoder Mode	Encoder Mode TI1
Parameters for Channel 1	Divine Educ
Polarity	Rising Edge
IC Selection	Direct No division
Prescaler Division Ratio	No division
Input Filter	0
Parameters for Channel 2	Dising Edge
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division

Input Filter 0

7.9. TIM4

Combined Channels: Encoder Mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 0 Counter Mode Up Counter Period (AutoReload Register - 16 bits value) 65535 Internal Clock Division (CKD) No Division auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode Encoder Mode TI1 ____ Parameters for Channel 1 ___ Polarity Rising Edge IC Selection Direct

Prescaler Division Ratio No division Input Filter 0

Parameters for Channel 2 ____

Polarity Rising Edge IC Selection Direct Prescaler Division Ratio No division

Input Filter

7.10. TIM6

mode: Activated

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 83 * Counter Mode Up Counter Period (AutoReload Register - 16 bits value) 999 * Disable auto-reload preload

Trigger Output (TRGO) Parameters:

Trigger Event Selection Reset (UG bit from TIMx_EGR)

7.11. TIM8

Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value) 1 *

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value) 2000 *

Internal Clock Division (CKD) No Division

Repetition Counter (RCR - 8 bits value) 0

auto-reload preload Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit) Disable (Trigger input effect not delayed)

Trigger Event Selection Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State Disable
BRK Polarity High

Break And Dead Time management - Output Configuration:

Automatic Output State Disable
Off State Selection for Run Mode (OSSR) Disable
Off State Selection for Idle Mode (OSSI) Disable
Lock Configuration Off

PWM Generation Channel 3:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High
CH Idle State Reset

PWM Generation Channel 4:

Mode PWM mode 1

Pulse (16 bits value) 0

Output compare preload Enable
Fast Mode Disable
CH Polarity High

CH Idle State Reset

7.12. USART6

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate 14400 *

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max	User Label
ADC1	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	Speed n/a	
ADCI	PA0-WKUP	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC1 IN8	Analog mode	No pull-up and no pull-down	n/a	
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	Pull-up	Very High	
	PB9	I2C1_SDA	Alternate Function Open Drain	Pull-up	Very High	
RCC	PH0- OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
	PB11	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM8	PC8	TIM8_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC9	TIM8_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
GPIO	PC13- ANTI_TAMP	GPIO_Input	Input mode	Pull-up *	n/a	
	PC15- OSC32_OU T	GPIO_Input	Input mode	Pull-up *	n/a	
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	Low

ADC1: DMA2_Stream0 DMA request Settings:

Mode: Circular *
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: Enable *
Peripheral Data Width: Half Word
Memory Data Width: Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Pre-fetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0	
DMA2 stream0 global interrupt	true	0	0	
USART6 global interrupt	true	0	0	
PVD interrupt through EXTI line 16				
Flash global interrupt	unused			
RCC global interrupt	unused			
ADC1, ADC2 and ADC3 global interrupts	unused			
TIM1 break interrupt and TIM9 global interrupt	unused			
TIM1 update interrupt and TIM10 global interrupt	unused			
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused			
TIM1 capture compare interrupt	unused			
TIM2 global interrupt		unused		
TIM3 global interrupt		unused		
TIM4 global interrupt		unused		
I2C1 event interrupt		unused		
I2C1 error interrupt	unused			
TIM8 break interrupt and TIM12 global interrupt	t unused			
TIM8 update interrupt and TIM13 global interrupt	unused			
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused			
TIM8 capture compare interrupt	unused			
SPI3 global interrupt	unused			
FPU global interrupt		unused		

8.3.2. NVIC Code generation

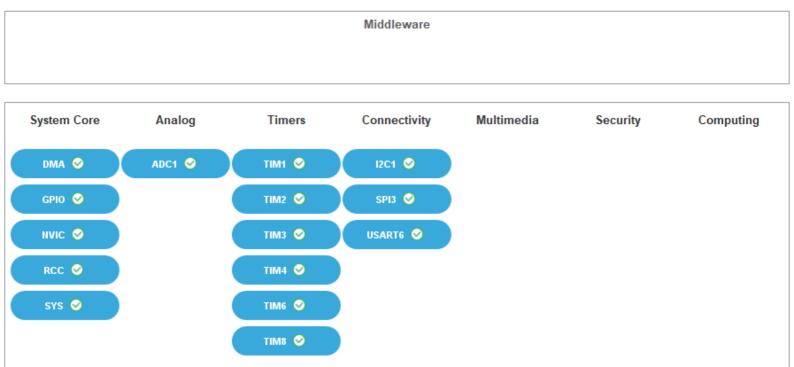
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true
DMA2 stream0 global interrupt	false	true	true
USART6 global interrupt	false	true	true

^{*} User modified value

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/DM00037051.pdf

Reference http://www.st.com/resource/en/reference_manual/DM00031020.pdf

manual

Programming http://www.st.com/resource/en/programming manual/DM00046982.pdf

manual

Errata sheet http://www.st.com/resource/en/errata_sheet/DM00037591.pdf

Application note http://www.st.com/resource/en/application_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application_note/CD00211314.pdf

Application note http://www.st.com/resource/en/application_note/CD00249778.pdf

Application note http://www.st.com/resource/en/application_note/CD00259245.pdf

Application note http://www.st.com/resource/en/application_note/CD00264321.pdf

Application note http://www.st.com/resource/en/application_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application_note/DM00024853.pdf

Application note http://www.st.com/resource/en/application_note/DM00025071.pdf

Application note http://www.st.com/resource/en/application_note/DM00040802.pdf

Application note http://www.st.com/resource/en/application_note/DM00040808.pdf

Application note http://www.st.com/resource/en/application_note/DM00042534.pdf

Application note http://www.st.com/resource/en/application_note/DM00046011.pdf

Application note http://www.st.com/resource/en/application_note/DM00050879.pdf

Application note http://www.st.com/resource/en/application_note/DM00072315.pdf

Application note http://www.st.com/resource/en/application_note/DM00073742.pdf

Application note http://www.st.com/resource/en/application_note/DM00073853.pdf

Application note http://www.st.com/resource/en/application_note/DM00080497.pdf

Application note http://www.st.com/resource/en/application_note/DM00081379.pdf

Application note http://www.st.com/resource/en/application_note/DM00115714.pdf

Application note http://www.st.com/resource/en/application_note/DM00129215.pdf

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