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HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL AND ELECTRONICS ENGINEERING

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LABORATORY REPORT

Waveform generator

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SUBJECT: Digital signal processing on FPGA

GROUP: 08

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1.1 Module Waveform Generator

1.1.1 Module Sine Waveform

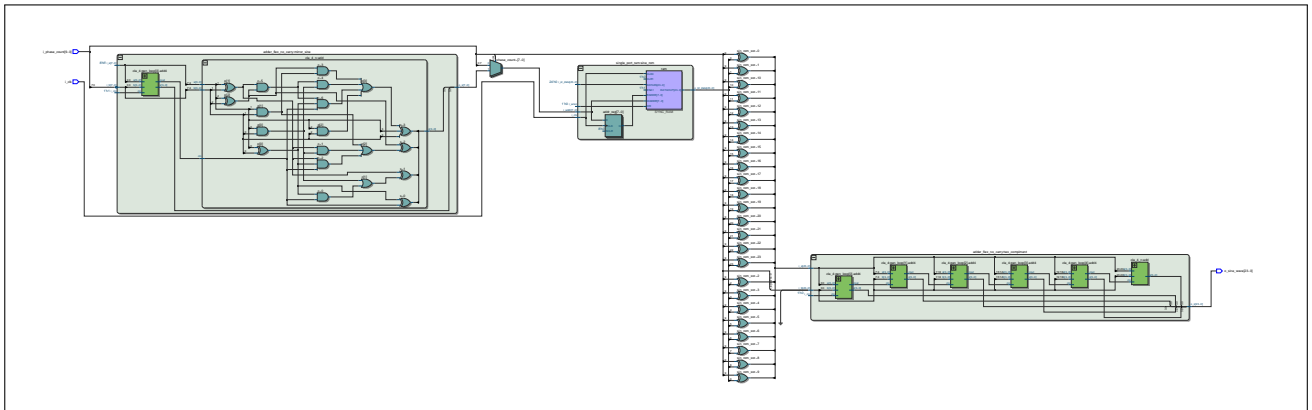


Figure 1.1: Block diagram for Module Sin_Wave.

1 HARDWARE DESIGN AND IMPLEMENTATION

1.1.2 Module Square Waveform

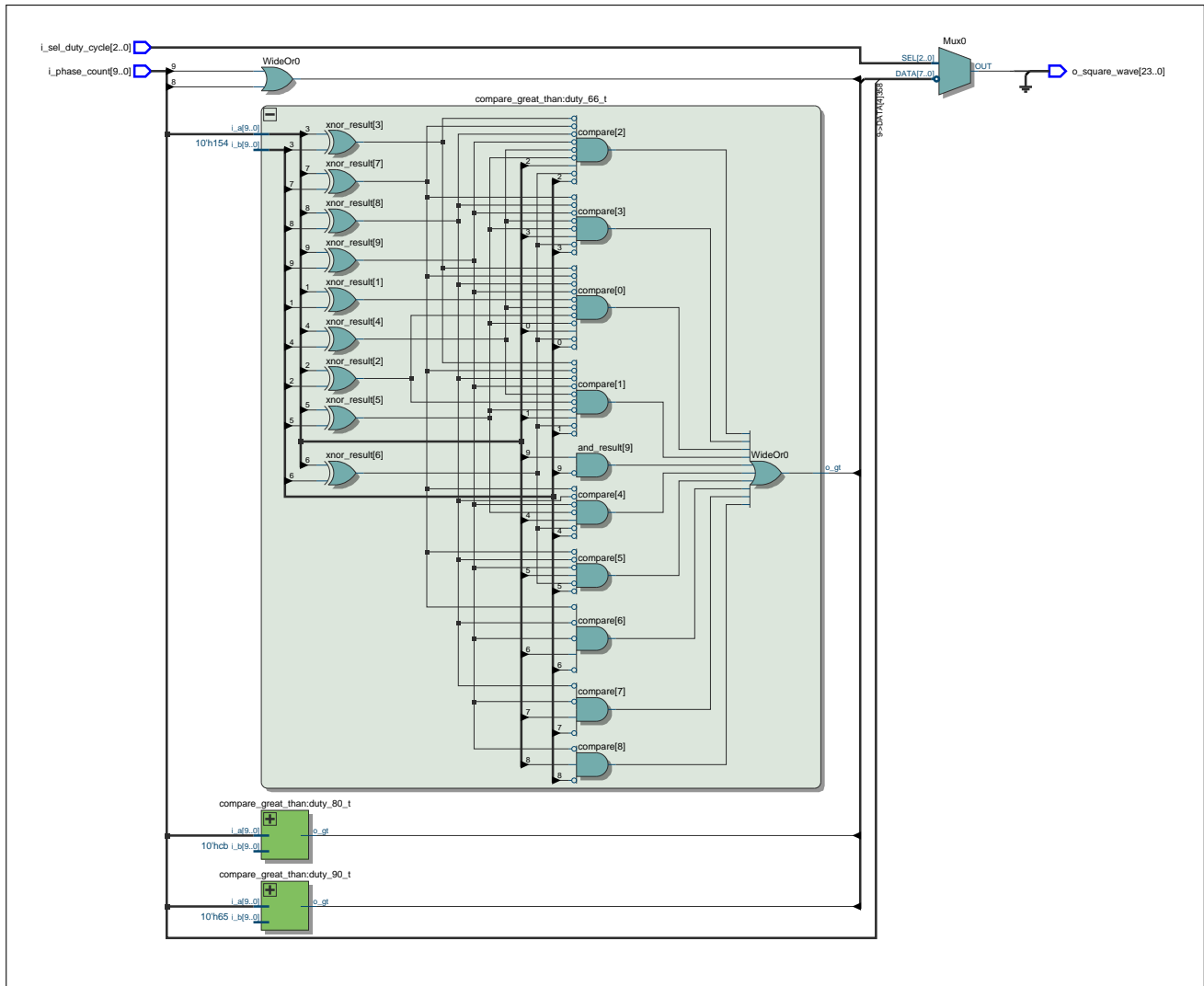


Figure 1.2: Block diagram for Module Square_wave.

1 HARDWARE DESIGN AND IMPLEMENTATION

1.1.3 Module Triangle Waveform

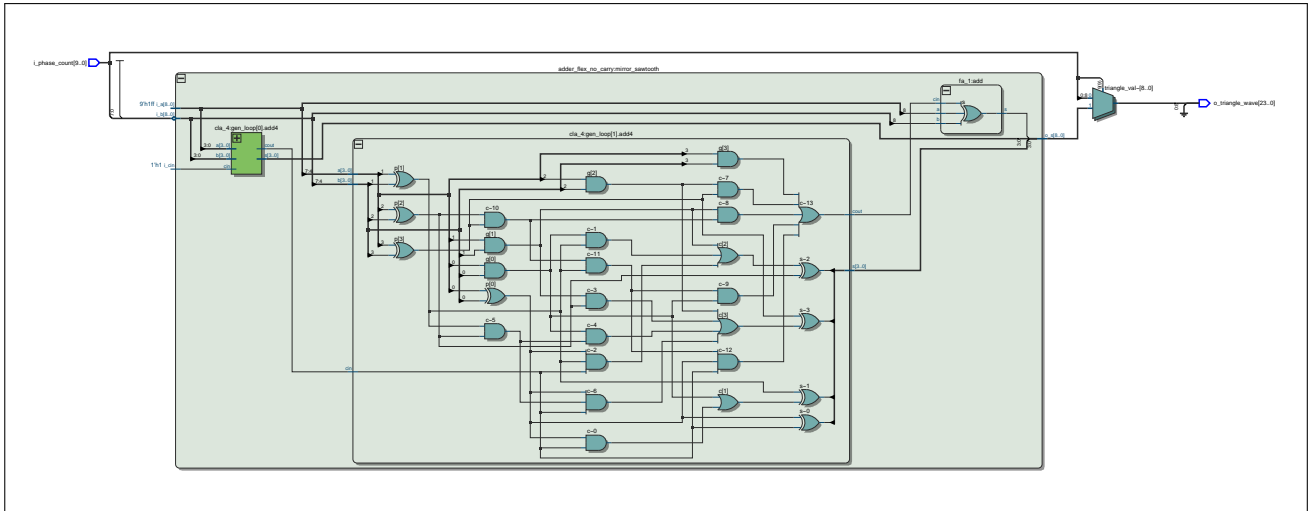


Figure 1.3: Block diagram for Module Triangle_wave.

1.1.4 Module Sawtooth Waveform

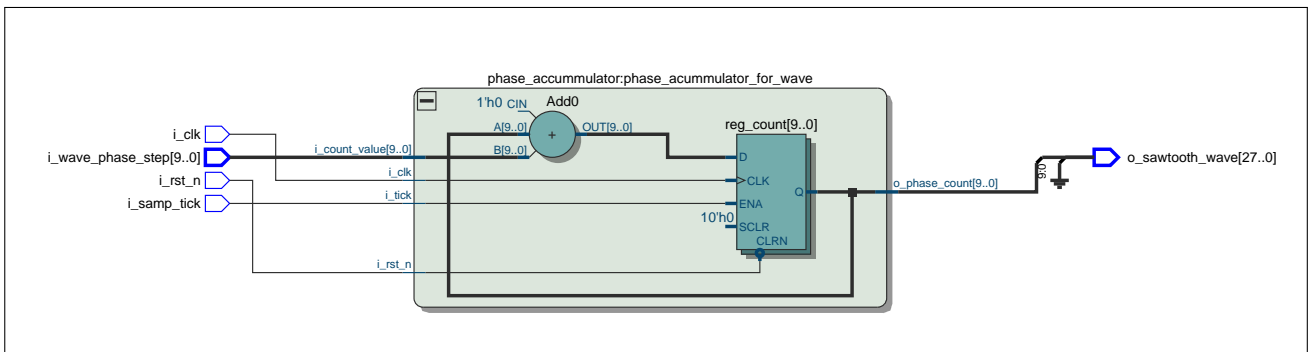


Figure 1.4: Block diagram for Module Sawtooth_wave.

1 HARDWARE DESIGN AND IMPLEMENTATION

1.1.5 Module ECG Waveform

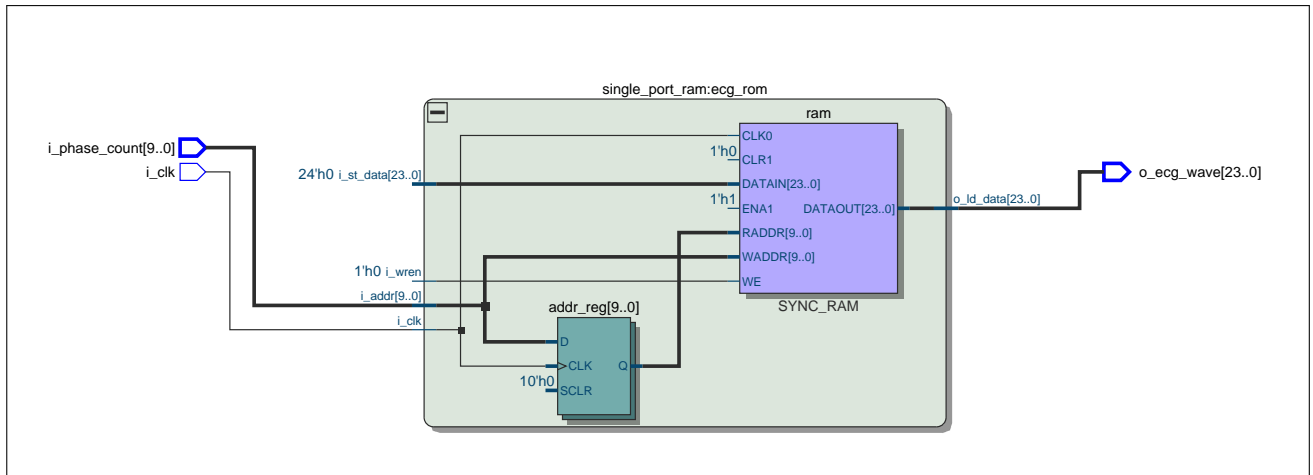


Figure 1.5: Block diagram for Module ECG_wave.

1 HARDWARE DESIGN AND IMPLEMENTATION

1.1.6 Module Waveform Generator

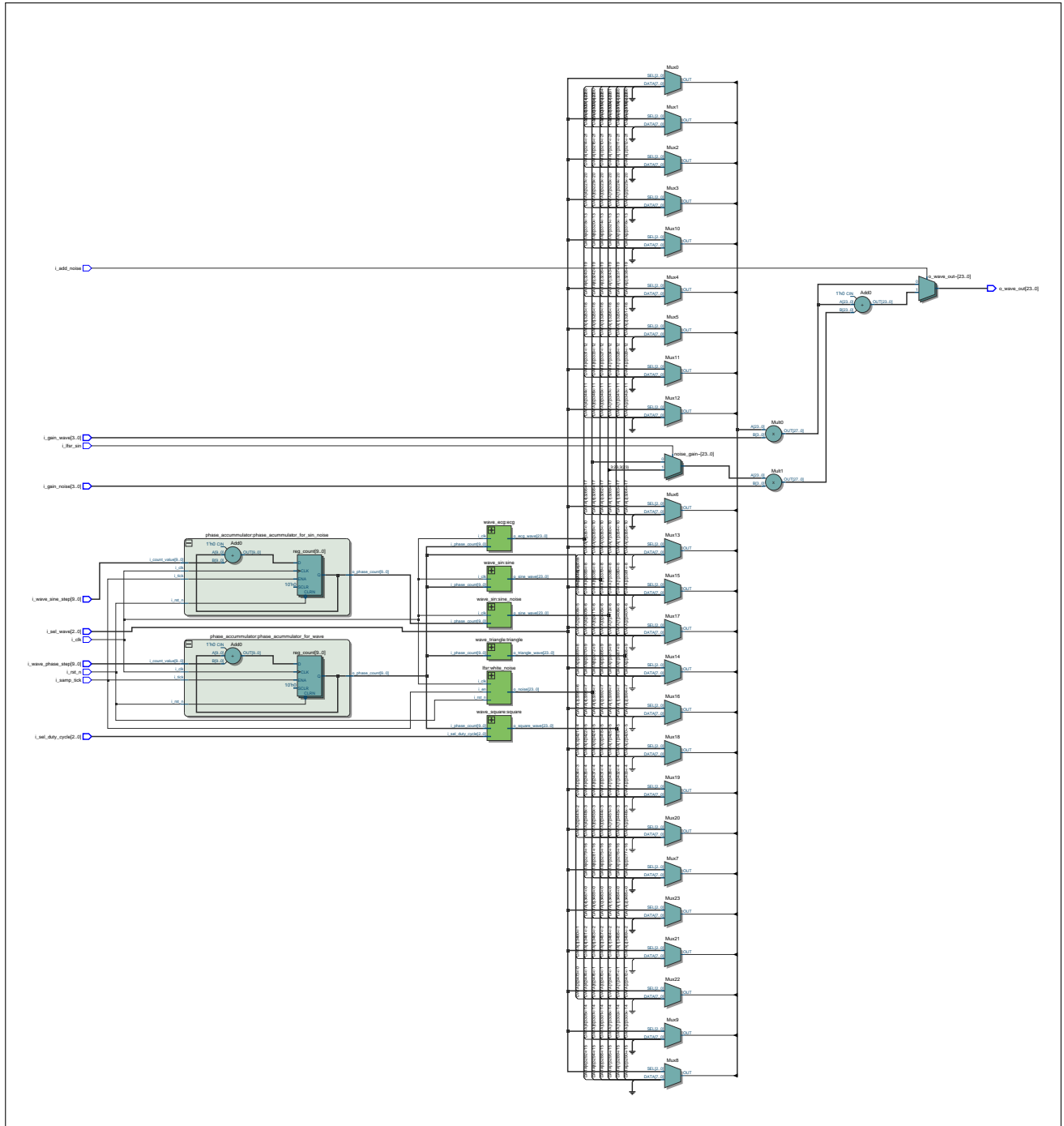


Figure 1.6: Block diagram for Module Waveform Generator.

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1.3 Module Control value

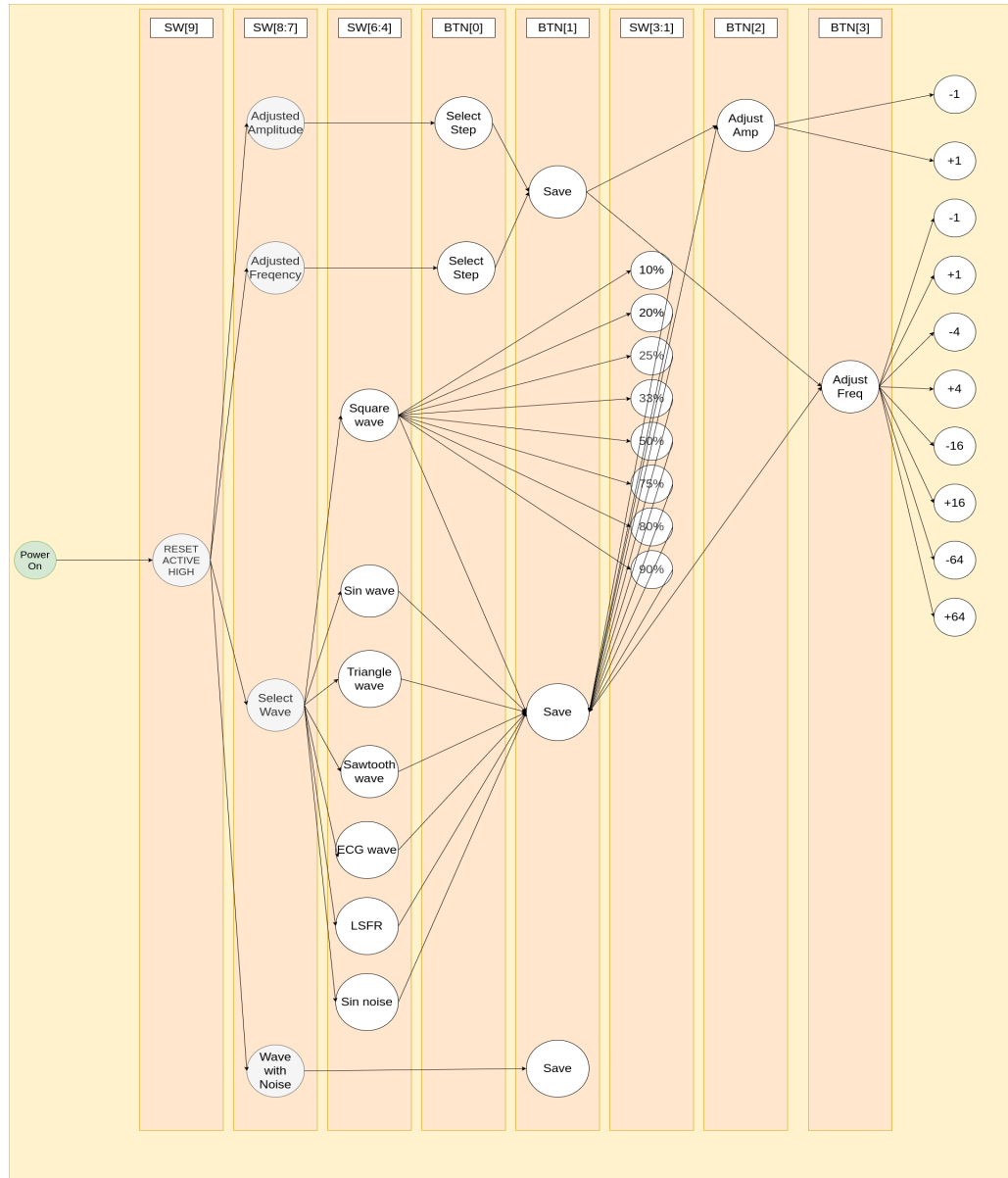


Figure 1.8: Communication operations between the user and the Control Value Module.

1 HARDWARE DESIGN AND IMPLEMENTATION

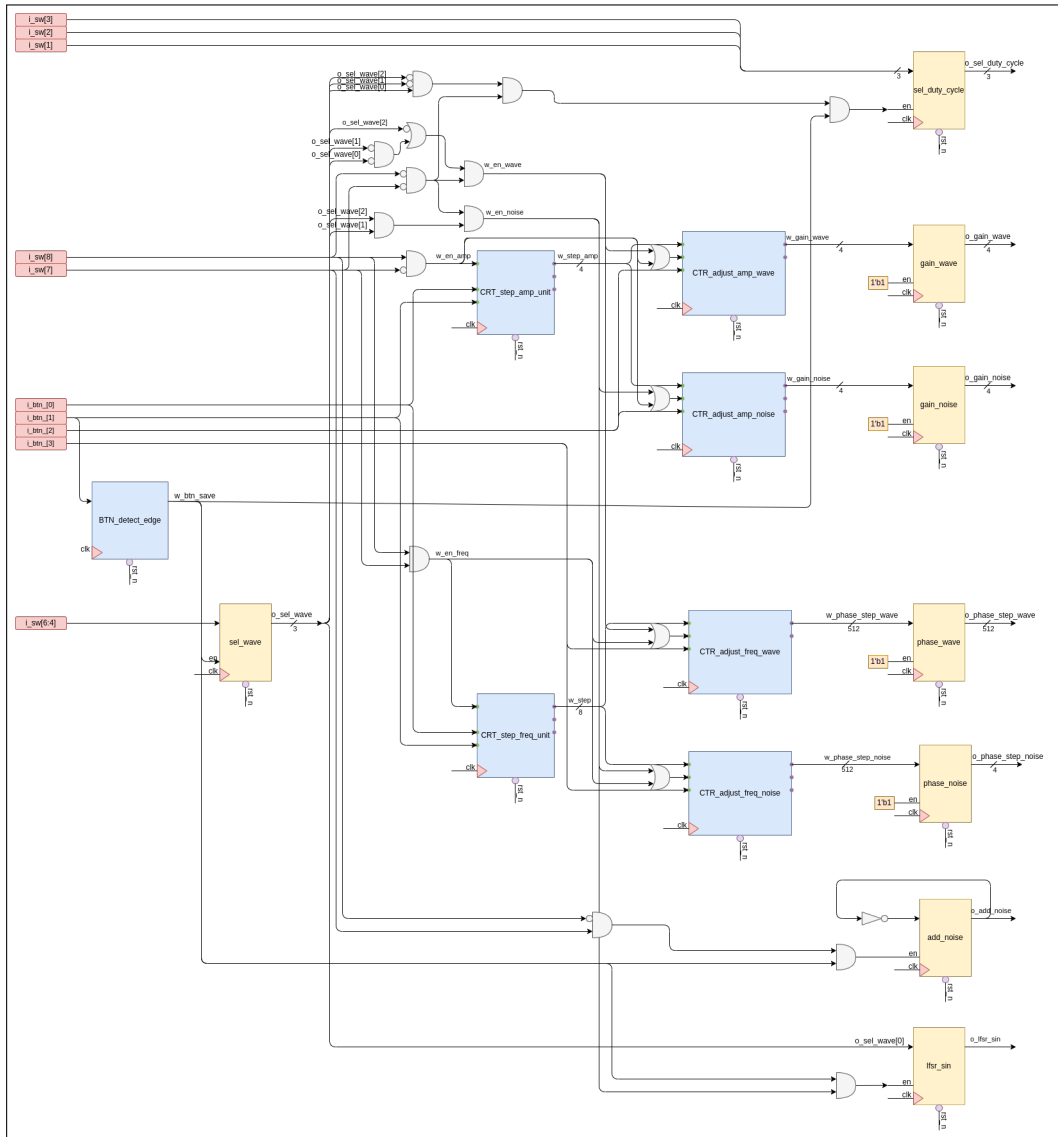


Figure 1.9: Block diagram for Module Control value.

1 HARDWARE DESIGN AND IMPLEMENTATION

1.3.1 Module I²C trans

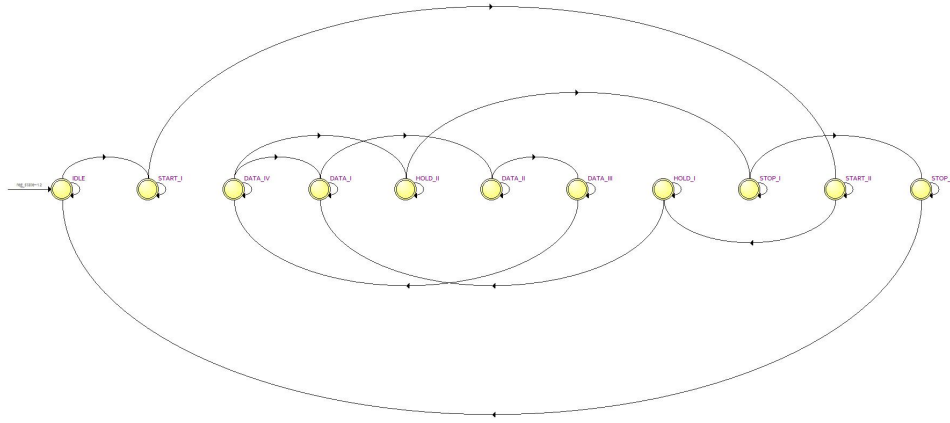


Figure 1.10: FSM control Module I²C trans.

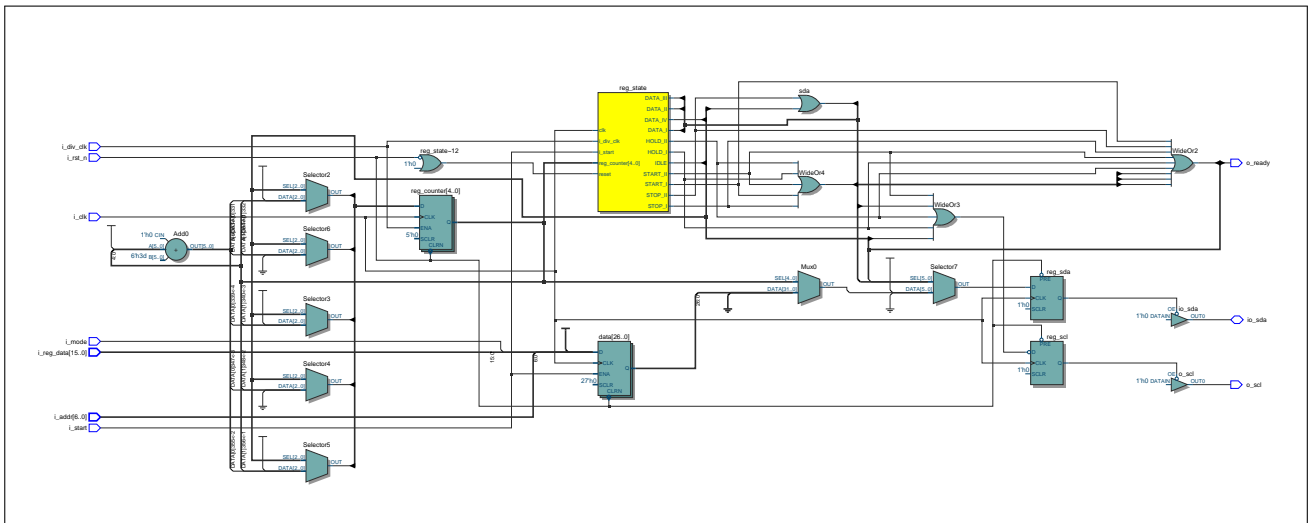


Figure 1.11: Block diagram for Module I²C trans.

1.3.2 Module Audio Codec config

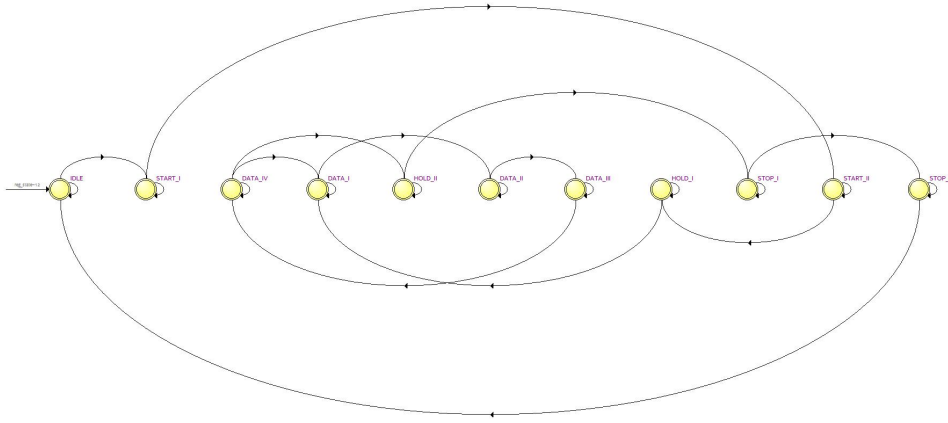


Figure 1.12: FSM control Module Aduio Codec config.

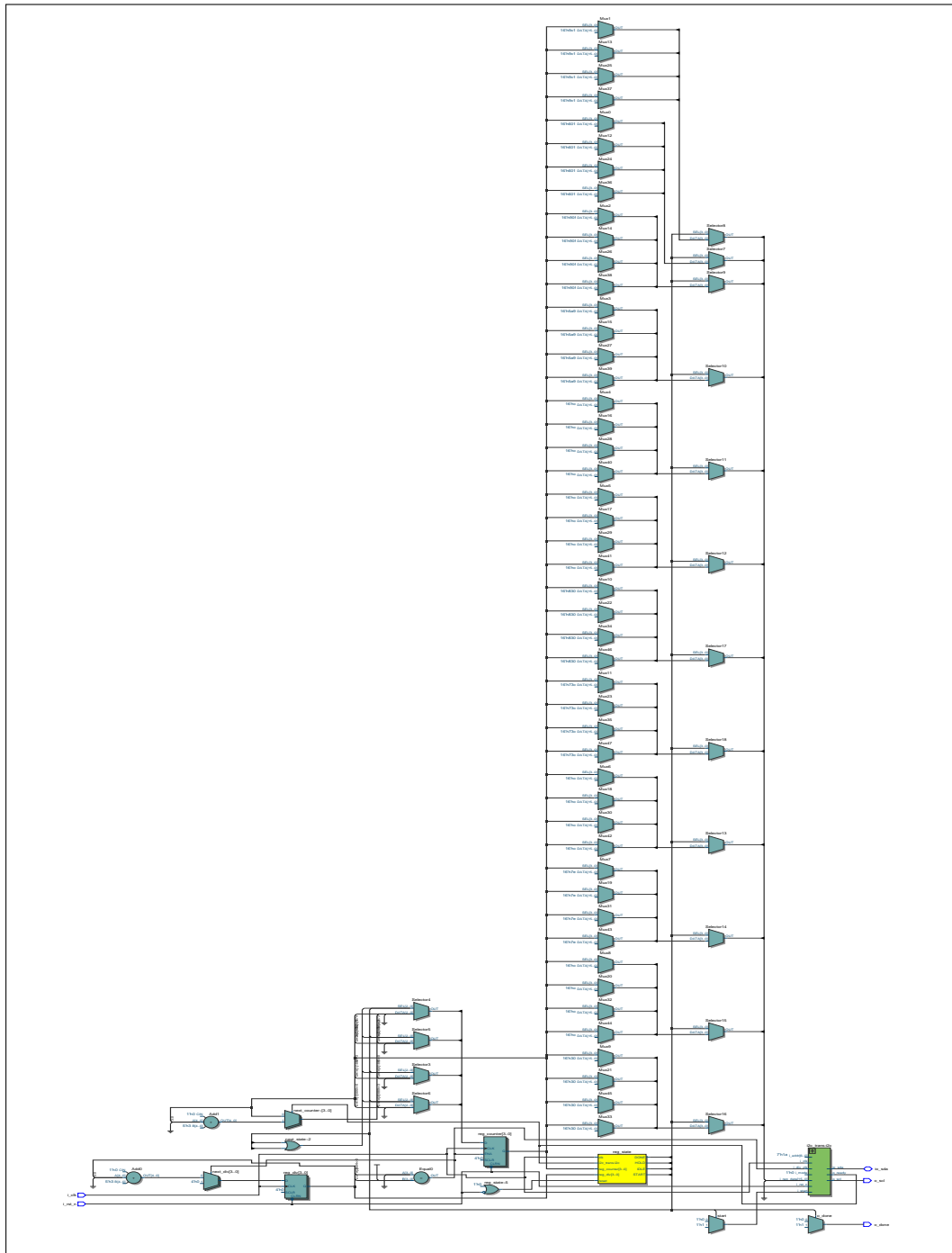


Figure 1.13: Block diagram for Module Audio Codec config.

1.3.3 Module Audio Codec data

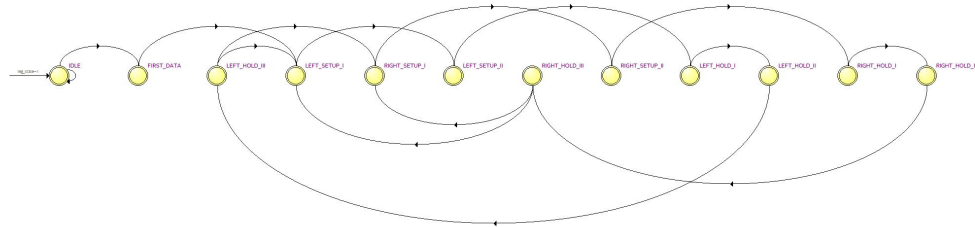


Figure 1.14: FSM control Module Audio Codec data.

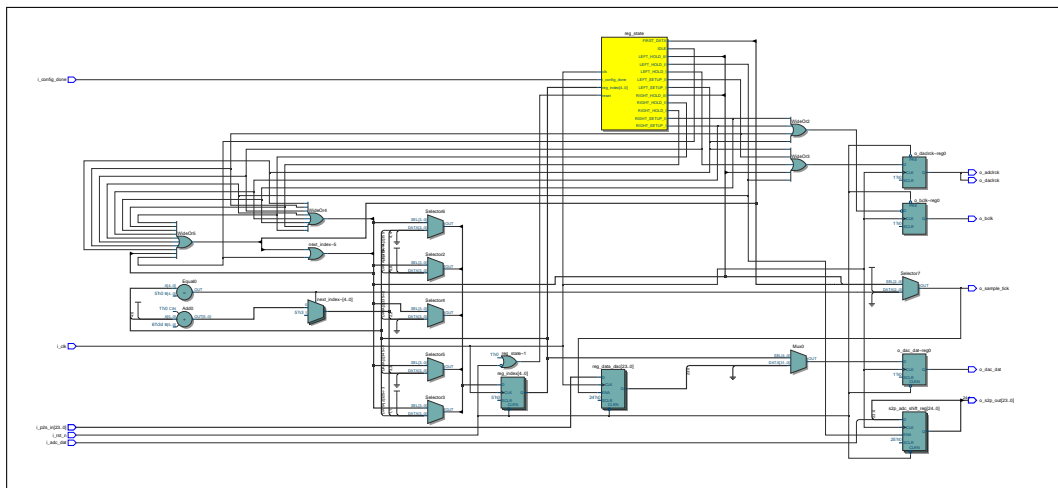


Figure 1.15: Block diagram for Module Audio Codec data.