VIETNAM NATIONAL UNIVERSITY HO CHI MINH CITY
HO CHI MINH CITY UNIVERSITY OF TECHNOLOGY
FACULTY OF ELECTRICAL AND ELECTRONICS ENGINEERING

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BIG PROJECT 2 REPORT

FPGA Implementation of 8-Point FFT - Digital System Design

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SUBJECT: Digital System Design and Verification

GROUP: 08

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Mục lục

Danh sách hình vẽ

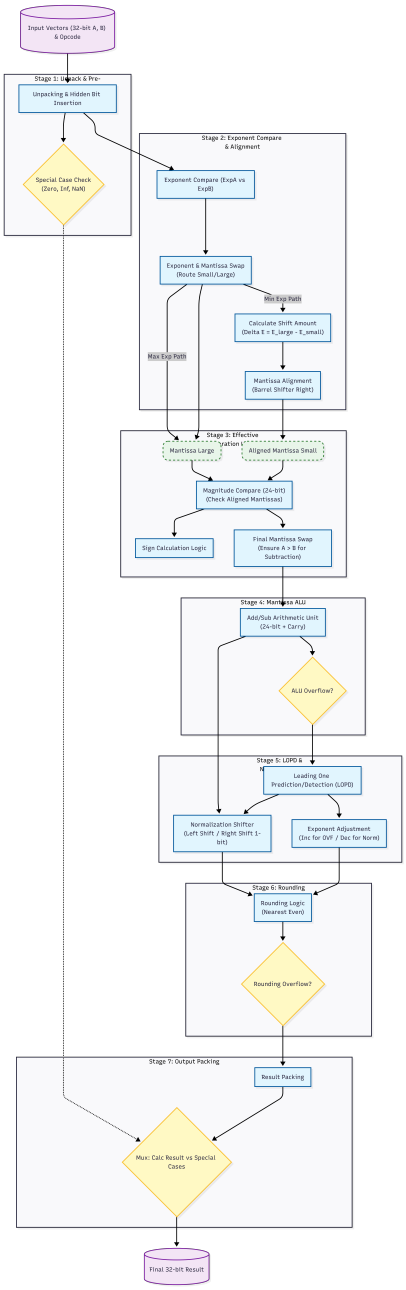
Danh sách bảng

List of Listings

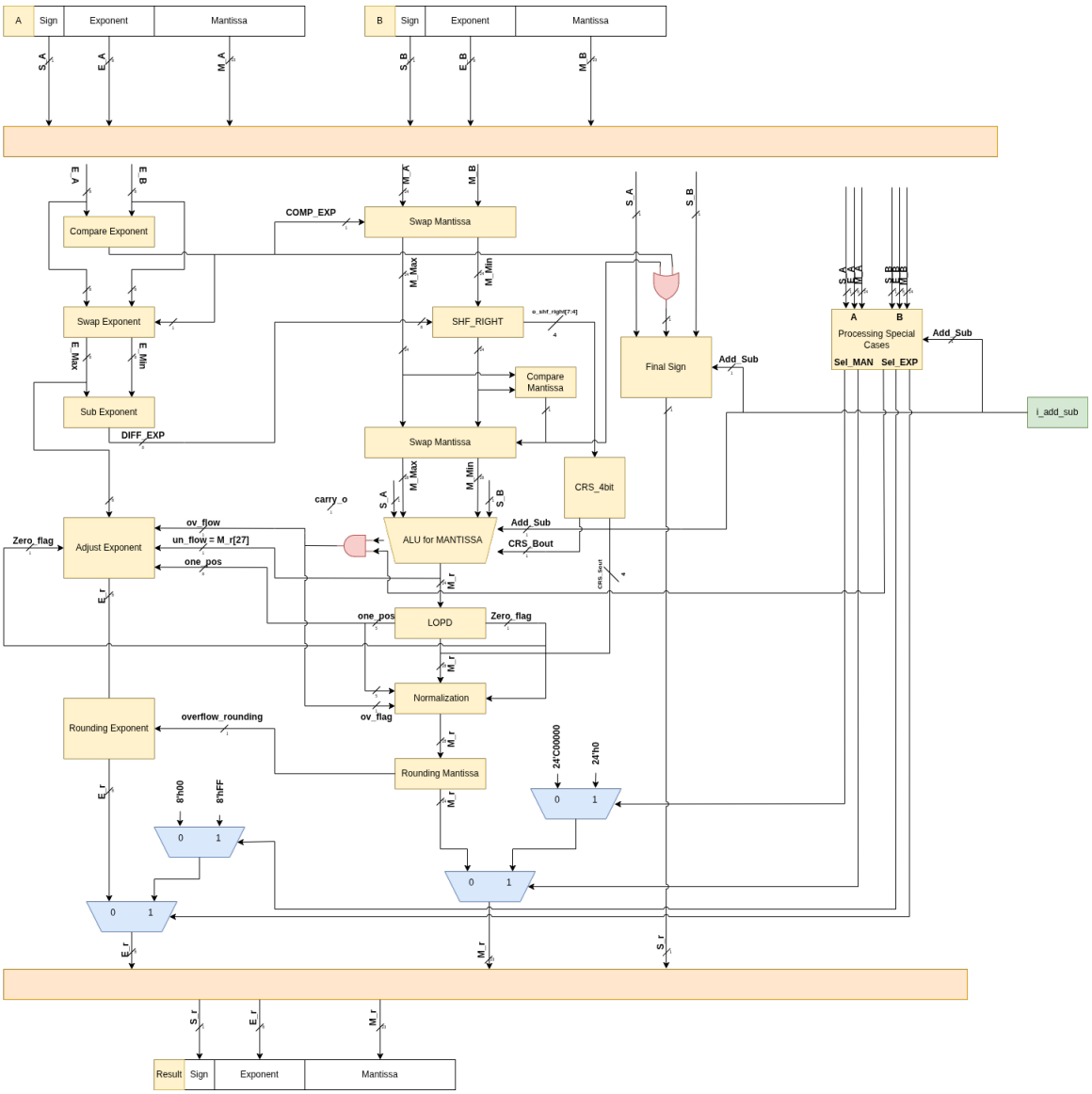
Chapter 1. Theorical Background

Chapter 2. RTL Implementation Strategy

2.1 IEEE 754 Single-Precision Floating-Point Adder/Subtractor Design

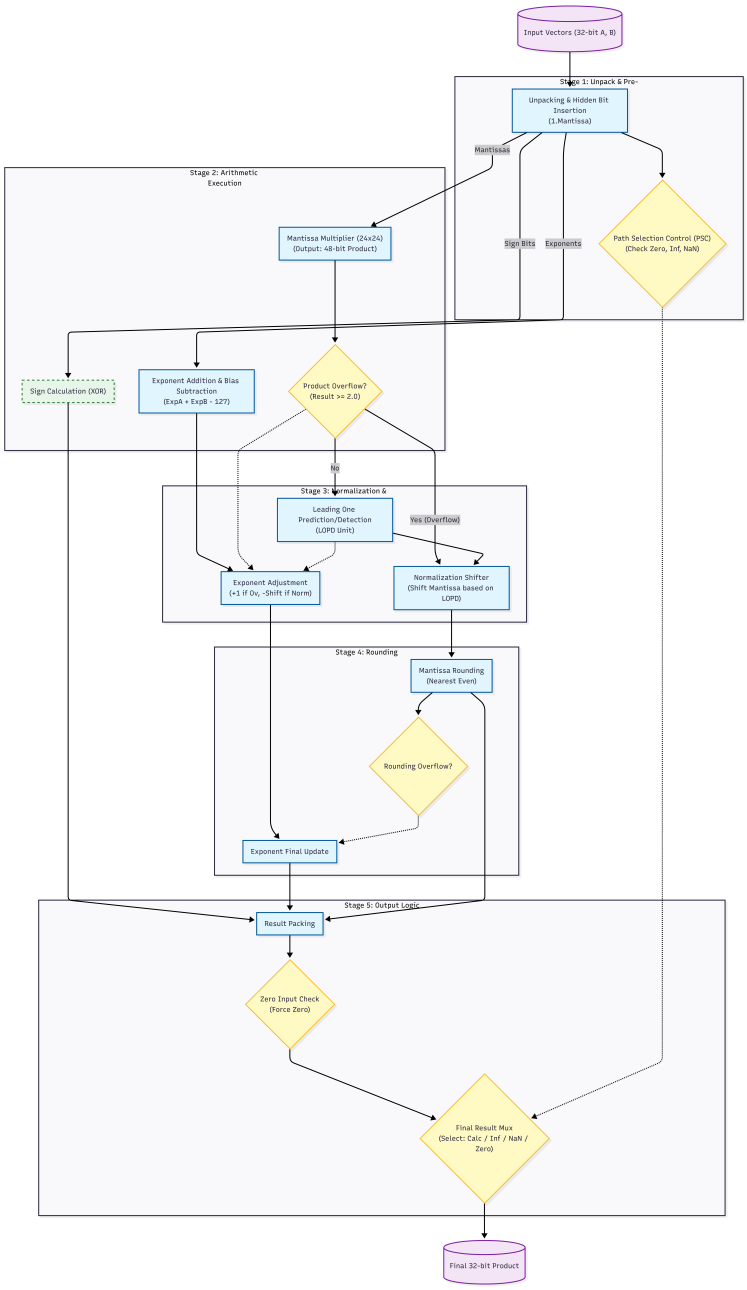


Hình 2.1: Algorithmic flowchart of the IEEE 754 Floating-Point Adder/Subtractor.

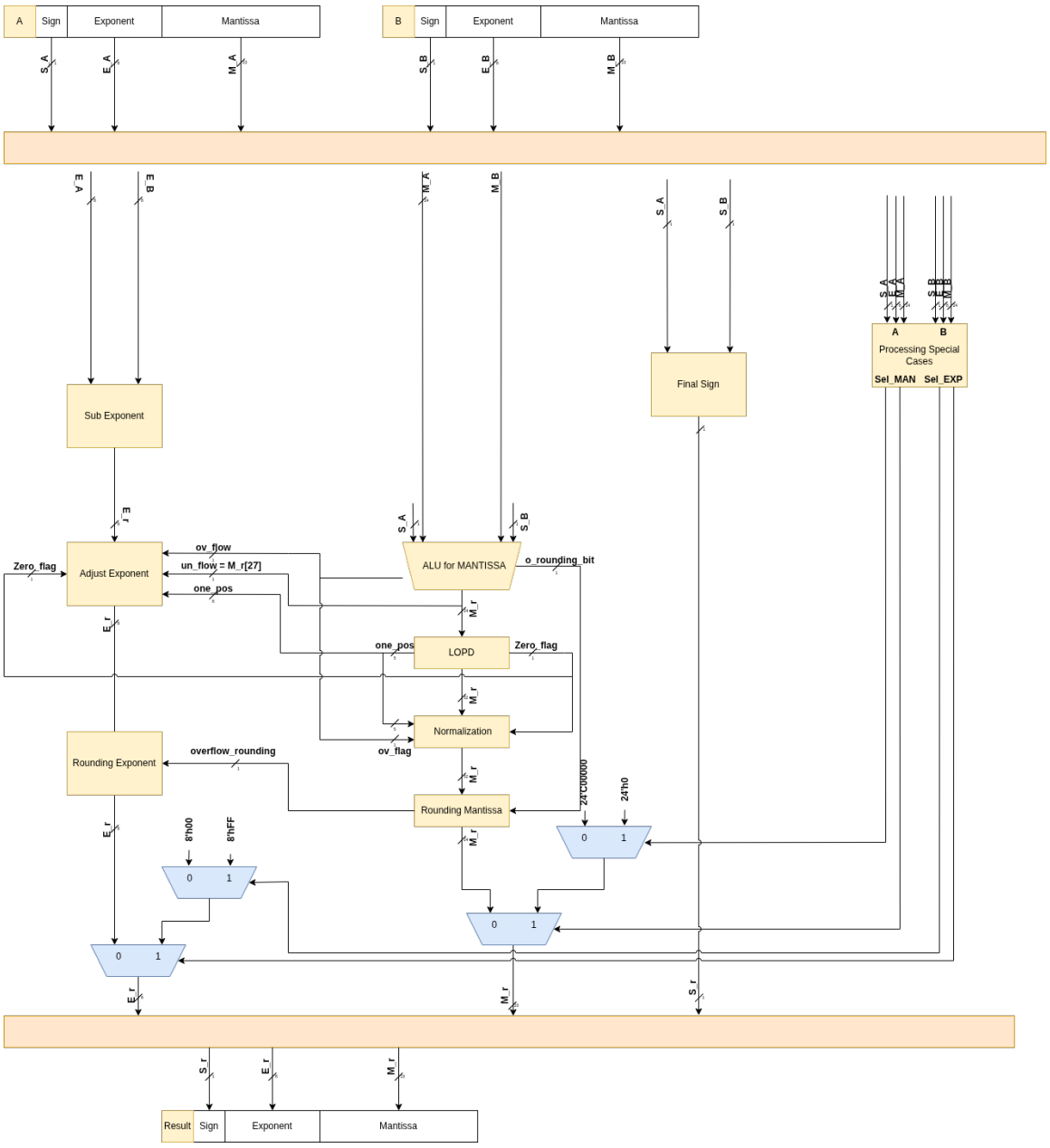


Hình 2.2: Top-level hardware architecture of the 32-bit Floating-Point Adder/Subtractor.

2.2 IEEE 754 Single-Precision Floating-Point Multiplier Design



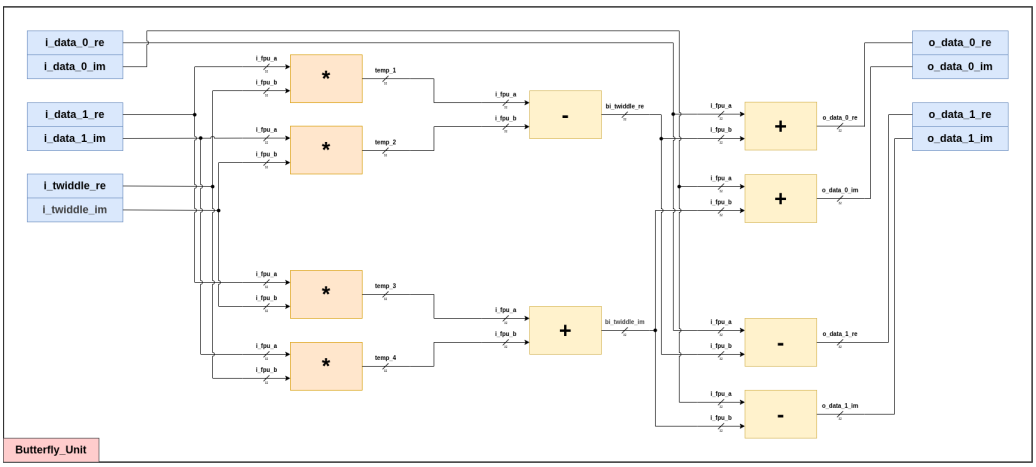
Hình 2.3: Algorithmic flowchart of the IEEE 754 Floating-Point Multiplier.



Hình 2.4: Top-level hardware architecture of the 32-bit Floating-Point Multiplier.

2.3 Radix-2 Butterfly Processing Unit (BPU) Design

$$(a + jb) * (c + jd) = (ad + bc) - j(ad - bc)$$



Hình 2.5: Structure of Radix-2 Butterfly Processing Unit (BPU).

2.4 8-Point FFT Processor Top-Level Architecture