Design and Implementation of Reversible Logic Based Bidirectional Barrel Shifter

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***Abstract*—Embedded digital signal processors and general purpose processors will use barrel shifters to manipulate data. This paper will present the design and implementation of the barrel shifter that performs logical shift right, arithmetic shift right, rotate right, logical shift left, arithmetic shift left, and rotate left operations. The main objective of the upcoming designs is to increase the performance without proportional increase in power consumption. In this regard reversible logic has become most popular technology in the field of low power computing, optical computing, quantum computing and other computing technologies. Device scaling is limited by the power dissipation; and demands better power optimizations methods. Techniques like Energy recovery, Reversible Logic are becoming more and more prominent special optimization techniques in Low Power VLSI designs. Rotating and data shifting are required in many operations such as logical and arithmetic operations, indexing and address decoding etc. The feynman gate will remove the fanout. By comparing the quantum cost, number of ancilla bits and number of garbage outputs the design is evaluated. The performance characteristics of the proposed design are evaluated, and the transistor cost, Garbage outputs and Quantum Cost are also calculated. The performance characteristics analysis is carried out in Xilinx environment.**

Keywords- barrel shifters, quantum cost, ancilla bits, verilog, garbage output, nanotechnology, quantum computing, fredkin gate, feynman gate.

I. INTRODUCTION

Rotating and shifting data is required in several applications including variable-length coding, arithmetic operations, and bit-indexing. Consequently, barrel shifters are capable of shifting or rotating data in a single cycle and are commonly found in both digital signal processors and general purpose processors. In reversible system information is not erased. Thus in reversible gates number of inputs and outputs are equal which means that the input stage can always be retained from the output stage. If a bit is erased in an irreversible circuit then it will dissipate kTln2 joules of heat energy where k is the Boltzmann's constant and T is the absolute temperature of environment [4]. There won't be dissipation of kTln2 joules of heat energy if the operations are performed in reversible manner based on reversible logic circuits [3]. Based on this observation, Bennett [3] showed, for a reversible computer the heat dissipation is exactly *kTln1* which is logically zero. Reversible logic also has the applications in emerging nanotechnologies such as quantum dot cellular automata, quantum computing, optical computing and low power computing, etc.

Low power design also plays a significant role in high-performance integrated circuits such as microprocessors and other high-speed digital computational circuits. The power consumption in microprocessors is projected to grow linearly in proportion to their die size and clock frequency. Various cooling systems have been introduced to reduce the heat from power dissipation and keep the chip temperature at an admissible level. This in turn has increased the packaging cost, which results in large revenue.

II. BASIC REVERSIBLE GATES

A ***Reversible Gate*** is an n-input, n-output circuit. To maintain the reversibility property of reversible logic gates several dummy output signals are needed to be produced in order to equal the number of input to that of output. These signals are commonly known as ***Garbage Outputs***. The quantum cost of reversible gate is equal to the number of 1x1 and 2x2 reversible gates needed to design a 3x3 reversible gate. The quantum cost of all 1x1 and 2x2 reversible gates are considered as unity [8], [7], [2]. The 3x3 reversible gates are designed from 1x1 NOT gate, and 2x2 reversible gates such as Controlled-V and Controlled-V+, the Feynman gate which is also known as Controlled NOT gate.

A NOT gate is 1x1 gate represented as shown in Fig. 1. Its quantum cost is unity since it is a 1x1 gate.

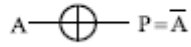


Fig. 1. NOT GATE

The input vector, *Iv* and output vector, *Ov* for 2*2 ***Feynman Gate (FE)*** is defined as follows: *Iv = (A, B)* and *Ov = (P = A* and *Q=A ^B)*. Feynman gates are typically used as copying gates. If *Iv = (A, B=0)* then *Ov = (P =A* and *Q=A)*. Fanout is not allowed in reversible logic. Feynman gate is helpful in this regard as it can be used for copying the signal by which it avoids the fanout problem as shown in Fig.2(c).

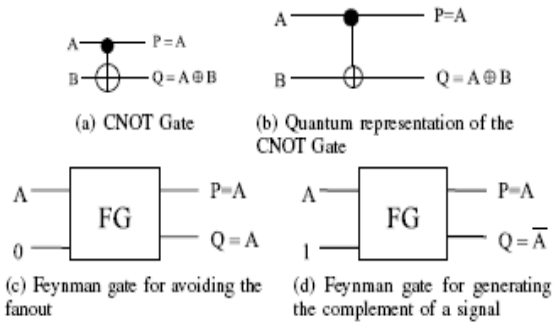


Fig. 2. CNOT gate, its quantum implementation and its useful properties

The input and output vector for 3*3 ***Fredkin gate (FR)*** [1] are defined as follows: *Iv* = (*A*, *B*,*C*) and *Ov =(P=A, Q= A'B^AC* and *R = A'C ^ AB)*. Figure 3(a) shows the block diagram of a Fredkin gate. A Fredkin gate can work as 2:1 MUX, as it is able to swap its other two inputs depending on the value of its first input. Thus when A=0 the outputs P and Q will be directly connected to inputs A and B and if A=1 the inputs B and C will be swapped resulting in the value of the outputs as Q=C and R=B.

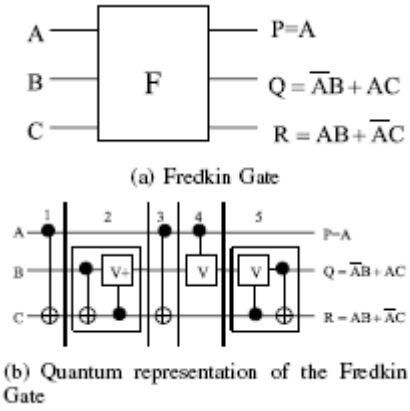


Fig. 3. Fredkin Gate and its quantum implementation

The quantum implementation of a Fredkin gate with a quantum cost of 5 is shown in Figure 3(b). In Fig. 3(b) each dotted rectangle is equivalent to a 2x2 Feynman gate and the quantum cost of each dotted rectangle is considered as 1 [8]. The same assumption is used for calculating the quantum cost of the Fredkin gate. Thus, the quantum cost of the Fredkin gate is 5 as it consists of 2 dotted rectangles, 1 Controlled-V gate and 2 CNOT gate.

III. Barrel Shifter

A Barrel shifter is an '*n*' input and '*n*' output combinational logic circuit in which k select lines controls the bit shift operation. Barrel shifter can be unidirectional allowing data to be shifted only to left (or right), or bi-directional which provides data to be rotated or shifted in both the directions. Among the different designs of barrel shifter, the logarithmic barrel shifter is most widely used because of its simple design, less area and the elimination of the decoder circuitry. The proposed work presents the design and implementation of reversible bidirectional arithmetic and logical barrel shifter that can perform six operations: logical right shift, arithmetic right shift, right rotate, logical left shift, arithmetic left shift and left rotate. The existing shifter is complex in design and requires large number of gates. As a result the total number of garbage outputs is high. Thus there is great room for improving the circuit complexity, total number of gates and garbage outputs, delay and quantum cost.

IV. Proposed Reversible Bidirectional Barrel shifter

The proposed design of reversible bidirectional barrel shifter can perform logical right & left shifting, arithmetic right & left shifting, rotating right & left operations. Table I shows that for different values of control signals sra, sla, rot and left the operations that can be performed by a (8,3) reversible bidirectional arithmetic and logical shifter.

TABLE I
Operation Performed By A (N, K) Reversible Bidirectional Barrel Shifter

Operation performed	Control signal values			
Logical right shift	Left=0	Rot=0	Sra=0	Sla=0
Arithmetic right shift	Left=0	Rot =0	Sra=1	Sla=0
Rotate right	Left=0	Rot=1	Sra=0	Sla=0
Logical left shift	Left=1	Rot=0	Sra=0	Sla=0
Arithmetic left shift	Left=1	Rot=0	Sra=0	Sla=1
Rotate left	Left=1	Rot=1	Sra=0	Sla=0

In this design, the input data is represented as i7, i6, i5, i4, i3, i2, i1, i0 while the shift value is controlled by select signals represented as S2S1S0 and the output data is obtained as shown in Table II .

TABLE II
Shift And Rotate Operation Output For K = 3

Operation	Y
3-bit shift right logical	0 0 0 a7a6a5a4a3
3-bit shift right arithmetic	a7a7a7a7a6a5a4a3
3-bit rotate right	a2a1a0a7a6a5a4a3
3-bit shift left logical	a4a3a2a1a0 0 0 0
3-bit shift left arithmetic	a7a3a2a1a0 0 0 0
3-bit rotate left	a4a3a2a1a0a7a6a5

The proposed reversible bidirectional arithmetic and logical barrel shifter design approach is illustrated as shown in Fig. 4 with an example of a (8,3) barrel shifter. The barrel shifter

performs the various operations such as logical right shift, logical left shift, rotate left etc. depending on the values of sra, sla rot and left control signals.

The design of a reversible barrel shifter can be divided into six modules: (i) Data reversal control unit-I, (ii) Arithmetic right shift control unit, (iii) Shifter or rotation unit which consists of three sub-modules that performs Stage I, Stage II and Stage III operations, (iv) Rotation unit, (v) Arithmetic left shift control unit, (vi) Data reversal control unit-II.

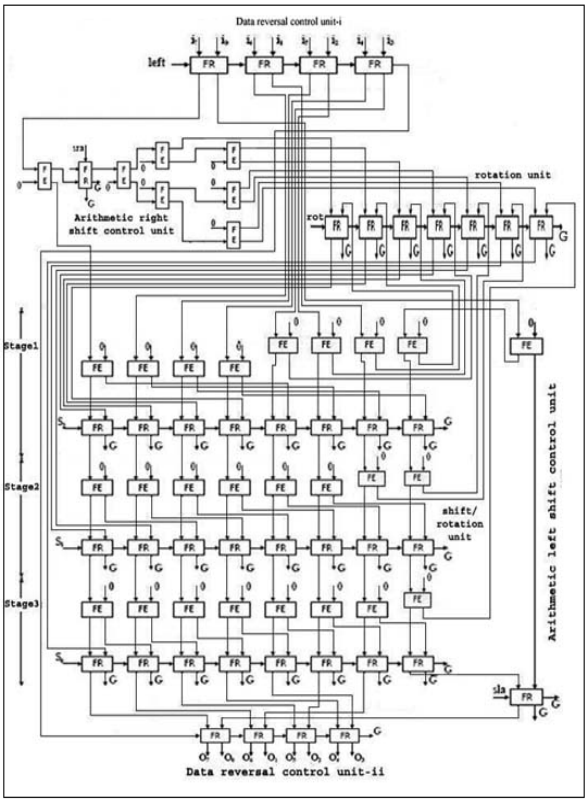


Fig. 4. Proposed (8,3) reversible bidirectional barrel shifter *FE represents Feynman Gates, FR represents Fredkin gates and G represents the garbage outputs

V. Performance Analization

To avoid the fanout problem, in the proposed design Feynman gate is used. Chains of n/2 Fredkin gates are used in data reversal unit-I and data reversal unit-II. The arithmetic right shift control unit uses one Fredkin and -1 Feynman gates. Chain of n Fredkin gates and n Feynman gates are used in shifter or rotation unit at each stage. Rotation unit fredkin gates for m=0 to (k-1) for each stage. One Fredkin gate and one Feynman gate is used in arithmetic left shift control unit.

A. Ancilla input Bits

The table III shows the number of ancilla bits required to design a reversible bidirectional barrel shifter for different values of n and k. +(n*k) Feynman gates are required to design a (n,k) reversible bidirectional barrel shifter. Each Feynman gate requires one ancilla input bit to copy the input data. Additionally, the Fredkin gate used in arithmetic right shift control unit requires one ancilla bit.

TABLE III
Ancilla Inputs In (N, K) Reversible Bidirectional Barrel Shifter

n/k	n=4	n=8	n=16	n=32	n=64
K=2	13	21	37	69	133
K=3		33	57	105	201
K=4			81	145	273
K=5				193	353
K=6					449

B. Quantum Cost

Table IV shows the quantum cost for a reversible bidirectional barrel shifter for different *n* and *k* values. The number of Feynman and Fredkin gates used will decide the quantum cost of (*n, k*) reversible bidirectional barrel shifter. The quantum cost of the Feynman gate is considered as one, while the quantum cost of the Fredkin gate is considered as five.

TABLE IV
Quantum Cost Of (N, K) Reversible Bidirectional Barrel Shifter

n/k	n=4	n=8	n=16	n=32	n=64
K=2	137	165	301	573	1117
K=3		237	421	789	1525
K=4			565	1029	1957
K=5				1317	2437
K=6					3013

C. Garbage Outputs

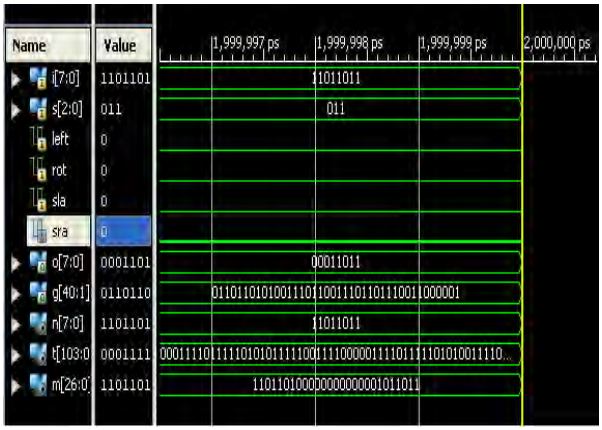
Each Fredkin gate in the chain of n Fredkin gates produces atleast one garbage output except the last Fredkin gate which produces two garbage outputs. Two garbage outputs are produced by Fredkin gate which is used in the design of arithmetic left shift control unit and arithmetic right shift control unit. One garbage output is produced by last Fredkin gate of the data reversal control unit-II as the control signal left cannot be utilized further.

TABLE V
Garbage Outputs In (N, K) Reversible Bidirectional Barrel Shifter

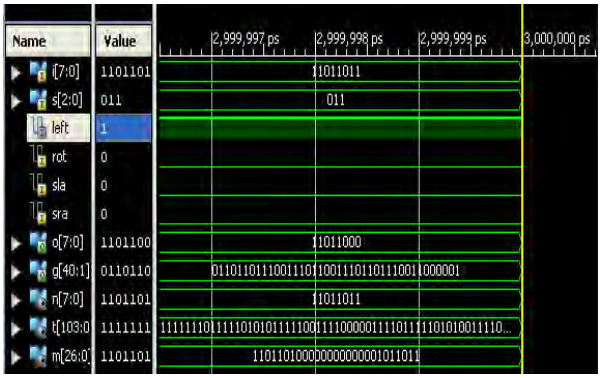
n/k	n=4	n=8	n=16	n=32	n=64
K=2	19	27	43	75	139
K=3		40	64	112	208
K=4			89	153	281
K=5				202	362
K=6					459

VII. Implementation And Results

The proposed design is functionally verified and the results are verified. The timing report was obtained after obtaining the netlist for the structural model of the digital implementation. The transistor cost was found in analog flow. Functionality was verified in Xilinx.



(a)



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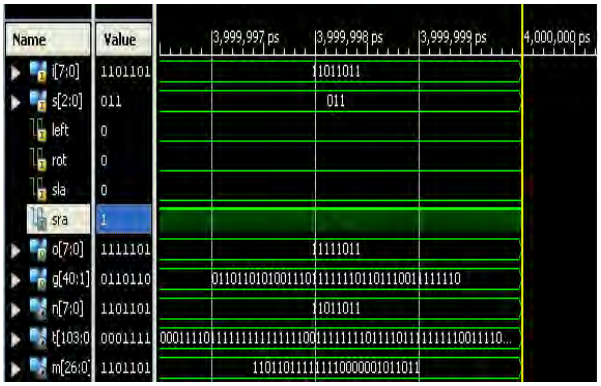
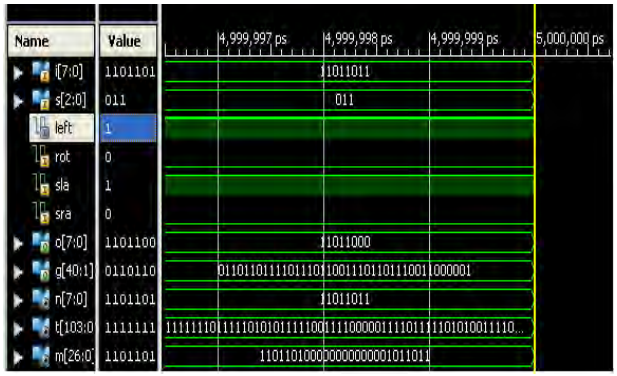
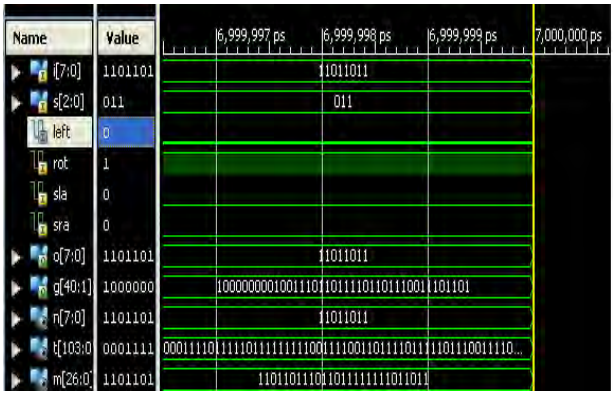


(c)



(d)



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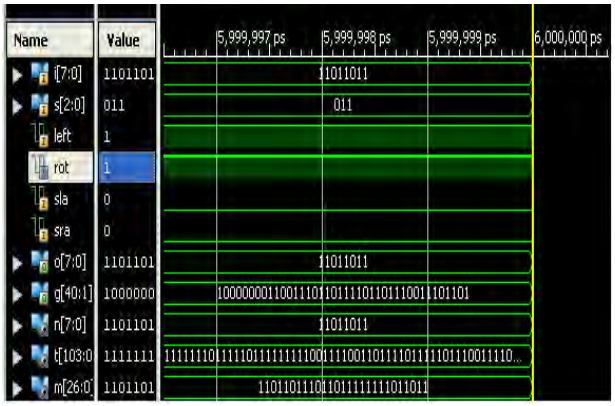

(f)

Figure.5: (a)-(f): A 8-bit bi-directional barrel shifter simulation result for all combinations outputs.

The universal barrel shifter is built by adding the rotation unit and the verification results are as follows. The schematic is a test circuit for input combination S=011, a square wave is applied to control signals to test for all the operations.

For the HDL structural design, the test vectors for excitation has been provided, and the response is as shown in Figure 5. Here the input reference vector is i=11011011.

Synthesis report

Final Results

RTL Top Level Output File Name : modbar.ngr
Top Level Output File Name : modbar
Output Format : NGC
Optimization Goal : Speed
Keep Hierarchy : No

Design Statistics

IOs : 63
Cell Usage :
BELS : 95
LUT2 : 8
LUT3 : 31
LUT4 : 51

MUXF5 : 5
IO Buffers : 63
IBUF : 15
OBUF : 48

Timing constraints

Delay: 12.638ns (Levels of Logic = 9)
Source: left (PAD)
Destination: o<5> (PAD)

Data Path: left to o<5>

Cell: in->out	Gate fanout	Net Delay	Delay	Logical Name (Net Name)
IBUF:I->O	23	1.106	1.174	left_IBUF (left_IBUF)
LUT3:I0->O	20	0.612	0.940	f1/Mxor_e_Result1 (n<7>)
LUT4:I3->O	3	0.612	0.454	f37/Mxor_e_Result1 (m<15>)
LUT4:I3->O	3	0.612	0.454	f15/Mxor_e_Result_and00011 (f15/Mxor_e_Result_and0001)
LUT4:I3->O	2	0.612	0.532	f23/f_and00011 (f23/f_and0001)
LUT4:I0->O	4	0.612	0.502	f33/e_and000011 (N3)
LUT4:I3->O	1	0.612	0.000	f33/Mxor_f_Result1 (f33/Mxor_f_Result)
MUXF5:I1->O	1	0.278	0.357	f33/Mxor_f_Result_f5 (o_2_OBUF)
OBUF:I->O	3.169			o_2_OBUF (o<2>)

VII. CONCLUSION

In this paper An Efficient Design of Reversible Logic Based Bidirectional Barrel Shifter has been proposed and implemented. The design of the proposed bidirectional shifter is done using Fredkin gates and Feynman gates. The number of garbage outputs, the number of ancilla inputs and the quantum cost of the (n,k) reversible bidirectional barrel shifter increase more rapidly by varying n and keeping k as a constant compared to the designs in which n is kept as a constant while k is varied. The functional verification of the proposed design of the reversible barrel shifters are performed through simulations using the Verilog HDL flow in Xilinx for reversible circuits. The design of bidirectional barrel shifter is been evaluated in terms of garbage outputs, ancilla inputs and the quantum cost. The proposed design of reversible bidirectional barrel shifter can perform logical right shifting, arithmetic right shifting, rotating right, logical left shifting, arithmetic left shifting and rotating left operations.

REFERENCES

[1] S. Kotiyal, H. Thapliyal, and N. Ranganathan "Design of a reversible bidirectional barrel shifter," in *Proc. of the 11th IEEE International Conference on Nanotechnology,* Portland, Oregon, USA, Aug 2011, pp. 463-468.

[2] I. Hashmi and H. Babu, "An efficient design of a reversible barrel shifter," in *VLSI Design, 2010. VLSID '10. 23rd International Conference on*, Jan 2010, pp. 93–98.

[3] S.Gorgin and A. Kaivani, "Reversible barrel shifters," in Proc. 2007 Intl. Conf. on Computer Systems and Applications, Amman, May 2007, pp. 479–483.

[4] C.H. Bennett, "Logical reversibility of computation," *IBM J. Research and Development*, vol. 17, pp. 525–532, Nov. 1973.

[5] A. Peres, "Reversible logic and quantum computers," *Phys. Rev. A, Gen. Phys.,* vol. 32, no. 6, pp. 3266–3276, Dec. 1985.

[6] S. Kotiyal, H. Thapliyal, and N. Ranganathan, "Design of a ternary barrel shifter using multiple-valued reversible logic," in *Proc. of the 10th IEEE International Conference on Nanotechnology*, Seoul, Korea, Aug. 2010, pp. 1104–1108.

[7] D. Maslov and D. M. Miller, "Comparison of the cost metrics for reversible and quantum logic synthesis," http://arxiv.org/abs/quantph/0511008, 2006.

[8] H. Thapliyal and N. Ranganathan, "Design of reversible sequential circuits optimizing quantum cost, delay and garbage outputs," *ACM Journal of Emerging Technologies in Computing Systems*, vol. 6, no. 4, pp. 14:1–14:35, Dec. 2010.