ĐẠI HỌC QUỐC GIA TP. HCM

TRƯỜNG ĐẠI HỌC BÁCH KHOA

MÔN HỌC: THIẾT KẾ VI MẠCH

BÁO CÁO LAB 1

MOS TRANSISTOR CHARACTERIZATION

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TP. HỒ CHÍ MINH, NĂM 2021

LABORATORY 1

MOS TRANSISTOR CHARACTERIZATION

OBJECTIVES

No.	Objective	Requirement
1	I-V characteristics of MOS transistors.	▪ Simulating curves $I_D\ vs\ V_{GS}$, and $I_D\ vs\ V_{DS}$ of *NMOS_VTL* and *PMOS_VTL* transistors.
2	The effects on I-V characteristics when varying: ➢ V_{GS}. ➢ Device's size.	▪ Simulating curves $I_D\ vs\ V_{GS}$, and $I_D\ vs\ V_{DS}$ of *NMOS_VTL* transistor, then observing the curves drawn.
3	Create layouts for MOS transistors.	▪ Create layouts for a *120n/60n NMOS_VTL* and a *50n/50n PMOS_VTL*. ▪ Show DRC confirmation and corresponding schematic with proof of LVS.

PREPARATION FOR LAB 1

- Students **must finish** lab 0 at home.

EXPERIMENT 1

Objective: Known MOS transistor operations and I-V curves.

Requirements: Procedure $I_D\ vs\ V_{GS}$, and $I_D\ vs\ V_D$ plots of NMOS_VTL and PMOS_VTL in FreePDK45.

Instructions: Assemble the circuit as shown in **Figure 1**, setting parameters for power supplies (using **vdc** source).

Check: Your report must show these results for both NMOS_VTL transistors.

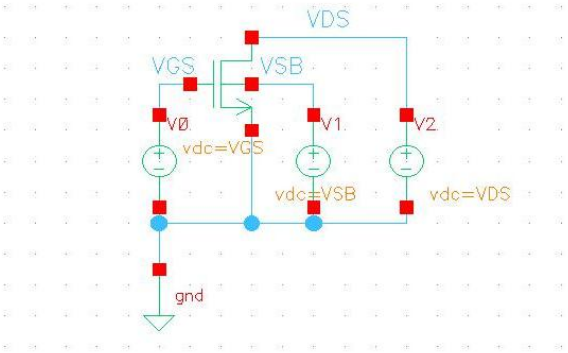
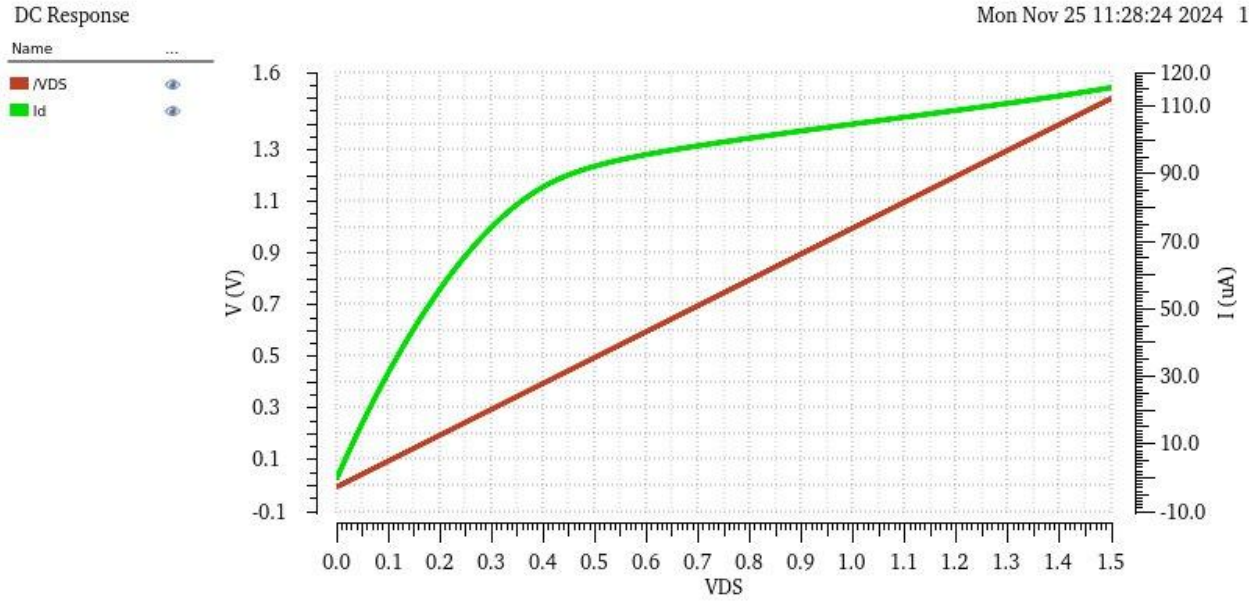
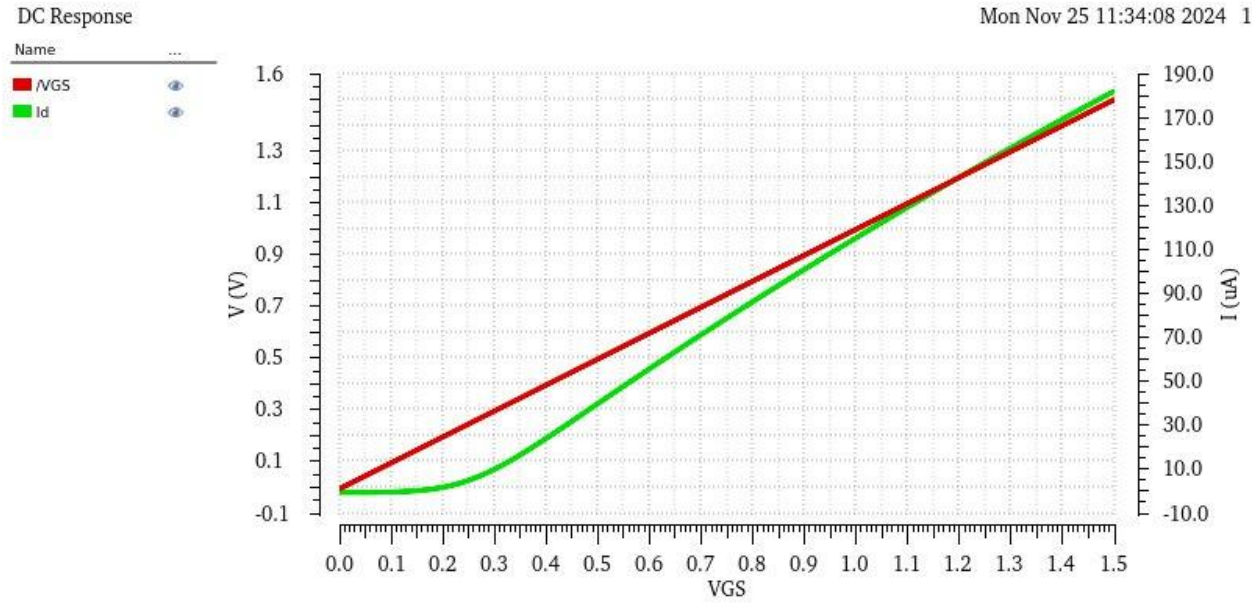


Figure 1 Test setup for the NMOS_VTL transistor.

- Simulate **curves $I_D\ vs\ V_{DS}$** @ V_{GS} = 1V, and sweeping variable V_{DS} = [0,1.5]V step 10mV.



- Simulate **curves I_D vs V_{GS}** @ V_{ds} = 1.5V, and sweeping variable V_{gs} = [0,1.5]V step 10mV.



Check: Your report must show these results for both PMOS_VTL transistors.

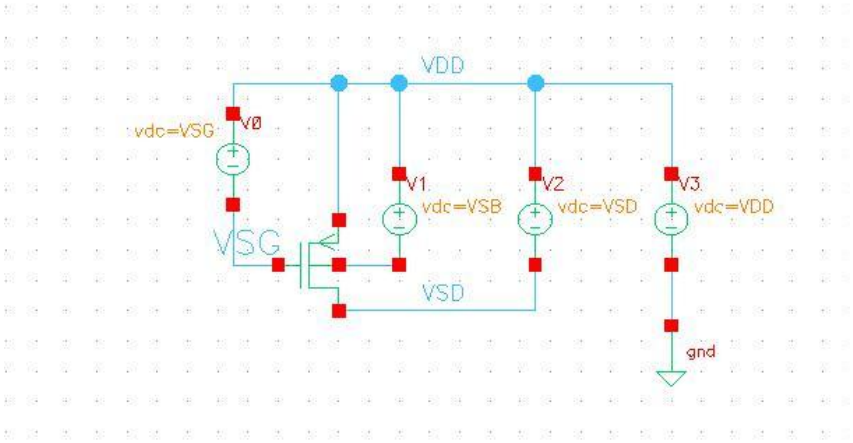
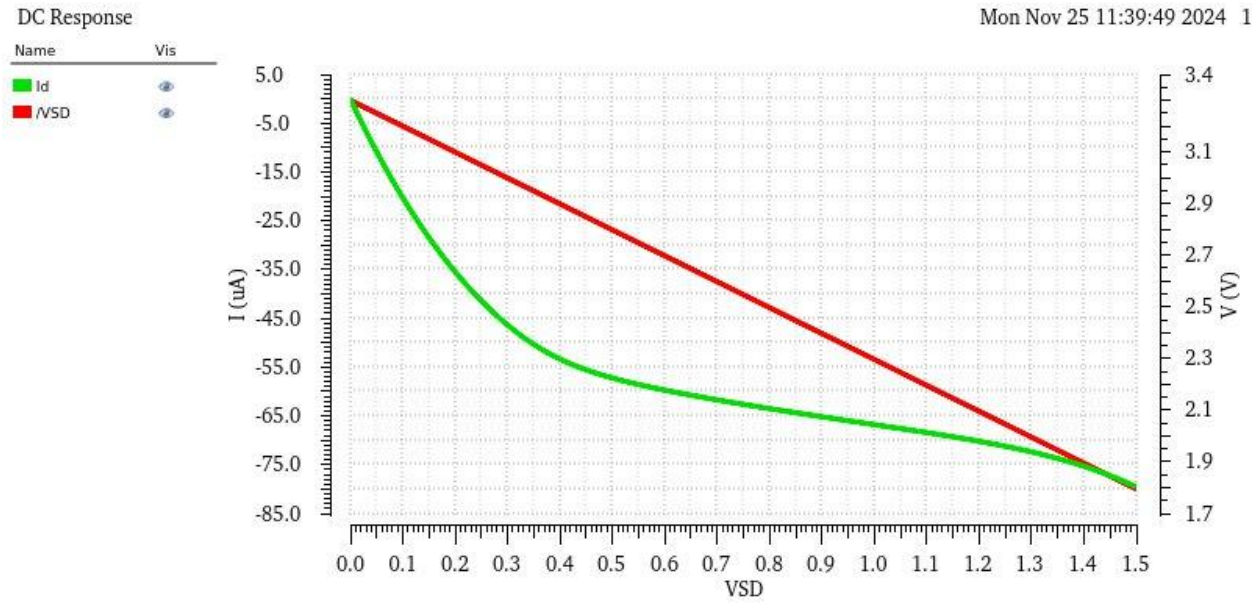
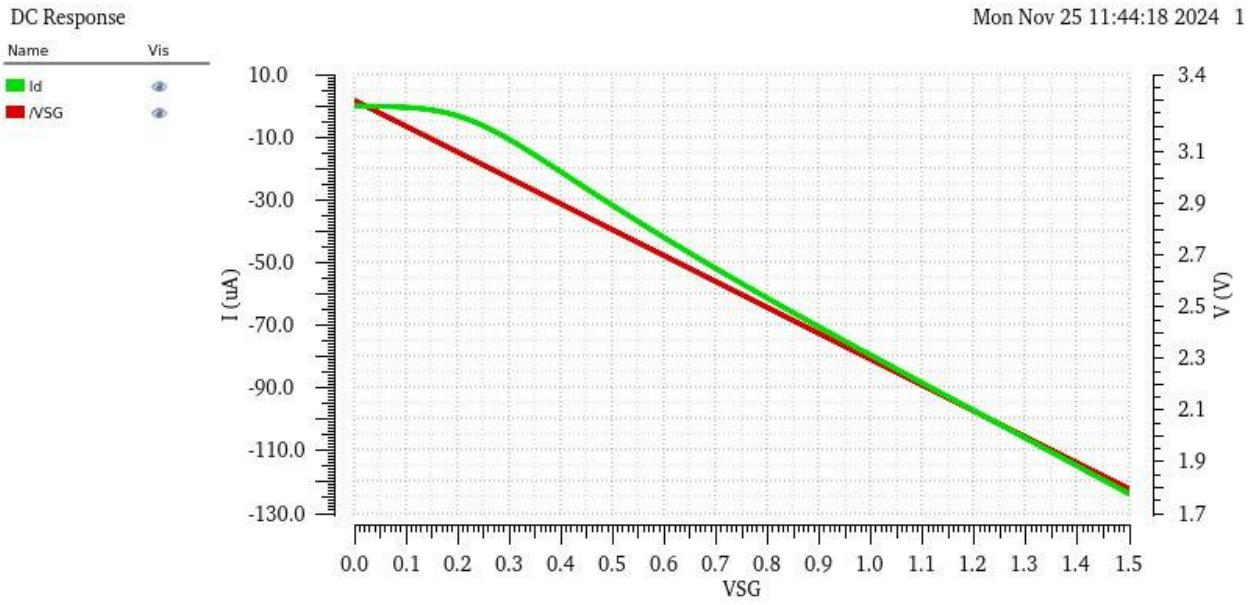


Figure 2 Test setup for PMOS_VTL transistor.

- Simulate **curves I_D vs V_{DS}** @ V_{GS} = 1V, and sweeping variable V_{DS} = [0,1.5]V step 10mV.



- Simulate **curves I_D vs V_{GS}** @ V_{ds} = 1.5V, and sweeping variable V_{gs} = [0,1.5]V step 10mV.



EXPERIMENT 2

Objective: The effects on IV characteristics when varying V_{GS}, and the device's size. ***Requirements:*** Simulate curves I_D *vs* V_{DS} and I_D *vs* V_{DS} when varying V_{GS}, and device's size. ***Instructions:***

- Replace the default size of the NMOS transistor with variables W, and L, respectively. It means your testbench has five parameters W, L, V_{GS}, V_{DS}, and V_{SB} shown in the figure below.

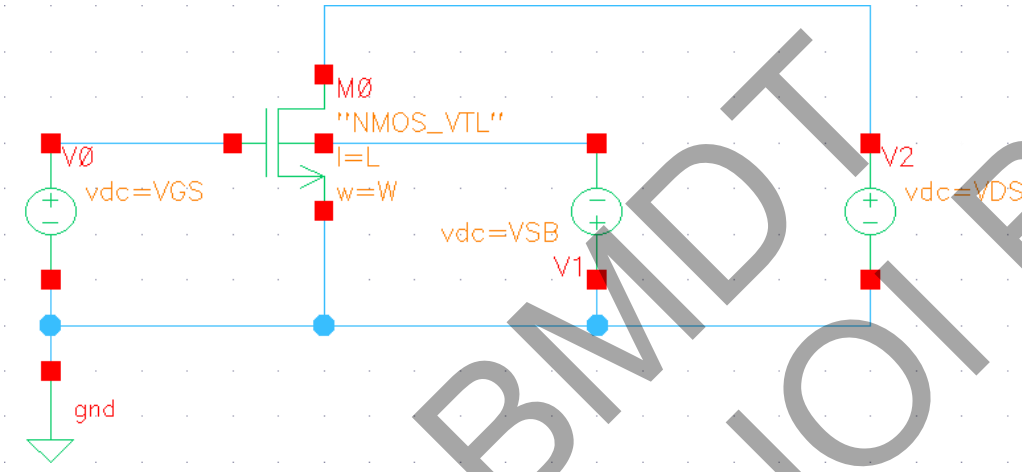


Figure 3 Testbench for experiment 2.

- In ADE-L, students open Parametric Analysis to sweep multiple variables:

Tool > Parametric Analysis > Run mode > Sweeps & Ranges

- **Parametric analysis** is used when two or more independent variables are present in a single function. Students can have the standard X-Y plot of I_D versus V_{DS} with a constant V_{GS}. But students need to plot the same X-Y plot multiple times for each of the discrete V_{GS} values. Students can refer to the settings and results in the figures below:

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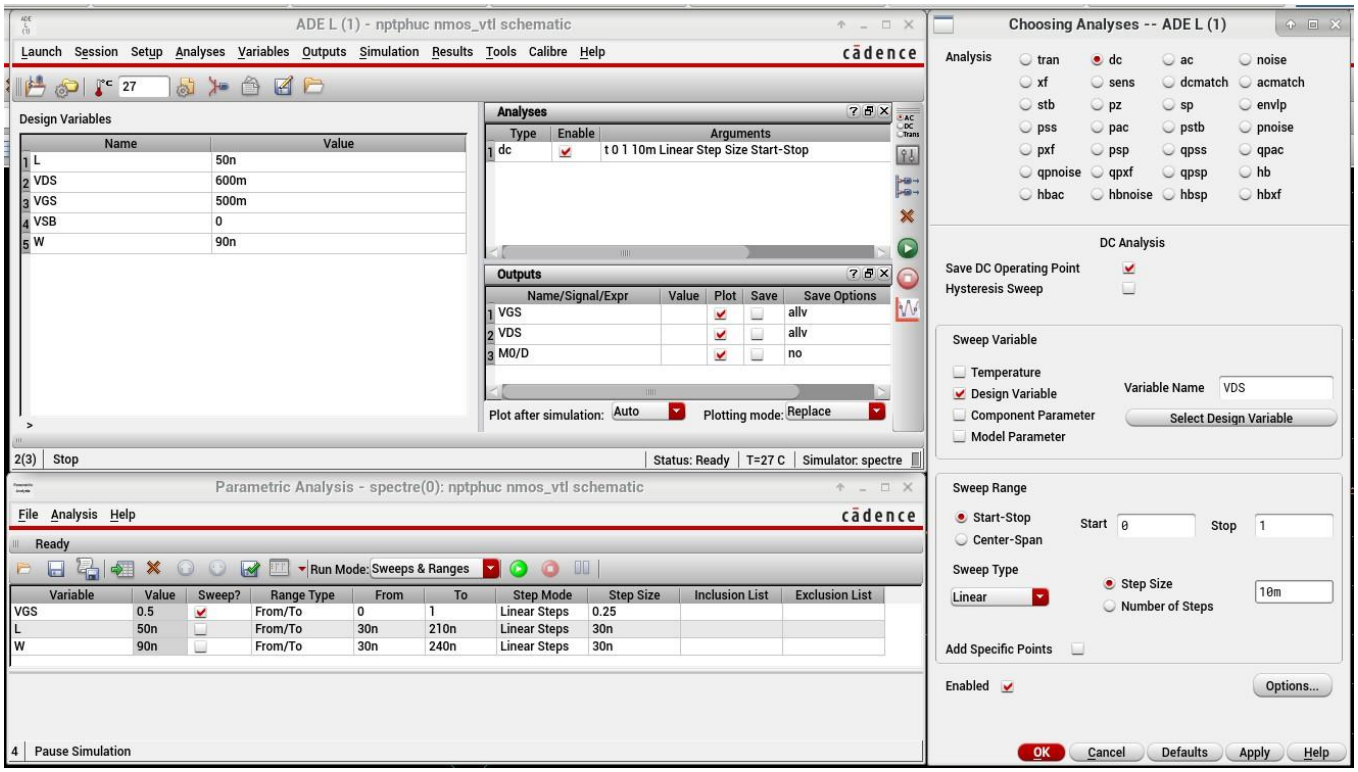


Figure 4 Setting parameters for characterizing $I_D \; vs \; V_{DS} \; @ \; V_{GS} = \{0, 0.25, 0.5, 0.75, 1.0\} \; V$

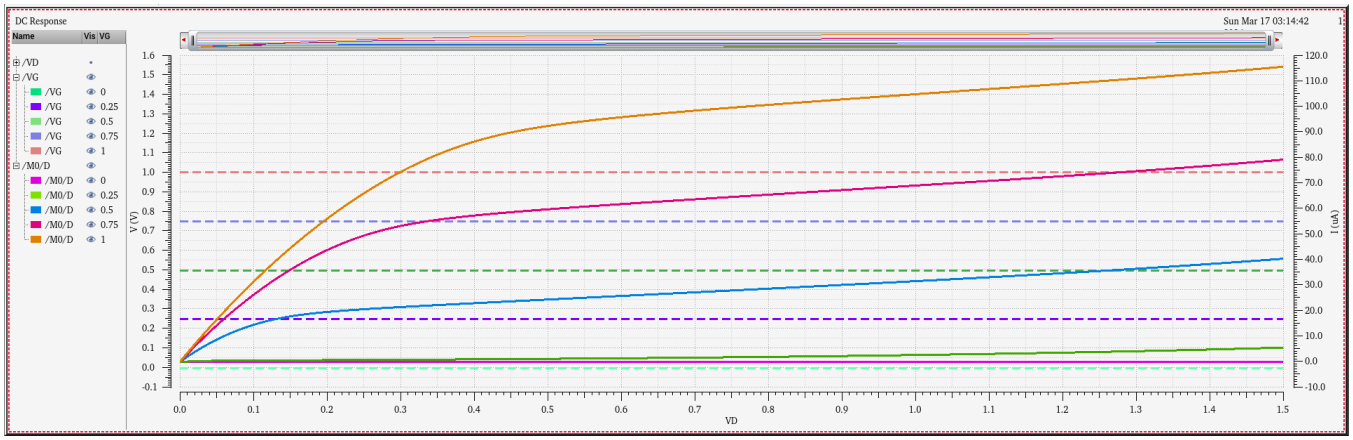
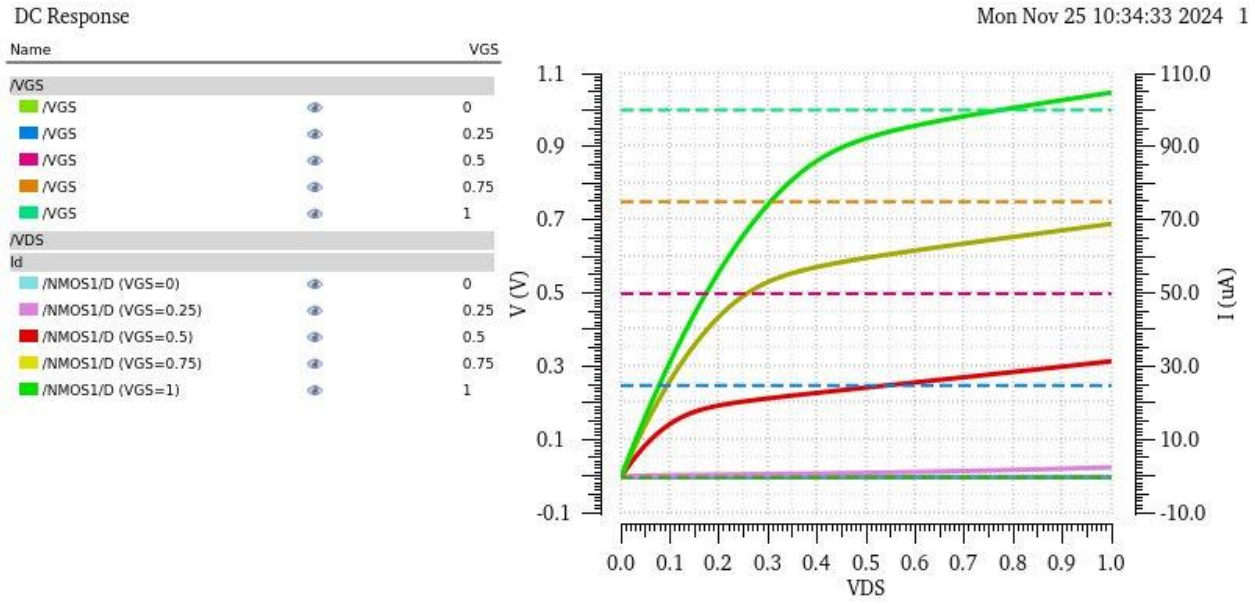


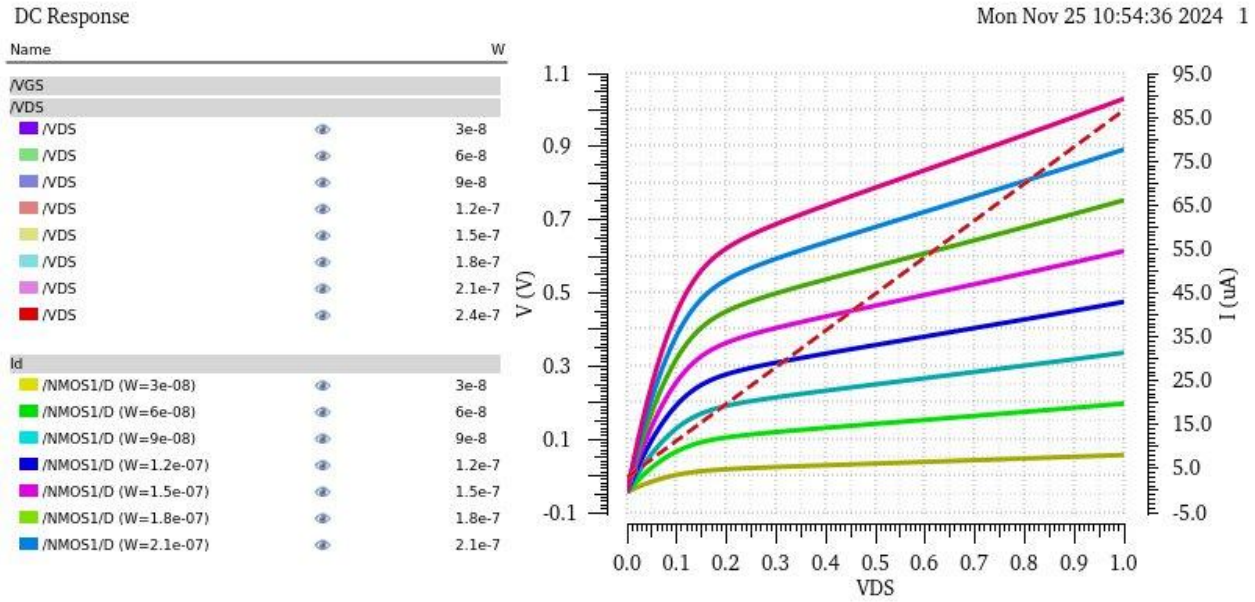
Figure 5 $I_D \; vs \; V_{DS} \; @ \; V_{gs} = [0,1] \; V$ step 0.25V.

Check: Your result must show these results.

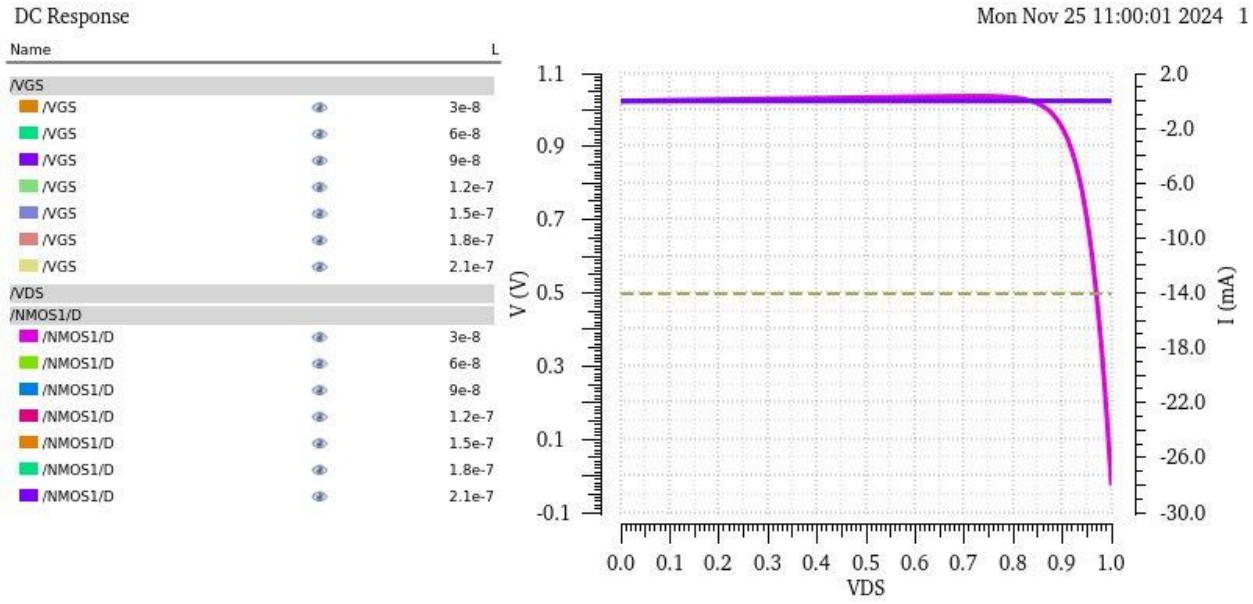
- Simulate curves $\boldsymbol{I_D \; vs \; V_{GS}} \; @ \; V_{gs} = [0,1] \; V$ step 0.25V.



- Simulate curves $\boldsymbol{I_D\ vs\ V_{DS}}$ @ W = [30,210] nm step 30nm.



- Simulate curves $\boldsymbol{I_D\ vs\ V_{DS}}$ @ L = [30,240] nm step 30nm.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EXPERIMENT 3

Objective: Create layouts for MOS devices.

Requirements:

- Create layout of a 120n/60n NMOS_VTL and a 50n/40n PMOS_VTL.
- Show DRC confirmation and corresponding schematic with proof of LVS.

Instructions:

➢ In this experiment, students will consider how the transistors are built. Designers need to understand the physical implementation of circuits because it has a major impact on performance, power, and cost. Easiest to understand by viewing both top and cross-section of a wafer in a simplified manufacturing process, where:

One is the top view, obtained by looking down on a wafer.

The other is the cross-section, obtained by slicing the wafer through the middle of a transistor and looking at it edge-wise.

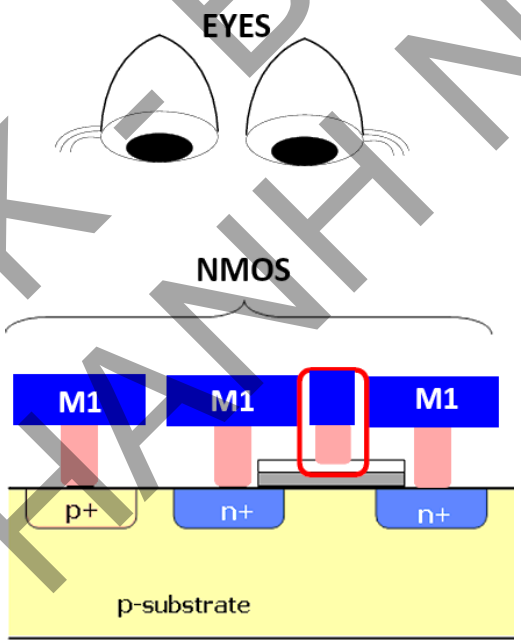

Figure 6 Cross section of an NMOS transistor.

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➢ Students begin by looking at the cross-section of a complete NMOS transistor, then look at the top view of the same NMOS transistor and define a set of masks used to manufacture the different parts of the NMOS transistor.

➢ According to layout instructions in lab 0, this lab only mentions layout steps to perform.

1. Add **n-active** (n-islands).

2. Add Poly (**PO**) for the gate.
3. Make drain, source, and bulk connections (contacts).
4. Create **pwell**.
5. Overlap the two active regions with the correct types of **implants**.
6. Create contacts for four terminals (**metal1**).

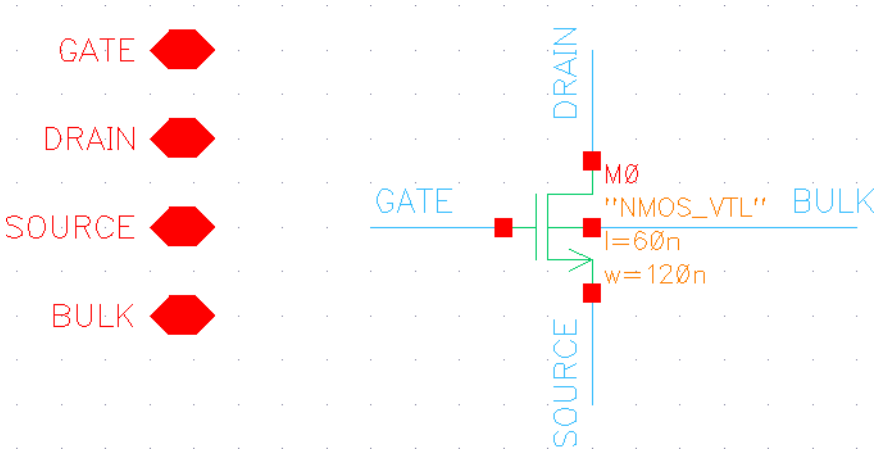
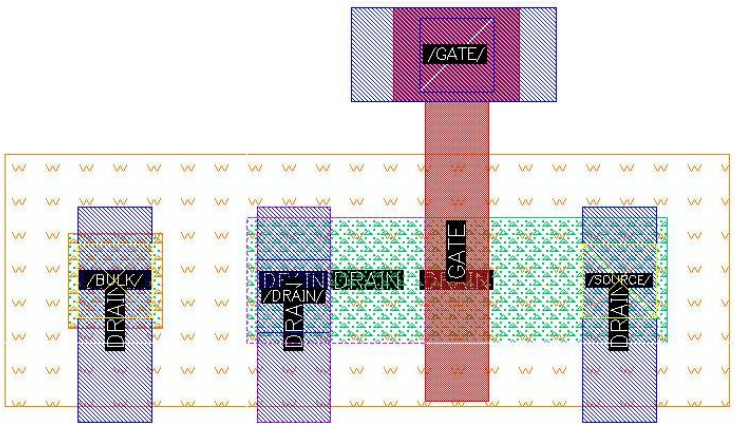
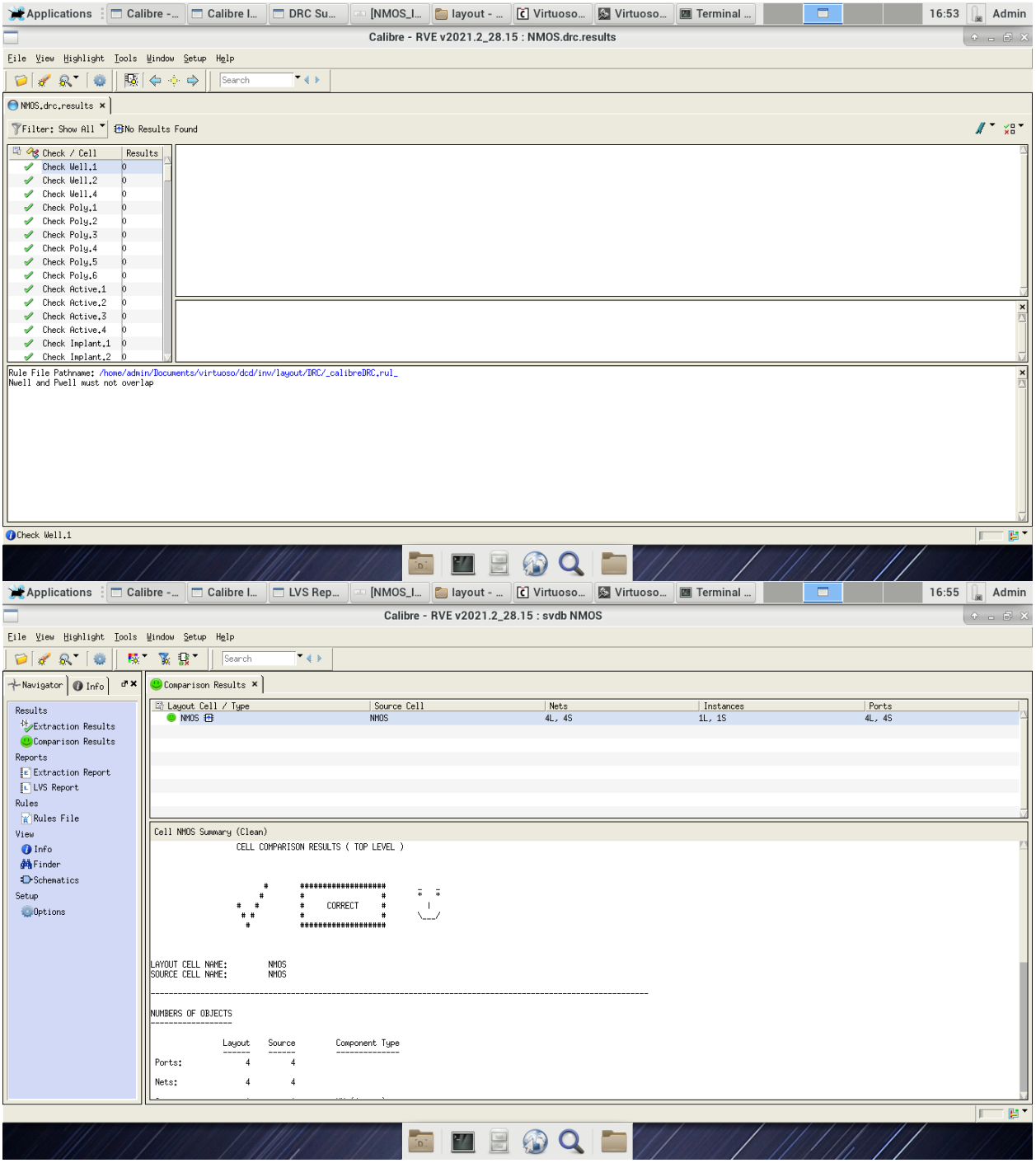


Figure 7 NMOS schematic.

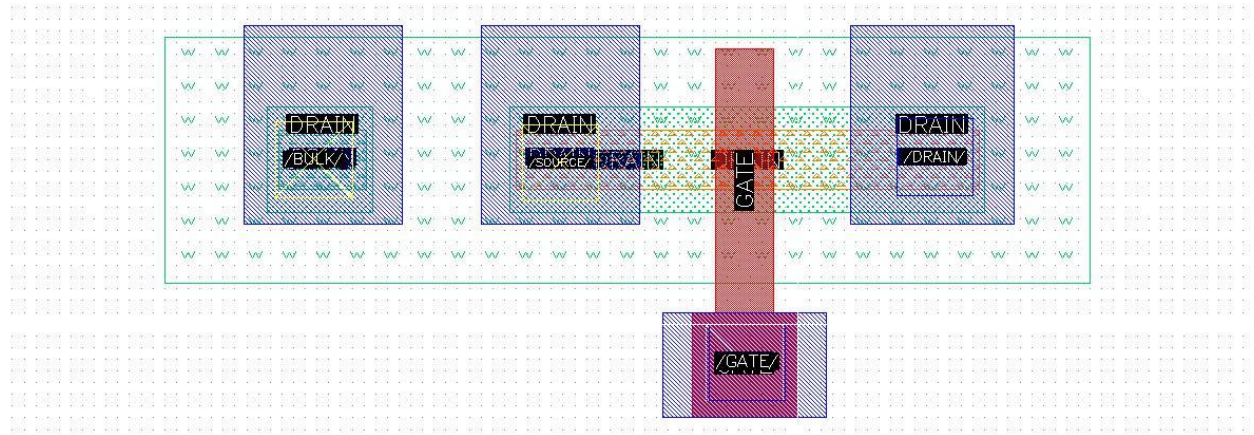
Check:

➢ Layout of a 120n/60n NMOS_VTL with DRC confirmation and corresponding schematic with proof of LVS.





➢ Layout of a 50n/50n PMOS_VTL with DRC confirmation and corresponding schematic with proof of LVS.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Applications
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Check Active.4
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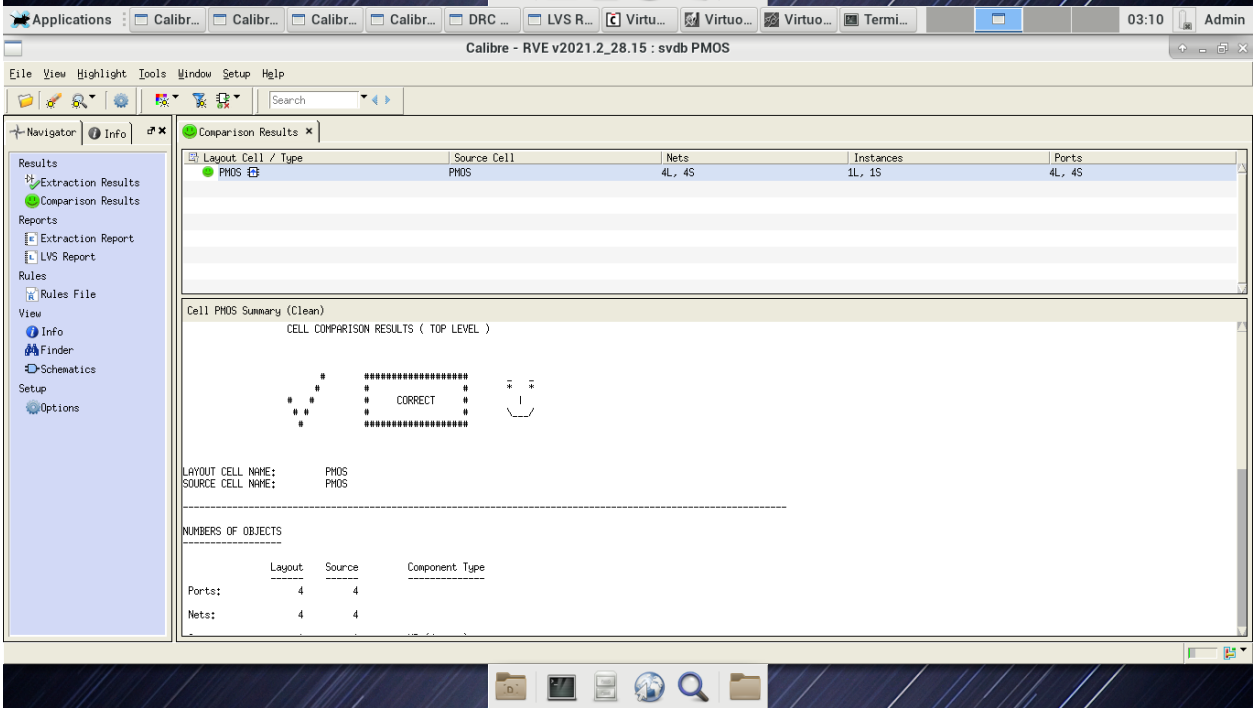
Nwell and Pwell must not overlap
Check Well.1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Admin
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LVS Report
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Finder
Schematics
Setup
Options
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Nets
Instances
Ports
PMOS
PMOS
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1L, 1S
4L, 4S
Cell PMOS Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: PMOS
SOURCE CELL NAME: PMOS
NUMBERS OF OBJECTS
Layout
Source
Component Type
Ports: 4 4
Nets: 4 4