LABORATORY 1
MOS TRANSISTOR CHARACTERIZATION

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OBJECTIVES

No.	Topics	Requirements
1	I-V characteristics of MOS transistors.	Simulate the I_D vs V_{GS} and I_D vs V_{DS} characteristics of NMOS_VTG and PMOS_VTG using FreePDK45.
2	Effects of varying V_{GS} and device size.	Simulate the I_D vs V_{GS} and I_D vs V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45 and analyze the impact of these parameters.
3	Second-order effects (Body effect, Channel-length modulation).	Simulate the I_D vs V_{GS} and I_D vs V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45 and analyze the impact of these parameters. Measure and analyze device characteristics: λ, γ, k_p.
4	Layout design for MOS transistors.	Design the layout for a 120n/60n NMOS and a 50n/40n PMOS transistor. Verify the design by performing Design Rule Check (DRC) and ensuring Layout Versus Schematic (LVS) confirmation.

PREPARATIONS

- Students must finish laboratory 0.
- Summarize the operating regions of NMOS according to the following table:

Conditions	Equation current I_D of NMOS	The operating region of NMOS
$V_{GS} < V_{TH}$	$I_D = 0$	Cutoff
$V_{GS} \geq V_{TH}$ $V_{DS} < V_{GS} - V_{TH}$	$I_D = k' \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$	Triode
$V_{GS} \geq V_{TH}$ $V_{DS} \geq V_{GS} - V_{TH}$	$I_D = \frac{1}{2} k' \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$	Saturation

Table 1: Operating regions of NMOS

EXPERIMENT 1

Objective: I-V characteristics of MOS transistors.

Requirements: Simulate the I_D vs V_{GS} and I_D vs V_{DS} characteristics of NMOS_VTG and PMOS_VTG transistors using FreePDK45.

Instructions: For example, design a testbench similar to **Figures 1 and 2** to characterize the devices, maintaining the default device dimensions ($W/L = 90n/50n$). Based on Lab 0, students should obtain results corresponding to the curves shown in **Figures 3 and 4**.

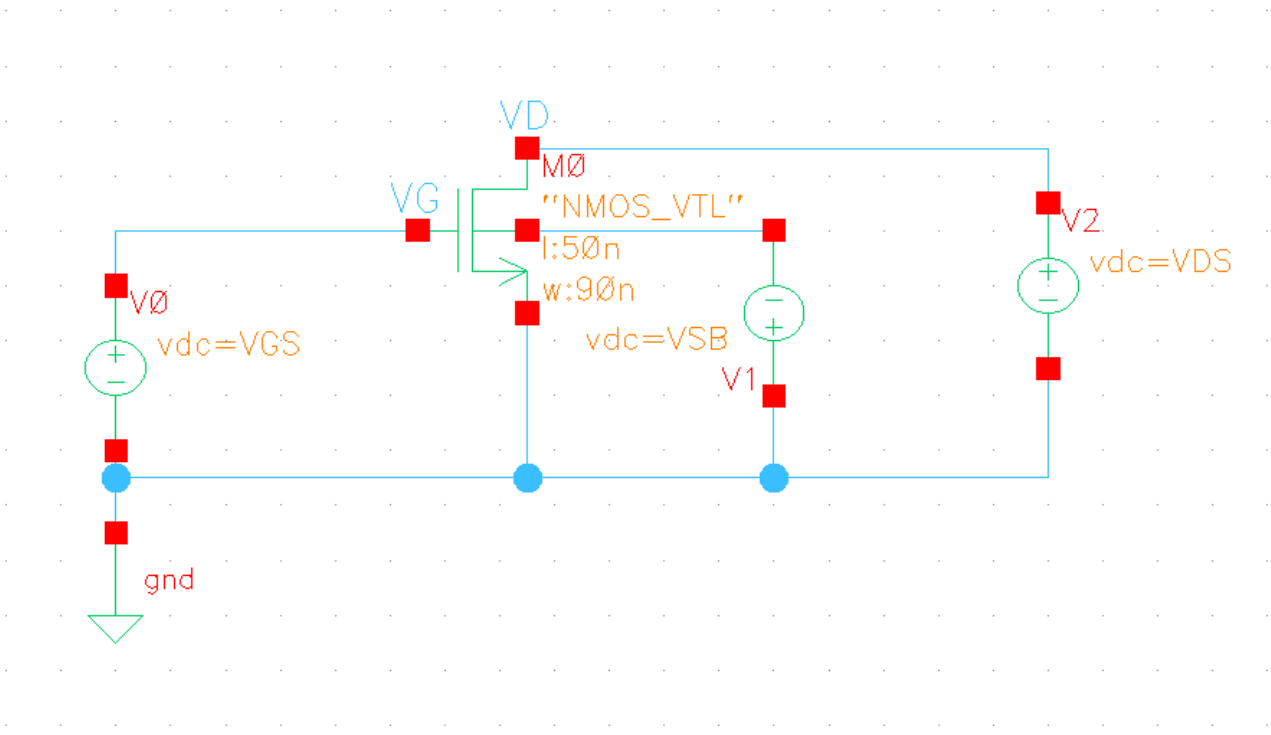

Figure 1: Test setup for the NMOS transistor.

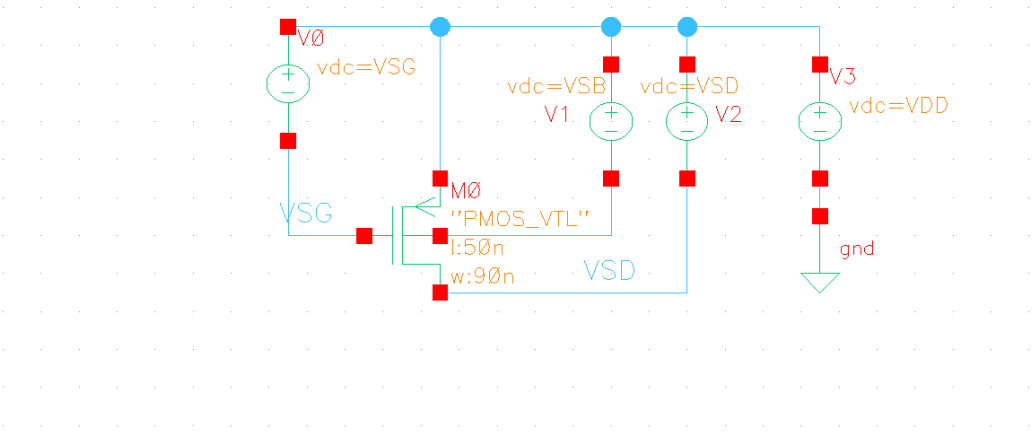

Figure 2: Test setup for the PMOS transistor.

Check: Your report must include the results for NMOS_VTG transistor. Additionally, provide a discussion on your simulation findings.

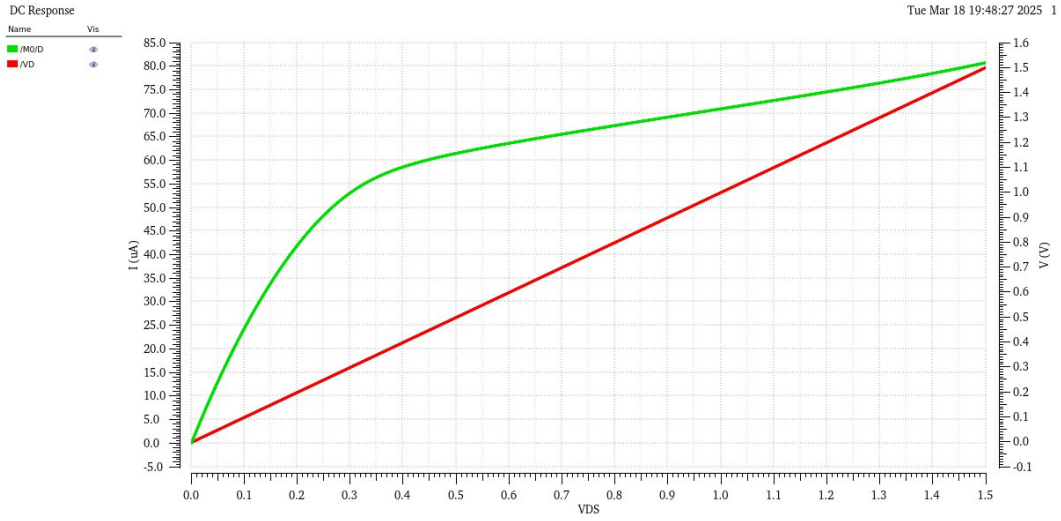

Figure 3: Simulate curves I_D vs V_{DS} @ $V_{GS} = 1V$, and sweeping variable $V_{DS} = [0, 1.5]V$ step 10mV.

When V_{DS} is small, the drain current I_D increases linearly with V_{DS} and gradually reaches the saturation region. At this point, I_D no longer increases linearly with V_{DS}; instead, it only rises slightly as V_{DS} increases due to the Channel Length Modulation effect, rather than remaining constant (fully saturated). The Channel Length Modulation effect occurs when V_{DS} increases, causing the conductive channel length from the source to the drain to shrink due to the influence of a strong electric field.

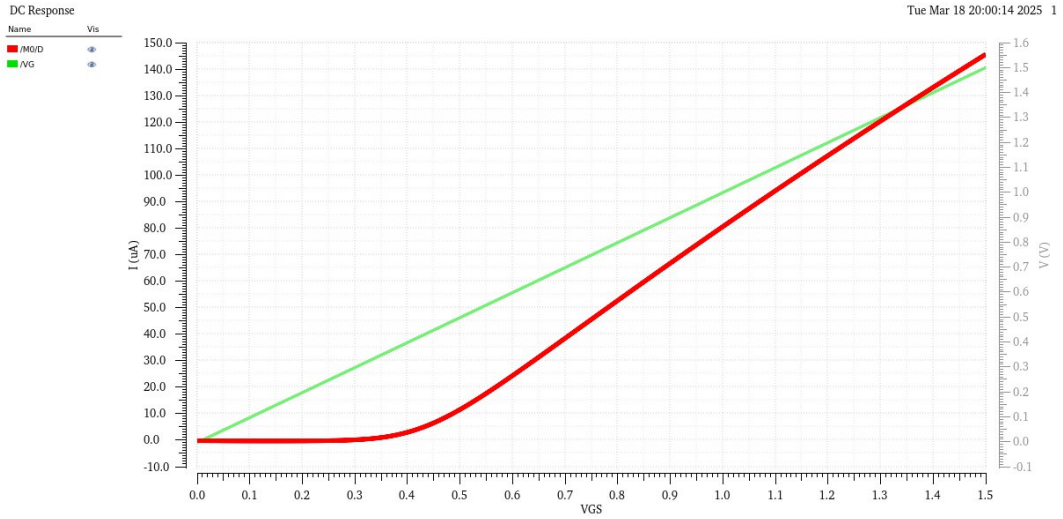

Figure 4: Simulate curves I_D vs V_{GS} @ $V_{DS} = 1.5V$, and sweeping variable $V_{GS} = [0, 1.5]V$ step 10mV.

To form a conducting channel, we need a sufficiently large V_{GS} (exceeding V_{TH}). When V_{GS} is small, it is the cut-off region, where $I_D = 0$. When V_{GS} ¿ V_{TH}, it enters the linear region (I_D increases linearly with V_{GS}).

Check: Your report must include the results for PMOS_VTG transistors. Additionally, provide a discussion on your simulation findings.

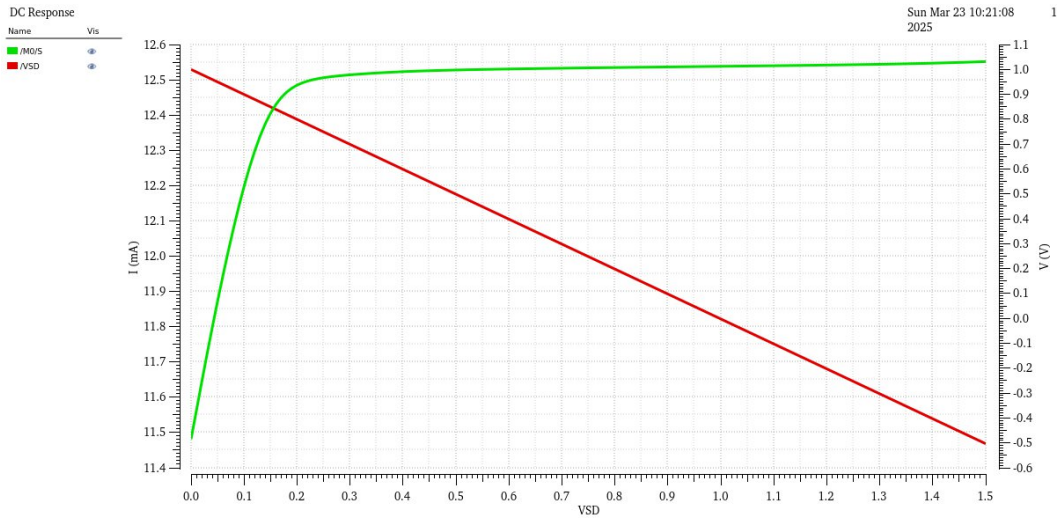

Figure 5: Simulate curves I_D vs V_{DS} @ $V_{SG} = 1V$, and sweeping variable $V_{SD} = [0, 1.5]V$ step 10mV.

For VSD from 0 to 0.3 V, I_d increases linearly. After 0.3 V, it's the saturation region where I_d almost doesn't change value anymore and stays constant even though V_{DS} continues to increase.

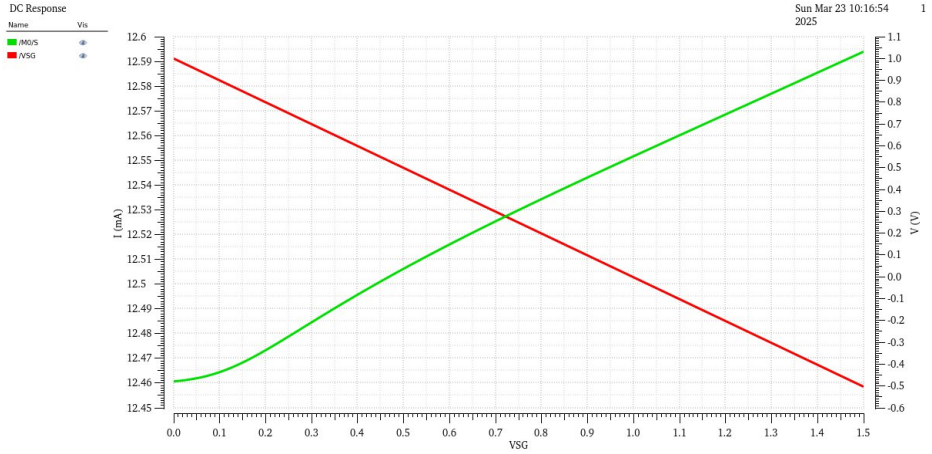

Figure 6: Simulate curves I_D vs V_{GS} @ $V_{SD} = 1.5V$, and sweeping variable $V_TSG = [0, 1.5]V$ step 10mV.

When $V_{SG} < |V_{THp}|$, the PMOS is in cutoff mode ($I_d = 0$). When $V_{GS} > |V_{THp}|$ and $V_{SD} < V_{GS} + |V_{THp}|$, it operates in the linear mode, and I_D runs from S to D ($I_D < 0$) increasing linearly with V_{SD}.

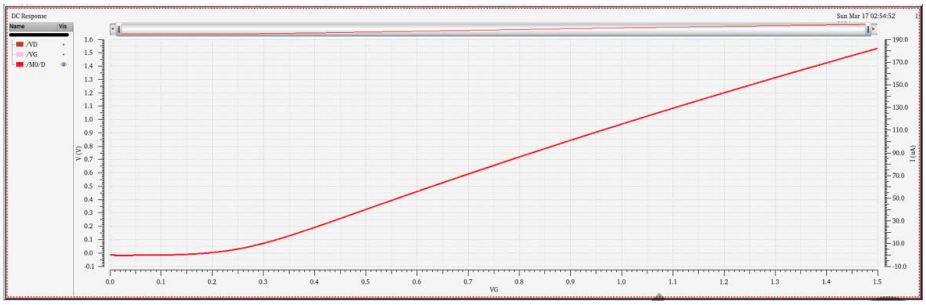

Figure 7: I_D vs V_{GS} of NMOS @ $V_{DS} = 1.5$V.

Q1. Based on the characteristics, please estimate the threshold voltage of the NMOS transistor. According to the figure, when V_{GS} exceeds 0.2 V, I_d increases linearly. We can estimate $V_{TH} = 0.3V$

Considering the region where $V_{GS} < 0.2V$, the drain current I_D is almost zero, which represents the cut-off region of the NMOS.

Q2. Based on the characteristics, please estimate the threshold voltage of the NMOS transistor.

Considering the region where $V_{GS} > 0.2V$, for it to be the conduction region, $V_{DS} < V_{GS} - V_T$. Given $V_{DS} = 1.5V$ and $V_T = 0.2V$, we can deduce that $V_{GS} > V_{DS} + V_T = 1.5 + 0.2 = 1.7V$ for the linear region.

For it to belong to the saturation region, $V_{GS} < 1.7V$ and $V_{GS} > 0.2V$. Therefore, on the characteristic curve, there are three regions:

$V_{GS} < 0.2V$: cut-off region (off)

$0.2V < V_{GS} < 1.7V$: saturation region (on)

$V_{GS} > 1.7V$: linear region (on)

Q3. Based on Figure 3, qualitatively determine the operating regions of the NMOS transistor.

The **cutoff region** is not observed in this graph, as $I_D > 0$ for all V_{DS} values, indicating that $V_{GS} = 1V$ is above the threshold voltage V_{th}. The NMOS transistor operates in the **triode region** for V_{DS} from $0V$ to approximately $0.4V$ to $0.5V$, where I_D increases significantly with V_{DS}. The transistor enters the **saturation region** for V_{DS} from approximately $0.5V$ to $1.5V$, where I_D becomes relatively constant, with a slight increase due to channel-length modulation.

Q4. When the NMOS transistor is biased in the saturation region, does the drain current remain constant? Provide a theoretical explanation.

In the saturation region, which occurs when $V_{DS} \geq V_{GS} - V_{th}$, the channel of the NMOS transistor is pinched off near the drain end. The ideal model for the drain current in saturation is given by:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2$$

where:

- μ_n: Electron mobility,
- C_{ox}: Oxide capacitance per unit area,
- W/L: Width-to-length ratio of the channel,
- V_{GS}: Gate-to-source voltage,
- V_{th}: Threshold voltage.

In this ideal model, I_D depends only on V_{GS} and V_{th}, and is independent of V_{DS}. This suggests that the drain current should remain constant as V_{DS} increases, assuming V_{GS} is fixed. This behavior arises because, in saturation, the channel is pinched off, and the effective channel length no longer changes with V_{DS}. The electric field in the pinched-off region accelerates carriers, but the current is limited by the channel near the source, which is controlled by V_{GS}.

As V_{DS} increases, the pinch-off point moves closer to the source, effectively reducing the channel length L. This reduction in L increases the W/L ratio, which in turn increases I_D. The effect of channel-length modulation modifies the drain current equation as follows:

$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$ where λ is the channel-length modulation parameter (a small positive constant). The term $(1 + \lambda V_{DS})$ indicates that I_D increases slightly with V_{DS}, leading to a small positive slope in the I_D vs. V_{DS} curve in the saturation region.

Q4. Propose methods to reduce the slope of the drain current when the NMOS operates in the saturation region.

Increase the Channel Length L The channel-length modulation parameter λ is inversely proportional to the channel length L. By increasing L, the value of λ decreases, which reduces the term $(1 + \lambda V_{DS})$, thereby decreasing the slope of I_D with respect to V_{DS}. A longer channel length makes the pinch-off region a smaller fraction of the total channel, reducing the relative impact of channel-length modulation. However, increasing L may reduce the transistor's speed (due to increased transit time for carriers) and increase the area occupied by the transistor on the chip.

Operate at Lower V_{DS} **Values** Since the slope of I_D is proportional to λV_{DS}, operating the transistor at a lower V_{DS} (while still ensuring it remains in the saturation region, i.e., $V_{DS} \geq V_{GS} - V_{th}$) can reduce the slope. This method involves careful biasing of the circuit to keep V_{DS} as low as possible within the saturation region. However, this approach may limit the voltage headroom in the circuit and may not be feasible in applications requiring a large output voltage swing.

Use Feedback Circuits Negative feedback can be employed in the circuit to stabilize the drain current. For example, a current mirror or a feedback loop can be designed to sense changes in I_D and adjust the gate voltage V_{GS} to counteract the increase in I_D due to channel-length modulation. This method does not reduce λ directly but compensates for its effect, resulting in a flatter I_D vs. V_{DS} characteristic.

EXPERIMENT 2

Effects of varying VGS and device size

NMOS:

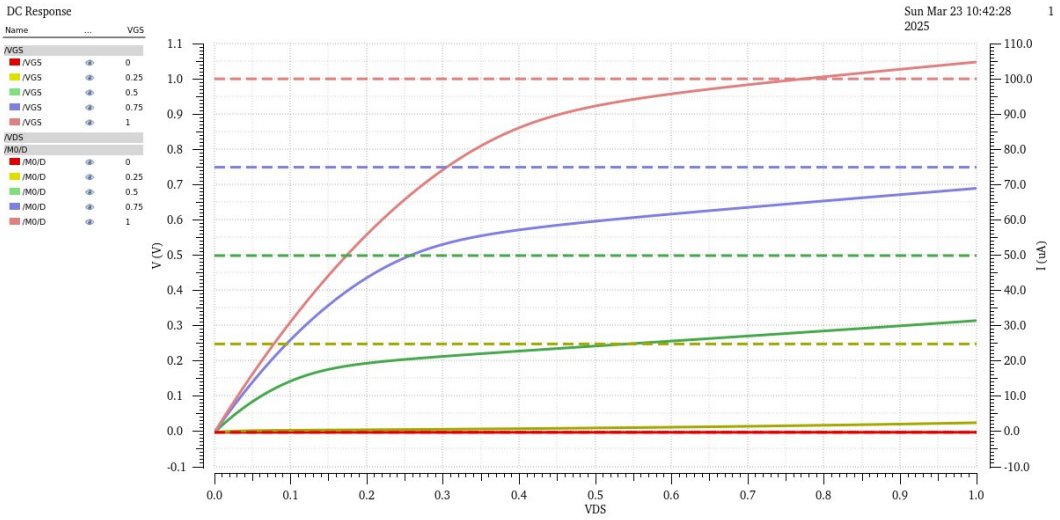

Figure 8: I-V Characteristics of NMOS: V_{GS} [0V - 1V], step 0.25V.

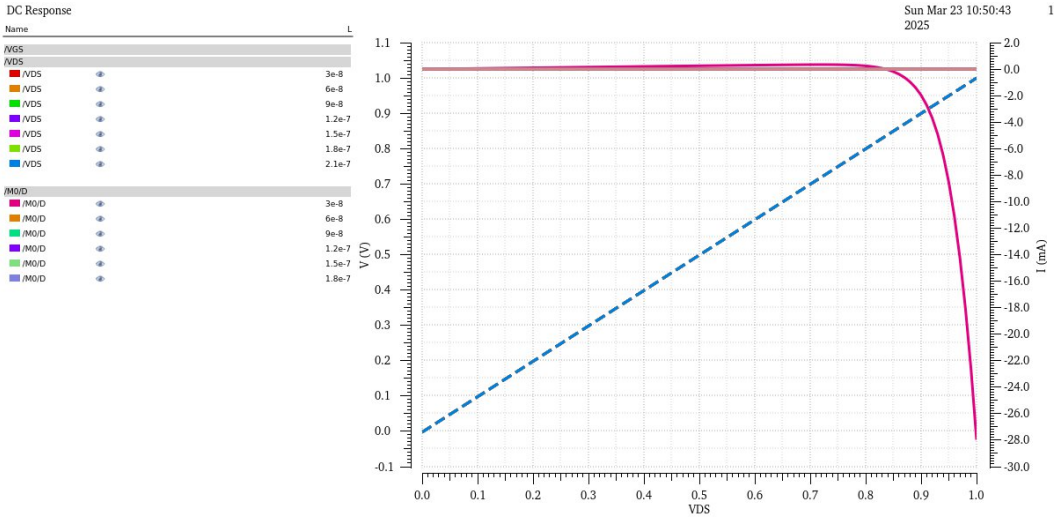

Figure 9: I-V Characteristics of NMOS: W [30,210] nm, step 30 nm.

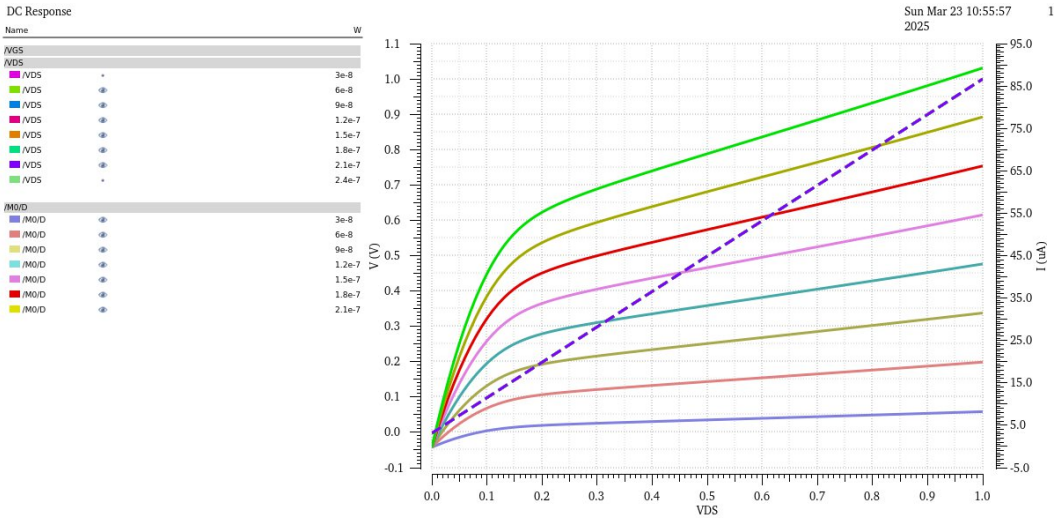

Figure 10: I-V Characteristics of NMOS: W [30,210] nm, L [30,240] nm step 30 nm.

PMOS:

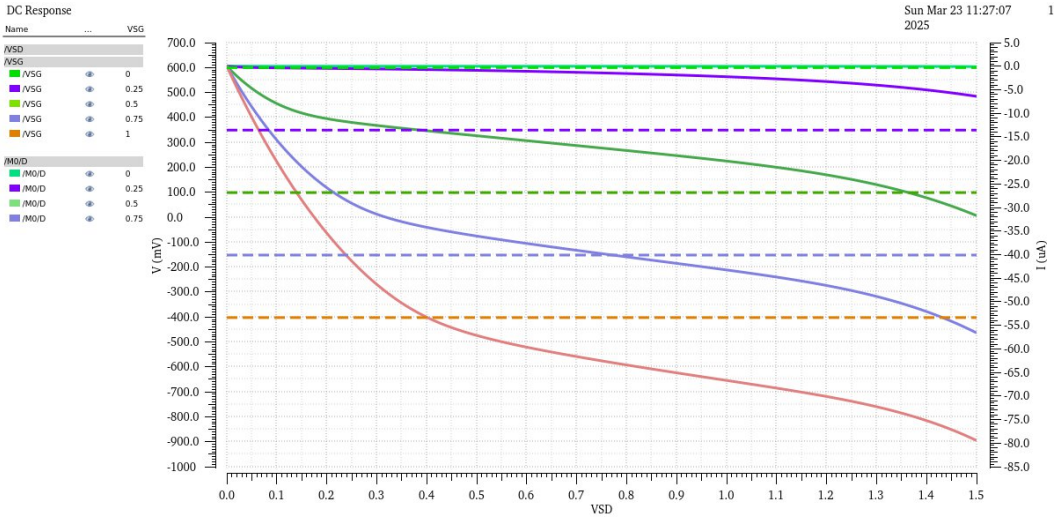

Figure 11: I-V Characteristics of PMOS: W [30,210] nm, step 30 nm.

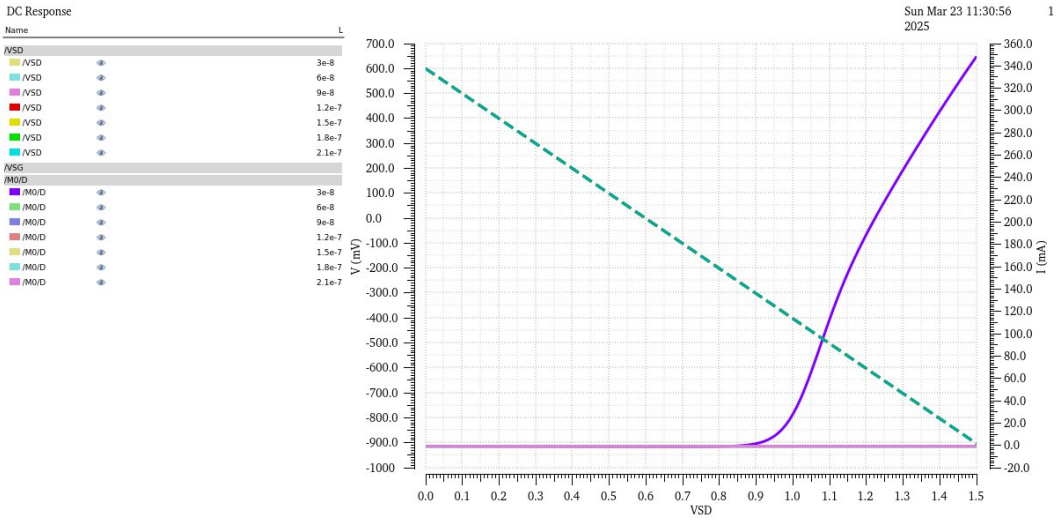

Figure 12: I-V Characteristics of PMOS: W [30,210] nm, L [30,240] nm step 30 nm.

EXPERIMENT 3

Explore second-order effects (Body effect, Channel-length modulation).

NMOS:

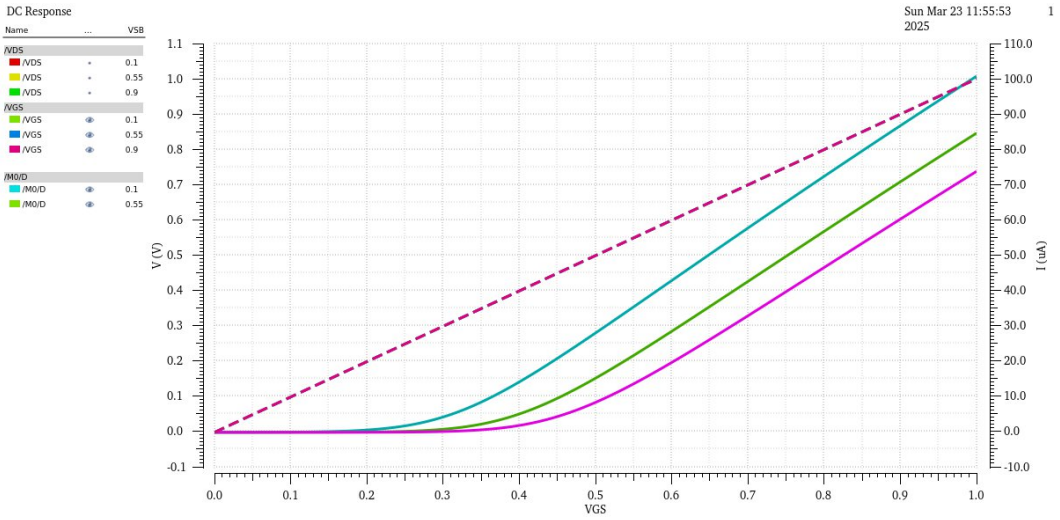

Figure 13: I-V characteristics of NMOS: $V_{DS} = 1\,\text{V}$, $V_{SB} = \{0.1, 0.55, 0.9\}\,\text{V}$, V_{GS} swept from 0V to 1V, step 10mV.

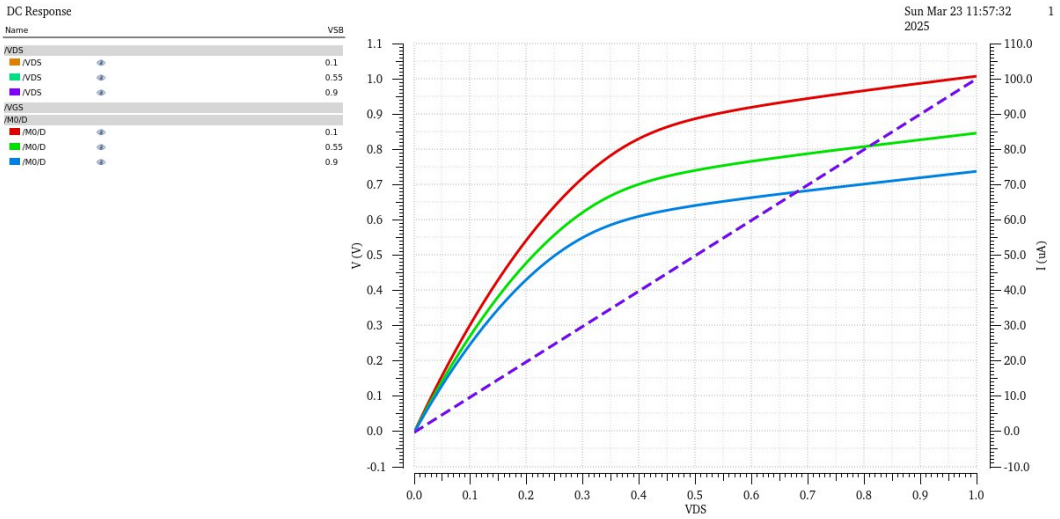

Figure 14: I-V characteristics of NMOS: $V_{DS} = 1\,\text{V}$, $V_{SB} = \{0.1, 0.55, 0.9\}\,\text{V}$, V_{DS} swept from 0V to 1V, step 10mV.

PMOS:

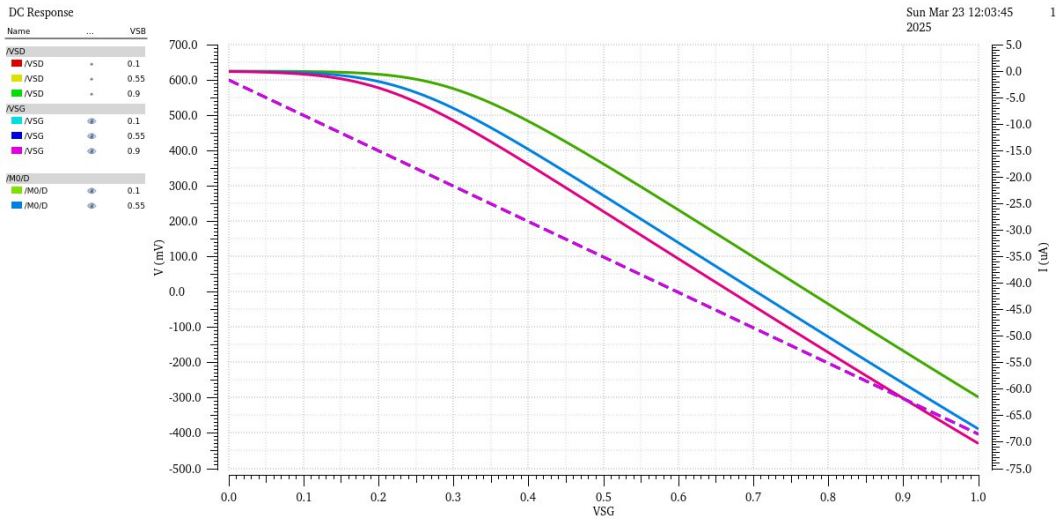

Figure 15: I-V characteristics of PMOS: $V_{DS} = 1\,\text{V}$, $V_{SB} = \{0.1, 0.55, 0.9\}\,\text{V}$, V_{SG} swept from 0V to 1V, step 10mV.

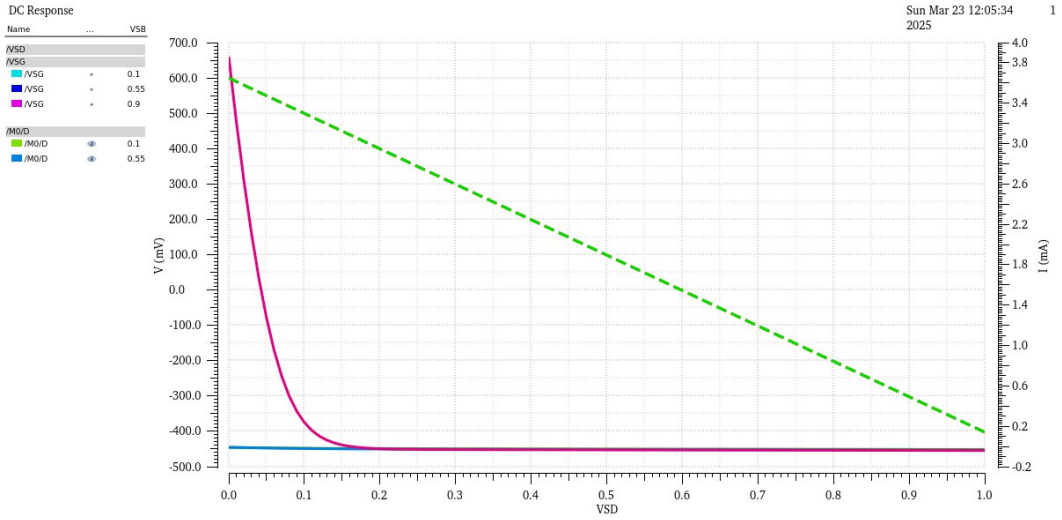

Figure 16: I-V characteristics of PMOS: $V_{DS} = 1\,\text{V}$, $V_{SB} = \{0.1, 0.55, 0.9\}\,\text{V}$, V_{SD} swept from 0V to 1V, step 10mV.

EXPERIMENT 4

Layout design for MOS transistors.

NMOS:

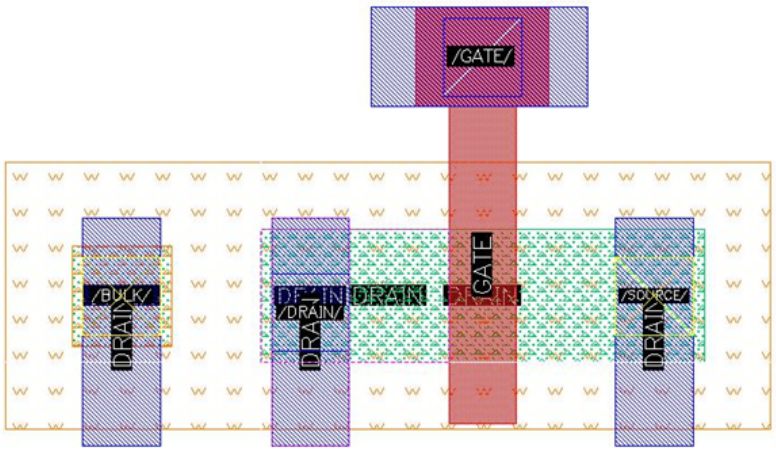

Figure 17: Layout of NMOS 120n/60n

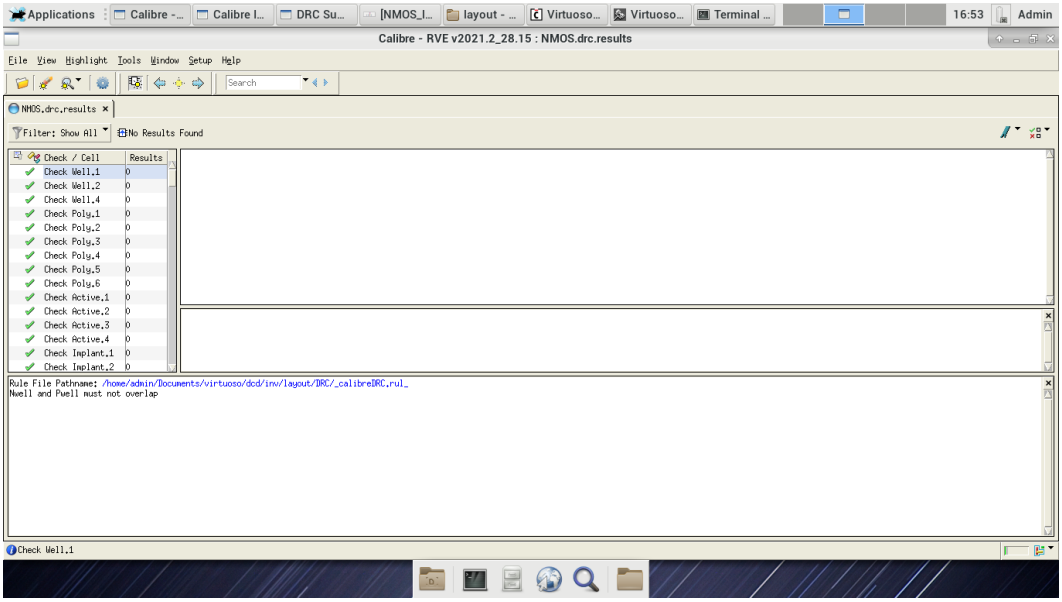

Figure 18: Check DRC of NMOS layout 120n/60n

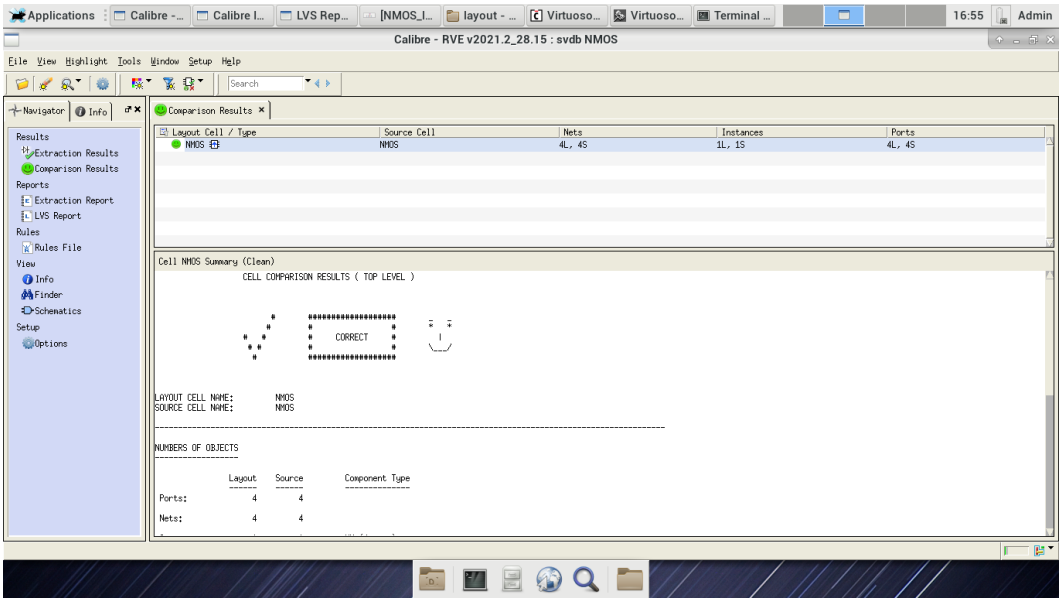

Figure 19: Check LVS of NMOS layout 120n/60n

PMOS:

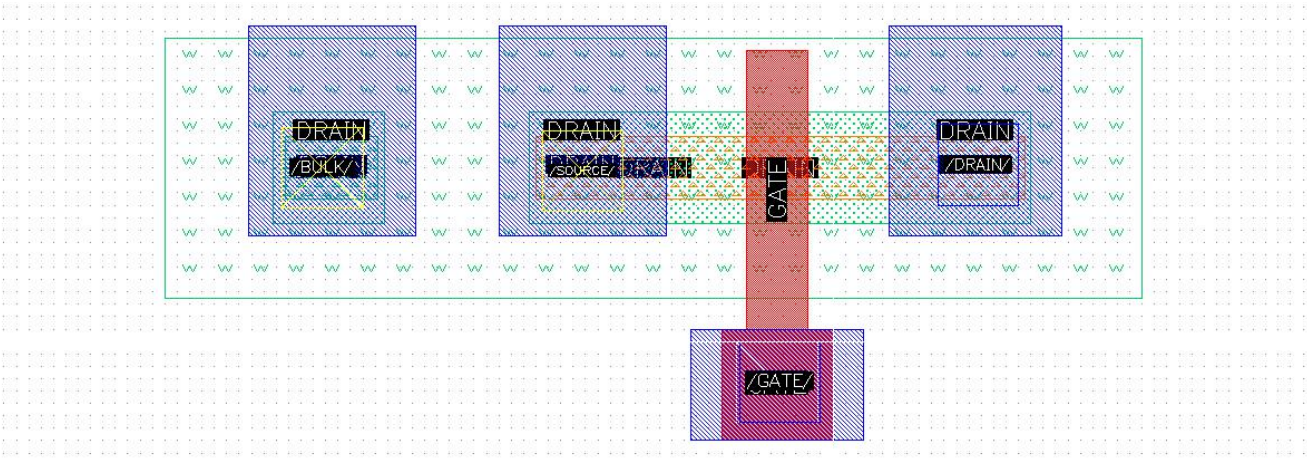

Figure 20: Layout of PMOS 50n/50n

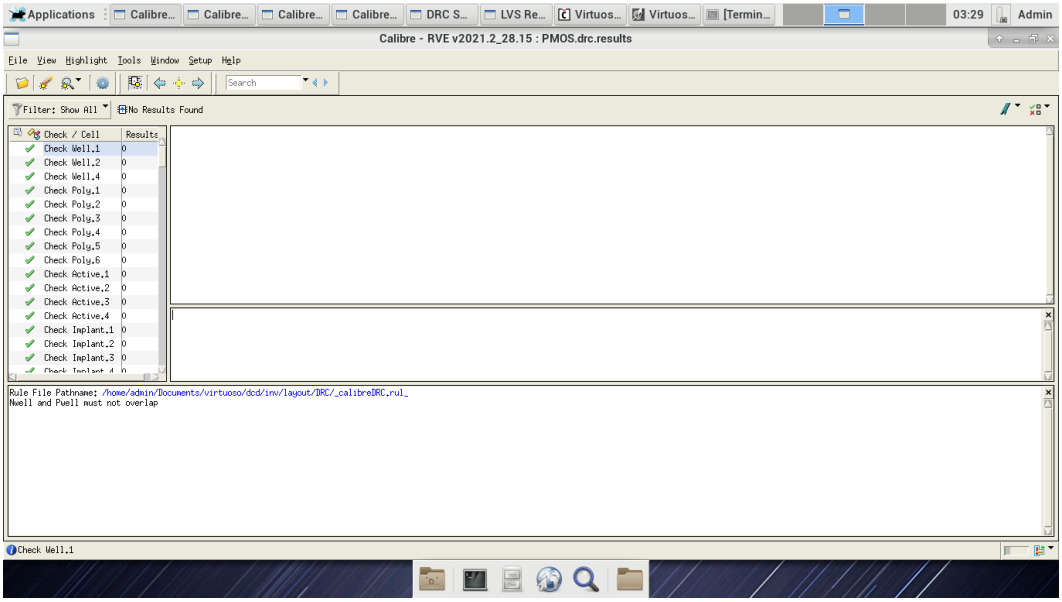

Figure 21: Check DRC of PMOS layout 50n/50n

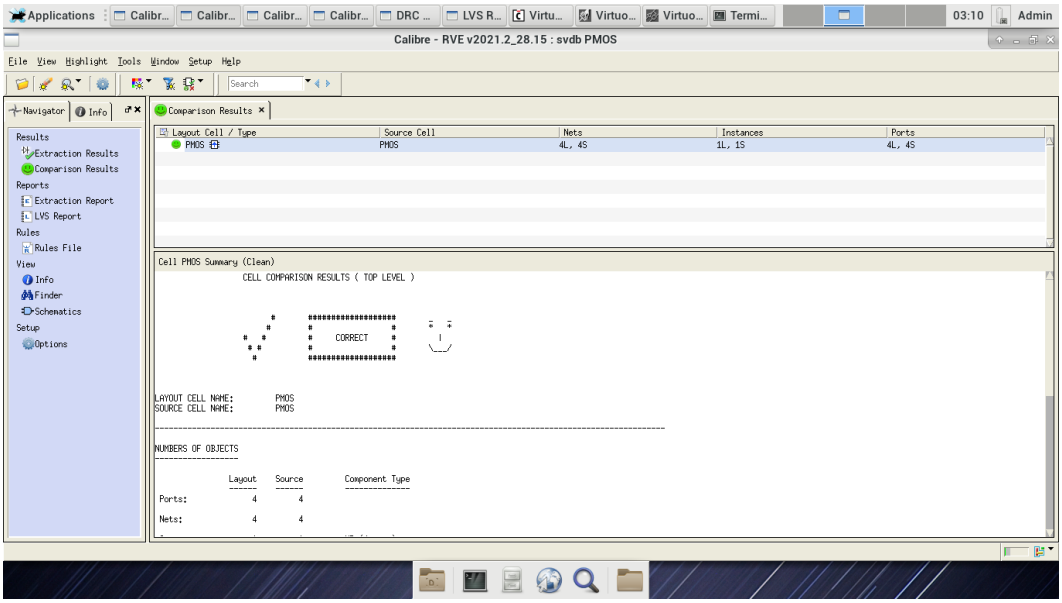

Figure 22: Check LVS of PMOS layout 50n/50n