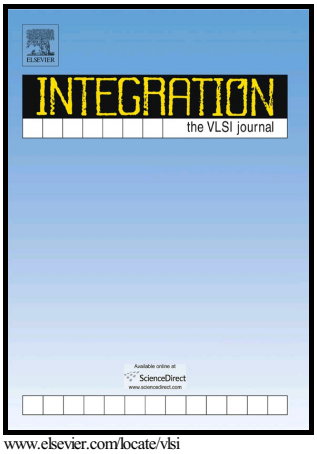

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Abstract

In this paper, we present a double-operating-mode adder which may be employed either in low-power (LP) or high-performance (HP) operating mode. The adder has a hybrid structure based on a carry-lookahead and carry-propagate structures and hence is called CL-CPA. The selection between the two operating modes is performed through a mode selection bit during the operational period. The hybrid structure of the adder provides the feature of selecting the operating mode depending on the application deadlines and system available energy resources. The adder structure is realized by modifying the carry look-ahead tree (CLT) structure and then combining it with a carry propagate adder (CPA). During the LP mode, only the CPA structure is utilized while the CLT is deactivated through the power gating scheme. On the other hand, during the HP mode, the CLT structure is activated and the adder performs with its highest speed and power consumption using both CLT and CPA structures. The efficacy of the proposed hybrid adder is assessed by comparing its speed, power, energy, and area parameters with those of the other conventional adders obtained using HSPICE simulations for a 45-nm CMOS technology in a wide range of supply voltages. The results revel switching from the LP to HP operating mode leads to about 5.4X decrease, 2.5X increase, and 2.1X decrease in the delay, power, and energy of the 64-bit CL-CPA, respectively, averaged over the supply voltages. Also, the proposed hybrid adder provides flexibility on speed and power with an acceptable area usage for applications where both high speed and low power adders are required.

Keywords: Carry lookahead adder, carry propagate adder, hybrid adder, high performance, low power, voltage scaling

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I. INTRODUCTION

Adder units, which are among the basic blocks in arithmetic and logic units (ALUs), are utilized in performing most of the arithmetic operations such as subtraction, multiplication, and division [1]. The delays of these units have a key role in the critical path delays of the processors (especially, in the execution unit) which determine the operating clock frequency. In addition, due to their high usages, their

powers form a significant portion of the power consumption of computational cores of the processors [2]. Thus, designing efficient adders may lead to the performance improvement and power reduction of processors.

One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the subthreshold current which is the main leakage component in OFF devices has an exponential dependence on the supply voltage level through the drain induced barrier lowering effect (DIBL) [3]. The dependence of the power (and performance) on the supply voltage has been the motivation for the design of circuits with the feature of dynamic voltage and frequency scaling (DVFS). In these circuits, to reduce the energy consumption, the system may change the voltage (and frequency) of the circuit based on the workload requirement [4]. For these systems, the circuit should be able to operate under a wide range of supply voltage levels. Also, dynamic voltage scaling from the superthreshold voltage (nominal voltage) down to the near-threshold voltage (supply voltage levels near the threshold voltage of transistors) has been considered as an approach that provides a more desirable tradeoff point between delay (frequency) and power dissipation of the circuits [4] [5].

In addition to the knob of the supply voltage, one may choose between different adder families for optimizing power and speed. Various adder families/structures have been proposed in the past to tradeoff speed, power and area for possible use in ALUs. The prominent structures include ripple carry adder (RCA) and carry select adder (CSLA) [6-8] of the carry propagate adders (CPAs) family, and also, Kogge-Stone adder (KSA) and Brent-Kung adder (BKA) from parallel prefix adders (PPAs) family [1] [2]. The RCA has the simplest structure with the smallest area and power consumption while its critical path delay is worst. The PPAs, which are also called carry look-ahead adders (CLAs), exploit direct parallel prefix structures to generate the carry as fast as possible [9] [10]. There are different types of the parallel prefix algorithms that lead to different PPA structures with different performances [11]. KSA [12] (a dense tree adder) is among the fastest adders with large area and power consumption. On the other hand, BKA [13] (a sparse tree adder) has been proposed to reduce area and power at the cost of slight increase in delay.

Each adder structure has a unique operating frequency and power consumption variations under the DVFS technique. It means that by combining some adder structures (hybrid adder design methodology) and also using the DVFS technique, one may enjoy from more speed/power trade-offs. One straight-forward approach is to use all the candidate structures in one adder block, and each time, based on the delay requirement and energy resource, turn one structure while turning off others by using the power gating technique. In [14], both RCA and CLA structures were employed in an adder unit where the output was chosen using a multiplexer. In this structure, for small input bit lengths (≤ 12), the RCA adder was used while for other cases the CLA was used. Using this structure led to the power consumption reduction compared to the case of using solely the CLA while due to the output multiplexing, the delay of the adder was increased slightly. Additionally, implementation of two independent adders in the structure made the area usage of unit large. There are other work focused on designing hybrid adders [15-22]. In [15-19], hybrid adders based on the combining carry select adders with the carry look-ahead ones were proposed. A general architecture for designing hybrid adders by combining CLAs and CSLAs was proposed in [20]. Also, in this work, different hybrid adder structures based on the proposed architecture were implemented and compared with each other. To provide a higher speed, a hybrid adder by combining CLA and multiplexer-based carry skip adder structures was proposed in [21]. In all of these works, the focus was on improving (optimizing) only one design parameter of the hybrid adder structures (speed or power).

In this paper, we propose a hybrid double-operational-mode adder structure which is able to switch from low-power (LP) operating mode using a carry propagate structure to a high-performance (HP) operating one based on a modified carry look-ahead tree. The use of the DVFS technique may lead to more speed/power adjustment for the adder, and hence, the impacts of the supply voltage scaling on the

different parameters of the proposed hybrid adder structure is investigated. Finally, the effectiveness of utilizing this adder inside the ALU of the processors is studied.

The rest of the paper is organized as follows. The proposed hybrid adder structure as well as the explanations and analyses of its two operating modes are described in Section II. Section III presents the results of comparing the characteristics of the proposed adder structure with those of other adders. Also, the effectiveness of employing the proposed hybrid adder in reducing the power/energy consumption of ALU of the processors is studied in Section III. Finally, Section IV concludes the work.

II. Proposed Hybrid CL-CPA Structure

In this section, first the internal structure of the proposed adder is described and, then, its area and delay are analyzed. Finally, the use of the power gating technique in this hybrid adder is explained.

A. Internal Structure of the CL-CPA

As mentioned before, the high speed carry-look-ahead tree structure is combined with the low power carry-propagate adder in the CL-CPA. These delays and power consumptions of these two adder structures have logarithmic and linear dependency on the adder bit length (N) (see, e.g., [1] and [2]) providing CL-CPA with the operating mode tenability. The switching between the two modes in the proposed hybrid structure shown in Fig. 1 is realized by some architectural and circuit level solutions. During the HP operating mode, the sum output is calculated using both a modified carry-look-ahead block (MCLB) suggested in this work and a carry-propagate adder (chain of RCA block) structure. For the LP operating mode, the add operation is performed only through the carry-propagate adder structure. During the HP operating mode, the process of determining the carry input of each RCA block is performed by MCLB while during the LP operating mode, the carry input of each RCA block is calculated using the previous RCA block in the chain of the RCA blocks. Therefore, the path of the carry input of each RCA block, except of the two first RCA blocks, is different in the two modes. It should be mentioned that during the LP mode, the MCLB is power gated.

Figure 1 shows the N-bit CL-CPA structure with the N-bit A and B inputs, carry input (C_i), N-bit sum output (S), and carry output (C_o). The inputs A and B are divided into m-bit groups which are, except for the last one, the inputs of the m-bit RCA blocks and the carry-lookahead sub-tree (CLST) blocks. The last group (most significant bits) is only used by the last RCA block. The carry input of all the RCA blocks (C_j), except for the two first ones, are fed through a 2:1 multiplexer. One of the

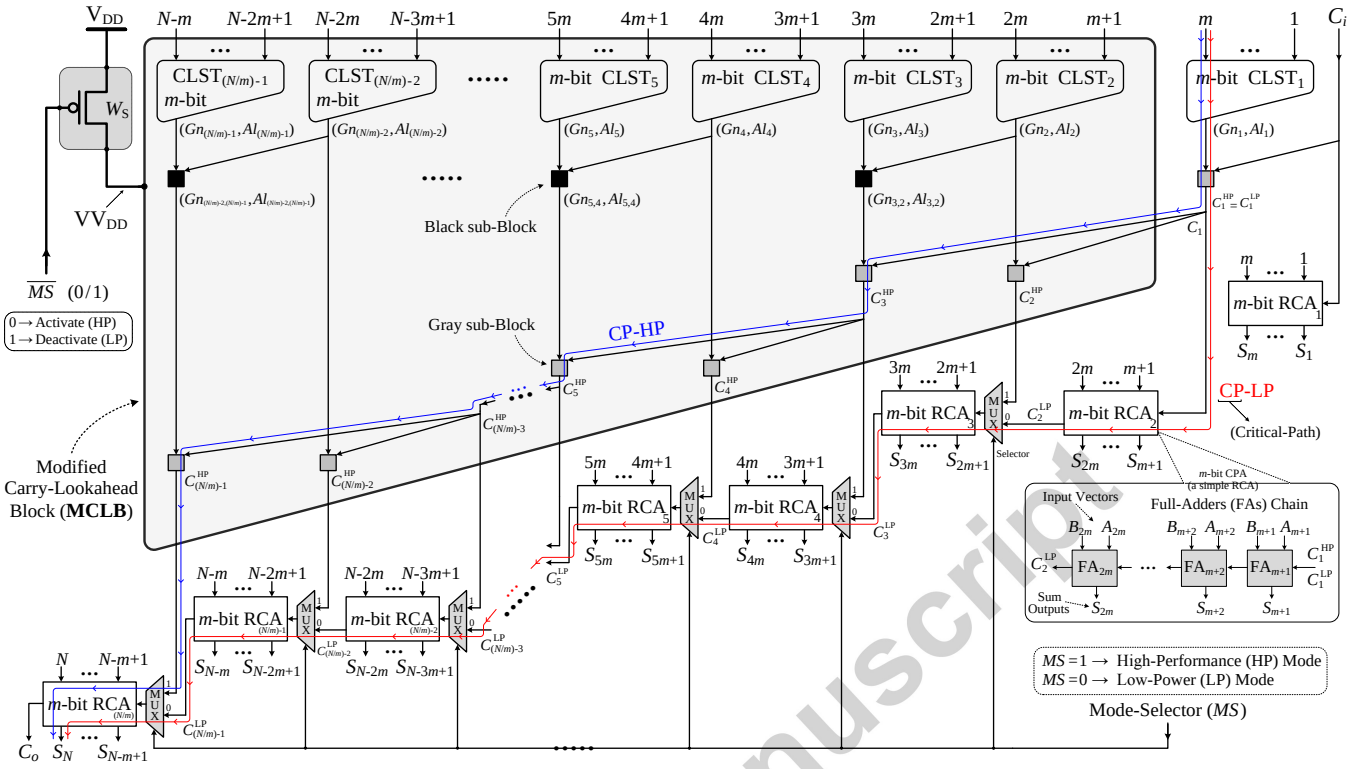

Fig. 1. Structure of the proposed hybrid CL-CPA.

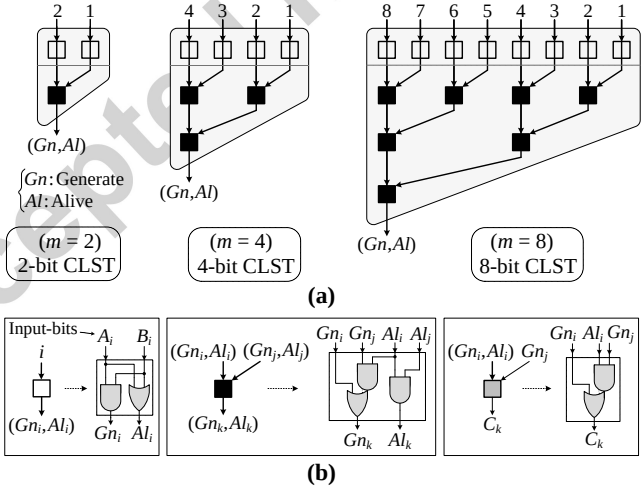

Fig. 2. (a) Internal structure of the carry-lookahead sub-tree (CLST) for m = 2, 4, and 8. (b) Internal structures of the different sub-blocks.

inputs of the multiplexer is from the generated intermediate carry by the MCLB (C_{j-1}^{HP}) while the other input is from the output carry of the previous RCA block (C_{j-1}^{LP}).

The carry input of the first RCA block is connected to the carry input of the CL-CPA (C_i) and the carry input of the second RCA block is generated by the first CLST (C_1). The fast generation of the carry input of the second RCA block (i.e., one RCA block carry skipping) leads to decreasing the propagating delay of the cascaded RCA blocks (CPA structure), and hence, it compensates for the delay overheads of

the 2:1 multiplexers used to select the carry inputs of the RCA blocks. This makes the delay of the proposed N-bit hybrid adder in the LP operating mode not larger than that of the N-bit RCA structure.

The MCLB contains (N/m – 2) parallel m-bit CLST blocks which, in the first step, each of them generates the Alive (Al) and Generate (Gn) signals for the m-bit groups of the inputs. In the next step, the Al and Gn signals of each pair of two adjacent CLST, except the $CLST_1$, are the input signals of the black sub-blocks (see Fig. 1) generating the Al and Gn signals for the 2m-bit groups of the inputs. Finally, each gray sub-block generates the intermediate carry signals (i.e., C_j^{HP}, j = 2, 3, …, (N/m) – 1) by using the corresponding Al and Gn signals and the generated intermediate carry of the previous groups (i.e., C_{j-k}^{HP} ; k = 1 or 2). The internal structures of the CLST block for the m values of 2, 4, and 8 are depicted in Fig. 2(a). Also, the internal structures of the white, gray, and black sub-blocks are shown in Fig. 2(b).

As was mentioned before, in the proposed hybrid adder structure, the MCLB is activated/deactivated using the power gating technique which is performed by a mode selector (MS) control signal. This signal, also, is used to determine the carry input of the RCA blocks. When the MS signal is high (HP operating mode), the MCLB is activated and the carry input of the RCA blocks are generated in parallel and the summation is done as fast as possible by consuming a larger power. On the other hand, when the MS signal is low (LP operating mode), the MCLB block is deactivated, and hence, the carry input signal should be propagated through the cascaded m-bit RCA blocks leading to a higher propagation delay and smaller power consumption.

B. Delay and Area of the Proposed Structure

In Fig. 1, the critical paths in LP and HP operating modes are shown by the red (labeled by CP-LP) and blue (labeled by CP-HP) lines, respectively. The first CLST and its corresponding gray block, and the last RCA and its corresponding carry input multiplexer are shared by both paths while the other parts of the paths are different. Thus, the delays of the critical paths in the LP ($T_{CP\text{-}LP}$) and HP ($T_{CP\text{-}HP}$) operating modes are expressed by

$$T_{CP-LP} = t_{□} + [\log(m) \times t_{■}] + t_{■} + \left[(N - m - 1) \times t_{carry}\right] + t_{sum} + \left[\left(\frac{N}{m} - 2\right) \times t_{mux}\right] \quad (1)$$

$$T_{CP-HP} = t_{□} + [\log(m) \times t_{■}] + \left[\frac{N}{2m} \times t_{■}\right] + \left[(m - 1) \times t_{carry}\right] + t_{sum} + t_{mux} \quad (2)$$

where t_{carry}, t_{sum}, and t_{mux} are the propagation delays of the carry output of a full adder (FA), the sum output of an FA, and the output delay of a 2:1 multiplexer, respectively. Also, $t_{□}$, $t_{■}$, and $t_{■}$ are the propagation delays of the white, black, and gray sub-blocks, respectively. The comparison between (1) and (2) shows that in the proposed adder by switching between the operating modes, the delay is changed significantly. By decreasing the RCA and CLST sizes (i.e., the value of m), the $T_{CP\text{-}HP}$ ($T_{CP\text{-}LP}$) is reduced (increased), while the maximum delay difference between the operating modes is for the case of m = 1. Also, by increasing m, the $T_{CP\text{-}HP}$ ($T_{CP\text{-}LP}$) increases (decreases), while for the case of m = N/2, the delays of two operating modes are the same. Hence, to have a meaningful delay difference between the two modes, the m value should be chosen from [1, (N/2) – 1]. Since the parallel tree structure (i.e., CLST) is more efficient when its size is equal to an integer power of two [8], it is preferred to select m from the set of $\{2^0, 2^1, 2^2, \ldots, 2^k\}$ where k = log (N/2) – 1.

The area usage of the proposed hybrid CL-CPA adder is smaller than those of the parallel prefix adders (e.g., KSA). This may be justified by considering that carry-propagate part of the CL-CPA consists of (N/m) m-bit RCA, (N/m – 2) 2:1 multiplexer, one m-bit CLST, and one gray sub-block. Also, the MCLB is a modified parallel sparse tree that only generates intermediate carries for each m-bit group based on the (N – 2m) bits of the A and B inputs and the carry bit generated for the first m-bit group

($CLST_1$). Hence, its power consumption and area usage are considerably smaller than those of the CLAs (PPAs) which compute all of the intermediate carry signals as well as the sum outputs in their structures. The MCLB is made up of white, gray, and black sub-blocks whose total number ($N_{B,MCLB}$) is indicated from

$$N_{B,MCLB} = [N - 2m] + \left[\left(1 - \frac{1}{2m}\right) \times N + (1 - 2m)\right] + \left[\frac{N}{m} - 2\right]. \quad (3)$$

Here, the first, second, and third brackets determine the number of white, gray, and black sub-blocks, respectively. Hence, the value of m, has a considerable impact on the speed and power consumption of the proposed adder in LP and HP operating modes, and also the overall area usage of the proposed hybrid adder making the selection of a proper (optimal) m value crucial. In this work, we implement the CL-CPA for the different bit length (32- and 64-bit) under the different m values, and select the value which leads to the smallest energy consumption in the both operating modes.

C. Power Gating

The MCLB is activated/deactivated by gating its supply voltage (V_{DD}) using a pMOS switch (see Fig. 1). This causes a virtual V_{DD} (VV_{DD}) appears across the MCLB. The width of the pMOS switch (W_S) impacts the speed, power consumption, and area usage of the proposed hybrid adder. When this switch is ON, W_S effects the speed of the circuit ($T_{CP\text{-}HP}$) where by decreasing m, its effect increases. This is due to the fact that for small m's, the larger portion of $T_{CP\text{-}HP}$ belongs to the delay of MCLB. On the other hand, when the pMOS switch is OFF, the width impacts the leakage power consumption of the adder in the LP mode. This leakage power consumption is negligible compared to the active power consumption of the proposed adder in the LP mode. This provides us with the opportunity of selecting the width based on its effect on the speed of the CL-CPA structure in the HP mode. In this work, the amount of W_S was selected such that no more than of 1% delay increase occurs compared to the case of the direct connection of the MCLB to V_{DD}.

III. Results and Discussion

In this section, we assess the efficacy of the proposed hybrid CL-CPA structure by comparing its delay, power, energy, energy-delay product, and area with those of the RCA, square-root CSLA (SQRT-CSLA), BKA, and KSA. The results were obtained for a wide range of supply voltage levels from the nominal voltage (superthreshold) to the nMOS threshold voltage ($V_{TH,nMOS}$) (near-threshold) [24]. All the adders considered here, were designed and simulated for the sizes of 32- and 64-bits using a 45-nm CMOS technology [25]. The simulations were performed using HSPICE [26] in the temperature of 25 °C. The nominal voltage of the technology was 1.1V and the threshold voltages of the nMOS and pMOS transistors were 0.677V and -0.622V, respectively (typical threshold voltage). It should be noted that, to extract the power consumption of the adders, 10,000 uniform random stimuli were injected to them. Also, for each adder structure at each supply voltage level, the injection rate of the stimuli was chosen based on the maximum operating frequency of the adder structure.

In the following subsections, first, the optimal blocks size (m) and pMOS switch width (W_S) of the proposed CL-CPA structure for the 32- and 64-bit length are determined. Next, the efficiency of the proposed hybrid adder structure in both modes is investigated. It should be noted that, in this section, the width of the pMOS switch is determined based on the ratio of W_S to the total widths of the pMOS transistors of the MCLB (W_T) [27]. Finally, this adder is used inside the ALU of the processor model and the impact of the switching between the two operating modes on the power/energy consumption of the ALU is studied.

A. Determining the Internal Structure

Based on the descriptions given in Subsection II.C, the proposed 32- and 64-bit CL-CPAs were implemented based on different amounts of m (using the sets of $\{2^0, 2^1, 2^2, 2^3\}$ and $\{2^0, 2^1, 2^2, 2^3, 2^4\}$ in the 32-bit and 64-bit cases, respectively). Noted that for each bit length and m value, the optimal W_S was considered. Also, to reduce the total capacitance of the virtual supply voltage (VV_{DD}), the body terminal of the pMOS switch was connected to the V_{DD} [23] [27] [28].

Fig. 3(a) shows the delay increase of the 32-bit CL-CPA compared to the case where the MCLB is directly connected to the V_{DD} (VV_{DD} = V_{DD}) in the HP mode ($T_{CP\text{-}HP}$) versus W_S. As was expected, the delay increase reduces as the width enlarges. For very large widths, the delay degradation due to using the sleep transistor is negligible. Also, the delay improvement rate versus W_S decreases as the width increases. As mentioned before, for each m value, the value of W_S which

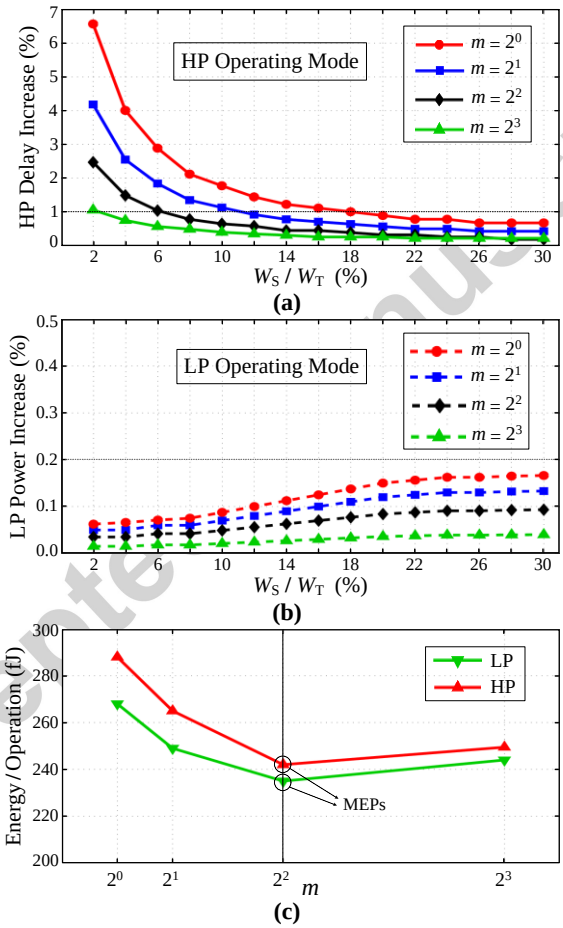

Fig. 3. (a) HP delay increase percentage, and (b) LP leakage power increase percentage versus the pMOS switch width (W_S). (c) Energy per operation of the 32-bit CL-CPA at the nominal supply voltage in the LP and HP operating modes for different m values.

led to the delay overhead just below 1% (using the results of Fig. 3(a)) was selected for the design. For the case of the 32-bit CL-CPA, the values of W_S were about 4%, 8%, 12%, and 20% of the W_T for the m values of 2^0, 2^1, 2^2, and 2^3, respectively. Also as the results show, by increasing m, the delay overhead decreases. It may be justified by noting that increasing m makes the lower portion of the $T_{CP\text{-}HP}$ depend on the delay of the MCLB (see (2)).

On the other hand, the simulation results reveal that the maximum (leakage) power consumption of the MCLB in the CL-CPA structures in the LP operating mode for different amounts of m and W_S were

below 0.2% which is negligible [see Fig. 3(b)]. Finally, Fig. 3(c) shows the energy per operation of the proposed 32-bit hybrid adder at the nominal voltage in the two operating modes for different amounts of m. In both LP and HP operating modes, the minimum energy points (MEPs) belong to the case of $m = 2^2$. Similarly, for the case of the 64-bit CL-CPA, our results indicated that the optimum amount of m was 2^3 with $W_S/W_T = 6\%$.

B. Discussion on Design Parameters

Switching from the LP (HP) to HP (LP) operating mode in the proposed CL-CPA structure has a delay overhead. The switching delays of the 32- and 64-bit CL-CPA in the superthreshold voltage (STV) and near-threshold voltage (NTV) are reported in Table I. These delays are extracted based on the time which needs to fully turn on (LP→HP) or turn off (HP→LP) the MCLB. As the results indicate the switching from the LP mode to the HP mode is very fast while the switching from HP to LP is slow. It should be noted that since the MCLB is not employed in the LP operating mode, the switching delay from HP to LP does not increase the delay of the first add operation in the LP mode. This makes the switching delay overhead of the proposed hybrid CL-CPA structure negligible.

The propagation delay and the power consumption of the 32- and 64-bit proposed hybrid adder and some other structures for a wide range of supply voltage are illustrated in Fig. 4. It is evident from the figure that the RCA (KSA) has the highest (lowest) delay and lowest (highest) power consumption due to its serial (parallel) structure. The smaller power consumption of BKA is associated to its sparse parallel tree structure with a propagation delay larger than that of the KSA. The delay of the SQRT-CSLA is smaller (larger) than that of the RCA (BKA) at all supply voltage levels while its power consumption is larger than that of the BKA owing to the logic duplication in its structure. In the case of the proposed hybrid CL-CPA, in the LP operating mode, the delays and power consumptions of the 32- and 64-bit CL-CPA structures are almost similar to those of the RCA at all supply voltage

TABLE I. OPERATING MODE SWITCHING DELAY OVERHEAD OF THE CL-CPA STRUCTURE

CL-CPA Structure	**Switching Delay (ns)**			
	LP → HP		HP → LP	
	STV	NTV	STV	NTV
32-bit	0.05	0.42	3.25	26.30
64-bit	0.07	0.57	4.32	34.50

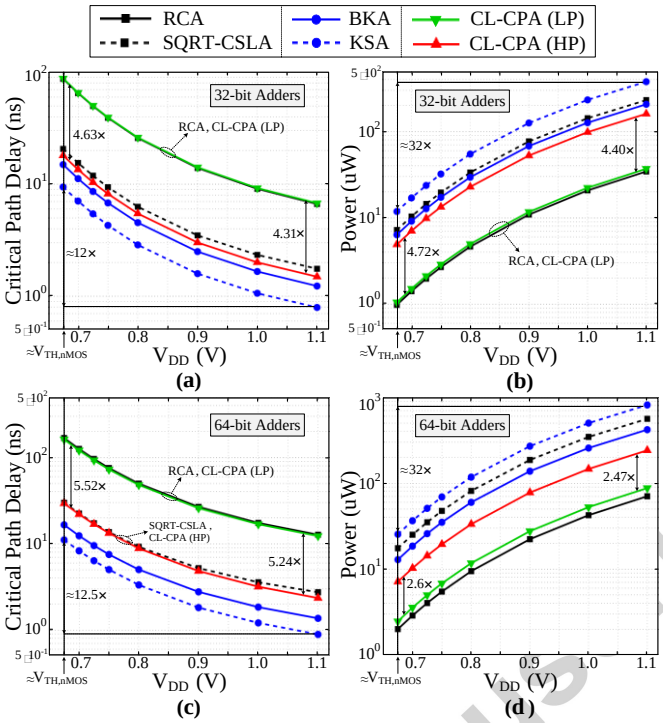

Fig. 4. Critical path delay and power consumption of the 32- and 64-bit adder structures versus the supply voltage.

levels while in the HP operating mode, the delay of the 32-bit CL-CPA is a bit smaller (larger) than that of the SQRT-CSLA (BKA). However, in the 64-bit case, the delay of the CL-CPA in the HP operating mode is about the same as (larger) that of the SQRT-CLSA (BKA). Also, the power consumptions of the 32- and 64-bit proposed hybrid adder structure, are smaller than those of the SQRT-CSLA, BKA and KSA. In the case of the 32-bit (64-bit) CL-CPA structure, the switching between LP to HP operating mode leads to 4.31× to 4.63× (5.24× to 5.52×) delay reduction. Also, by switching from HP to LP operating mode, the power consumption of the 32-bit (64-bit) CL-CPA is reduced 4.4× to 4.72× (2.47× to 2.6×). It should be noted that the differences between the amounts of the delay and power variations under the switching mode originate from the fact that the CPAs (CLAs) has a linear (logarithmic) dependency to the N (adder bit length) (see, e.g., [1] and [2]).

Fig. 5 shows the power-delay product (PDP) and the energy-delay product (EDP) of the 32- and 64-bit adders versus the supply voltage. The energy consumption of the 32-bit CL-CPA structure in both operating modes are almost similar to each other, and similar to that of the RCA which has the smallest energy among the other adder structures. By increasing the bit length from 32 to 64, the delay of the RCA increases two times (due to the linear dependency to N), while the delay of the KSA and BKA increase by about 1.2 times (due to the logarithmic dependency to N).

Similar to the BKA and KSA which have smaller energy consumption compared to that of the RCA when the input bit length is 64, the CL-CPA consumes less energy in the HP mode for this input bit width where the BKA also has very low energy consumption [Fig. 5(c)]. It should be noted that in both

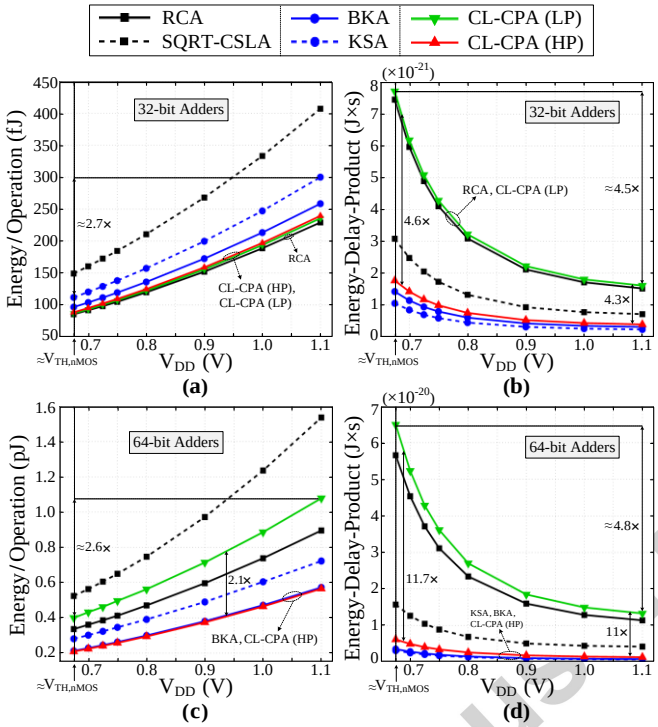

Fig. 5. Energy and energy-delay product (EDP) of the 32- and 64-bit adder structures versus the supply voltage.

TABLE II. AREA USAGES AND NUMBER OF TRANSISTORS OF THE ADDERS

Adder Structure	32-bit		64-bit	
	Area (μm^2)	# of Transistors	Area (μm^2)	# of Transistors
RCA	151.3	896	303.2	1792
SQRT-CSLA	357.4	2096	726.8	4263
BKA	286.1	1406	584.3	2862
KSA	403.2	2010	931.0	4628
CL-CPA	282.7	1512	541.5	2910

32- and 64-bit BKA, although the delay is larger than that of the KSA, its power consumption is much smaller than that of the KSA leading to a smaller energy usage at all supply voltages. Also, based on the results in Fig. 5(b) and (d), the EDPs of the 32- and 64-bit CL-CPA structures in the LP (HP) operating mode are almost the same as the EDP of the RCA (KAS and BKA).

Next, in Table II the area usages and the number of transistors for each adder structure are reported. The RCA (KSA) has the smallest area while the KSA has the highest area. The next largest adder is SQRT-CSLA. The area usage of the proposed CL-CPA structure is almost the same as that of the BKA while their areas are considerably smaller than the KSA and SQRT-CSLA. Also, as the results show, the area of the proposed hybrid adder is about 50% smaller than the case where the RCA and KSA are used separately in one adder unit.

C. Exploting CL-CPA by Processor

In this section, the effectiveness of the proposed adder in reducing the power consumption of the ALU is evaluated. The evaluation was performed by using Wattch simulator [29] when the information of the power consumption of the proposed adder in both operating modes was added. Note that since the smallest predefined technology on Wattch simulator was 90nm, the tool was modified to support simulation in the 45nm technology (V_{DD} = 1.1). Eight benchmarks from Mibench [30] package were run on this simulator under two scenarios. In the first scenario, the 32-bit CL-CPA was utilized in the LP mode while in the second scenario, the CL-CPA in the HP mode was used. Due to the critical delay difference in the two modes, in the first and second scenarios, the frequency of the processor was defined as 143 MHz and 564 MHz, respectively. These frequencies were determined based on the delays of the adder at the nominal supply voltage (see Fig. 4) and the forwarding path in the execution unit.

The percentages of the power consumption of the ALU due to the adder usage in each studied scenarios are depicted in Fig. 6(a). When the proposed adder is used in the LP mode, the percentage of the ALU power consumption due to the adder decrease considerably where the minimum (maximum) percentage, which is 15% (21%), belongs to the susan (sha) benchmark. In this mode, the average percentage is 18% while in the HP mode, the average is 52%. In the HP mode, the maximum (minimum) percentage belongs to the adpcm (susan) benchmark. Obviously, the lower power in the LP mode comes at the cost of increased latency. Finally, Fig. 6(b) shows the percentages of the energy consumption of the ALU due to the adder for different benchmarks. Similar to the case of the power consumption, for all benchmarks, the CL-CPA in the LP mode leads to a lower percentage of the energy consumption. The results indicate that by switching from the HP mode to the LP mode, on average, the percentage decreases from 10.3% to 3.6%.

The latency of the execution (runtime) of the benchmarks for the processor model used when the CL-CPA has been employed in the HP and LP modes are plotted in Fig. 7. As mentioned before, the processor (and ALU) runs the benchmarks with the frequencies of 564 MHz and 143 MHz, respectively. Since the frequencies were determined based on the delays of the adders, the ratios of the execution time increase, when switching from the HP to LP mode, is equal to the ratio of the frequencies for all the benchmarks.

IV. Conclusion

In this paper, a double-operating-mode hybrid carry-lookahead/carry-propagate adder structure called CL-CPA was proposed. The CL-CPA might operate in either low-power (LP) or high-performance (HP) operating mode where the desired operating mode was chosen by a selecting bit during the operational period. The proposed hybrid adder was realized by combining a modified carry lookahead tree structure with a simple carry propagate adder structure. During the low-power operating mode, the CL-CPA only employed the carry-propagate structure while the carry-lookahead tree structure was deactivated through the power gating scheme. On the other hand, during the high-performance operating mode, the carry-lookahead tree structure was activated and the

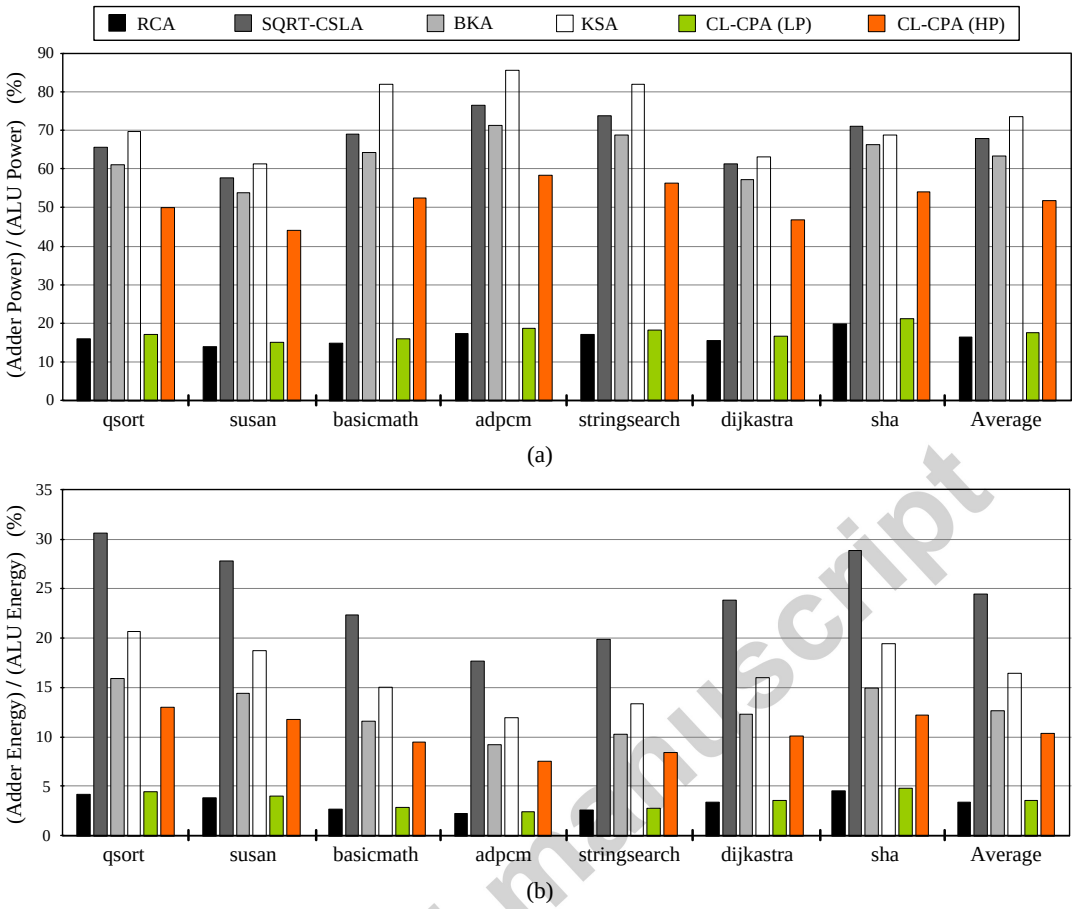

Fig. 6. The percentages of (a) the adder power consumption to the ALU total power consumption, and (b) the adder energy consumption to the ALU total energy consumption for different adder structures and benchmarks.

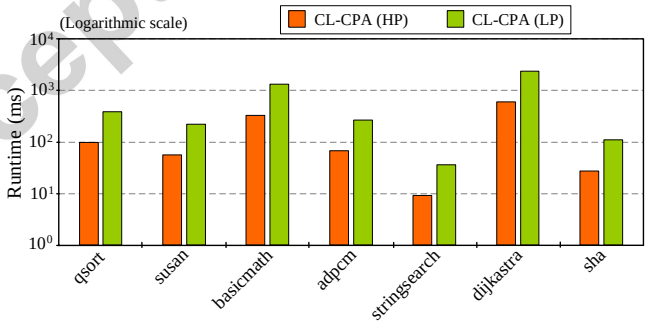

Fig. 7. Runtime of the considered benchmarks when the LP and HP modes of the CL-CPA are utilized.

hybrid adder operated with the highest speed and power consumption. The efficacy of the proposed CL-CPA adder was compared to those of the other conventional adder structures. The results revealed that the CL-CPA operates similar to the RCA during the low-power operating mode, while in the high-performance operating mode, its speed was similar to the parallel adder structures with a smaller power consumption. Finally, the effectiveness of the proposed adder in reducing the power consumption of the ALU for some benchmarks was studied. The results of this showed that when the adder was used in the

LP mode, the percentages of the adder power and energy in the total power and energy of the ALU decreased considerably at the cost of increases latency.

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Highilights

- Presenting a hybrid double-operating-mode adder structure which is able to switch from low-power (LP) operating mode to a high-performance (HP) operating one.
- Analyzing the design parameters of the proposed hybrid adder for both the low-power and high-performance operating modes.
- Investigation the impact of supply voltage scaling on the different parameters of the proposed hybrid adder.
- Studying the effectiveness of utilizing the proposed hybrid adder inside the ALU of the processors.