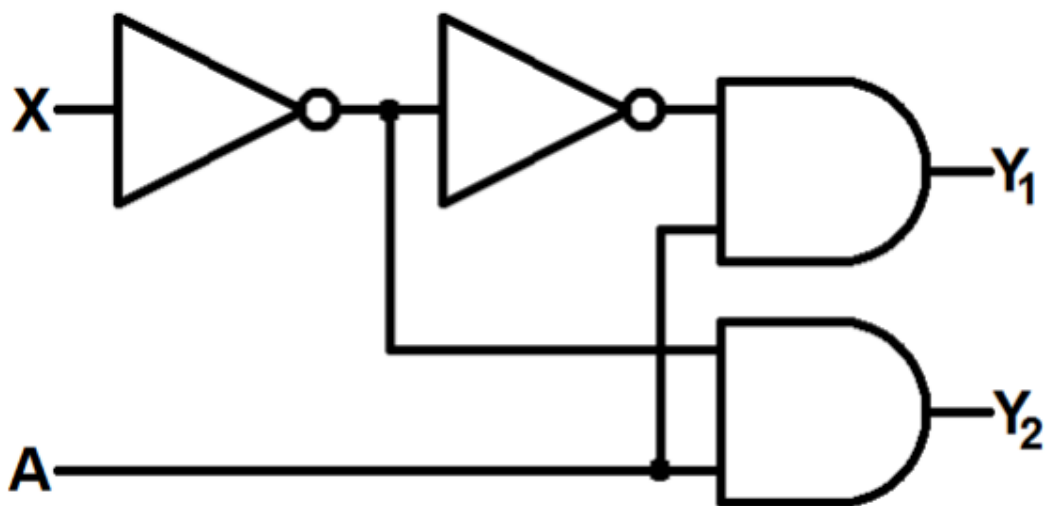# Digital Electronic Circuits

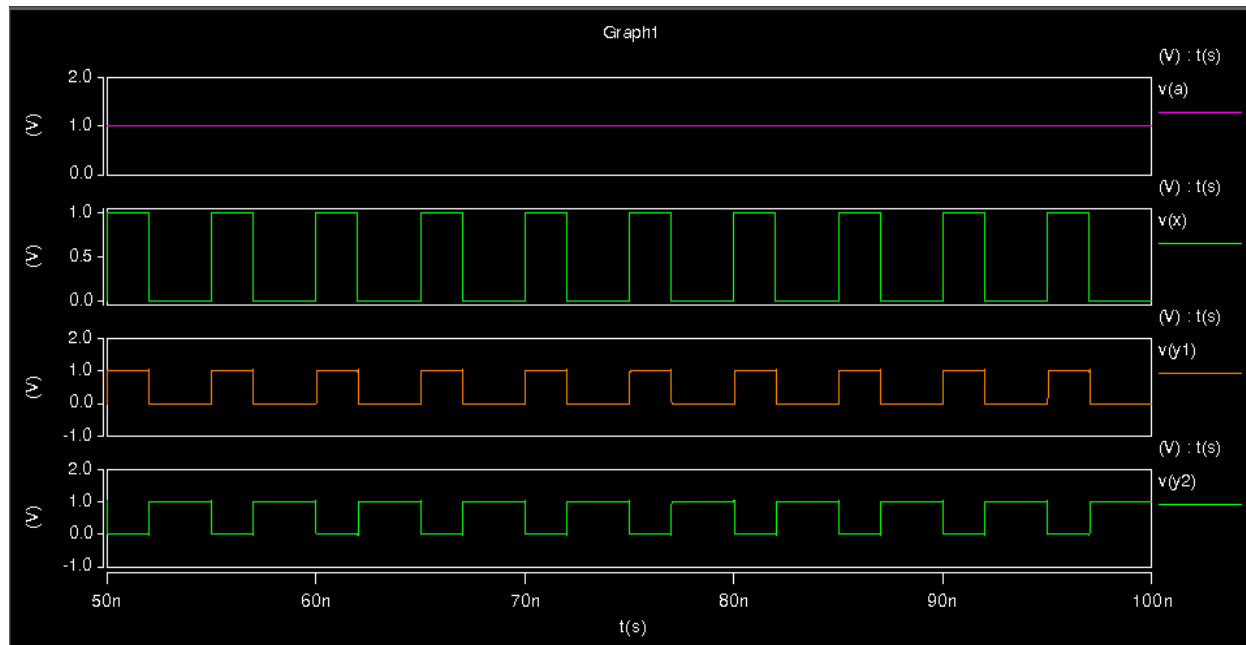## CA III

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در این تمرین کامپیوتری تلاش شده تا مدار مربوط به یک 1 to 2 decoder را در سطح ترانزیستور به سه روش مقایسه کنیم و نتایج را مقایسه کنیم.
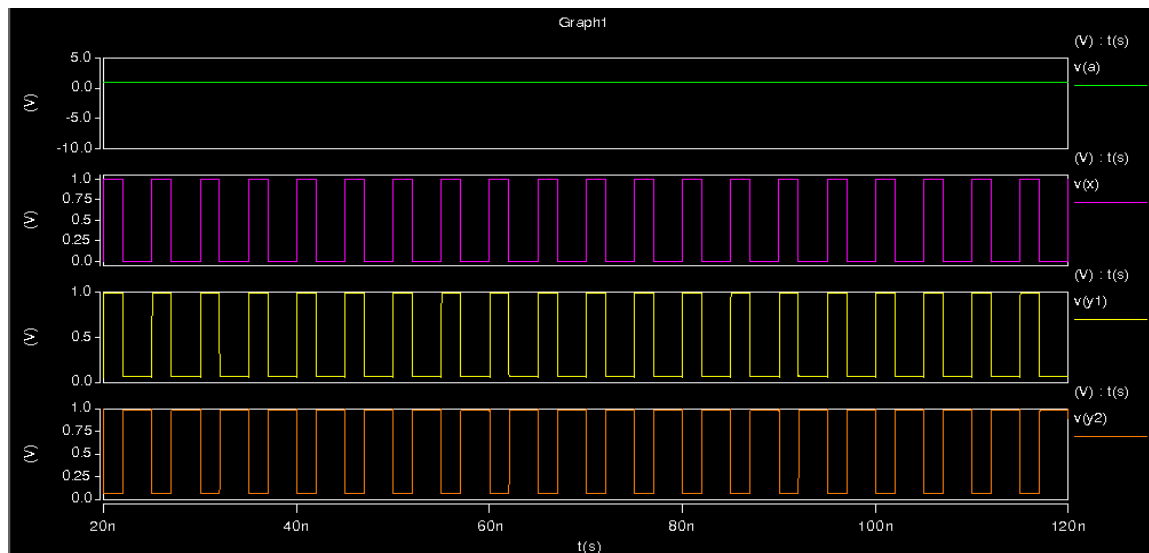
- **Static CMOS**

خروجی به ازای وروی های مختلف X

Avgpower = 1.349e-07

Trig	Trag	Tphl	Tplh	Another	Reason
X	Y1	2.017e-09	3.020e-09	A = 1	it is ok.
X	Y1	failed	failed	A = 0	Y1 does not change.
A	Y1	2.007e-09	3.010e-09	X = 1	it is ok.
A	Y1	failed	failed	X = 0	Y1 does not change.
X	Y2	1.345e-11	1.517e-11	A = 1	it is ok.
X	Y2	failed	failed	A = 0	Y2 does not change.
A	Y2	failed	failed	X = 1	Y2 does not change.
A	Y2	2.007e-09	3.010e-09	X = 0	it is ok.

- **Pseudo – NMOS**

خروجی به ازای وروی های مختلف X

Avgpower = 1.179e-04

Trig	Trag	Tphl	Tplh	another	reason
X	Y1	2.014e-09	3.016e-09	A = 1	it is ok.
X	Y1	failed	failed	A = 0	Y1 does not change.
A	Y1	2.006e-09	3.008e-09	X = 1	it is ok.
A	Y1	failed	failed	X = 0	Y1 does not change.
X	Y2	5.552e-12	2.052e-11	A = 1	it is ok.
X	Y2	failed	failed	A = 0	Y2 does not change.
A	Y2	failed	failed	X = 1	Y2 does not change.
A	Y2	2.006e-09	3.008e-09	X = 0	it is ok.

با مقایسه با جدول Cmos مشاهده میشود که برای تمامی حالت های ممکن تاخیر بهتر میشود بجز
تغییرات x به Y2 با A = 1

- Dynamic Logic
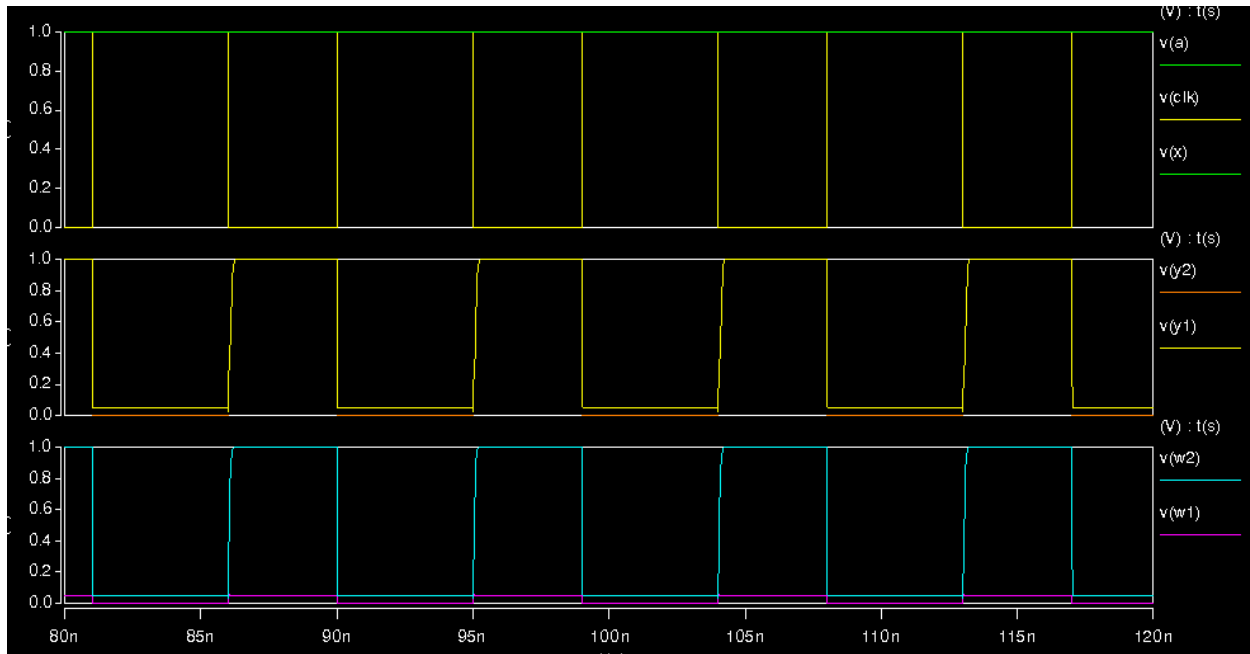
Avgpower = 5.542e-05

Trig	Trag	Tphl	Tplh	another	reason
X	Y1	4.007e-09	2.939e-09	A = 1	it is ok.
X	Y1	failed	failed	A = 0	Y1 does not change.
A	Y1	4.007e-09	2.937e-09	X = 1	it is ok.
A	Y1	failed	failed	X = 0	Y1 does not change.
X	Y2	4.007e-09	5.102e-09	A = 1	it is ok.
X	Y2	failed	failed	A = 0	Y2 does not change.
A	Y2	failed	failed	X = 1	Y2 does not change.
A	Y2	4.007e-09	2.844e-09	X = 0	it is ok.

با مقایسه با جدول Cmos و pseudo مشاهده میشود که Tplh کمتر شده به جز تغییرات x
به Y2 با A = 1 . ولی Tphl بیشتر شده است.