A Broadband Low-Cost Direct-Conversion Receiver Front-End in 90 nm CMOS

Jing-Hong Conan Zhan, *Member, IEEE*, Brent R. Carlton, *Member, IEEE*, and Stewart S. Taylor, *Fellow, IEEE*

***Abstract*—Transistors in aggressively scaled CMOS technologies have f_T greater than 150 GHz, which exceeds requirements for most existing commercial applications below 10 GHz. Excess transistor performance can be traded-off for cost by designing out inductors. This paper presents a prototype which exploits the speed of transistors to design highly integrated broadband receiver front-ends. The inductor-less prototype operates from 2 to 5.8 GHz and dissipates 85 mW at 5 GHz while occupying 0.2 mm^2 active area. It provides 44 dB of gain, 3.4 dB double side band noise figure, −21 dBm in-band IIP3 in the highest gain mode and −15 dB input matching.**

***Index Terms*—Broadband, current mode passive mixer, direct-conversion, inductor-less, low-cost, receiver, resistive feedback.**

I. Introduction

THE strong demand for high performance radios creates many engineering challenges. Future platforms are likely to support the following features: 2T3R WLAN a/b/g/n + WiMax, 2T2R UWB and bluetooth for connectivity; GPS for navigation; FM/XM radio and DVB-T/H for wireless connectivity and entertainment. One challenge is to mitigate interference between these devices to maintain signal integrity. This is especially important when more than one device operates simultaneously in the same frequency band. Careful planning through proper isolation in the frequency domain, spatial domain and time domain reduces the severity of this problem. Another challenge is to economically integrate these radios cost-effectively: more than ten radios co-exist in the aforementioned platform. Sharing resources, reducing device size, and increasing the level of integration are important for cost reduction. Architecture and system improvement is one way to reduce cost: for example, using broadband/multi-standard or reconfigurable components so that the number of front-ends could be reduced; implementing the radios as silicon-on-chip (SoC) or silicon-on-package (SoP) to reduce external component cost; sharing an ADC to provide an adequate sampling rate and effective number of bits (ENoB); reusing the OFDM engine in WLAN / WiMax / DVB-T/H applications. Alternatively, the cost can be brought down by reducing the area of each sub-block. One way to lower cost is to design-out high-Q inductors whenever possible to allow small, multiple transceivers to be integrated at a marginal additional cost.

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J.-H. C. Zhan was with the Communication Circuit Lab, Intel, Hillsboro, OR 95616 USA. He is now with the RF Division, MediaTek, HsinChu, Taiwan, R.O.C. (e-mail: jhc_zhan@ieee.org).

B. R. Carlton and S. S. Taylor are with the Communication Circuit Lab, Intel, Hillsboro, OR 95616 USA.

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This paper presents a broadband receiver front-end which exploits the advantages of aggressively scaled CMOS technology, and serves as a demonstration vehicle for an inductor-less design approach. Circuit techniques used in the prototype, particularly those focusing on improving receiver linearity, mitigating flicker noise in CMOS, and shrinking the die size are addressed in Section II. The measurement results are presented in Section III, followed by conclusions in Section IV.

II. Circuit Descriptions

A. Receiver Architecture

This prototype employs a direct-conversion architecture for its lower cost and power when compared to a super-heterodyne architecture. Although more prone to mixer switching quad flicker noise, it had been demonstrated that by using current-mode passive mixers [1]–[3], this problem can be effectively mitigated. A small current due to self-mixing still exists and produces flicker noise, but its magnitude is usually small, and the receiver flicker noise is typically dominated by the baseband amplifier instead of the mixer switching quad. Proper sizing and biasing of the baseband transistors improves the overall receiver performance when a passive mixer is employed. To improve mixer linearity and maximize dynamic range, a transimpedance amplifier with a real pole following the mixer is utilized. The transimpedance amplifier input impedance is relatively low and reduces the voltage swing at the output of the mixer during frequency down conversion. The low voltage swing and impedance presented to the mixer reduces the non-linearity produced by MOSFET channel resistance. Additionally, when properly designed, the output of the transimpedance amplifier can swing from rail to rail. Both mechanisms improve the linearity of the mixer. DC offset from self-mixing could be reduced by proper component sizing and through calibration.

Another critical component necessary for a low-cost receiver is an LNA with a small footprint, which covers the frequency range of interest, and provides gain adjustment to accommodate input signal level variations. Several LNA topologies provide broad bandwidth. Common-gate LNAs typically have broader bandwidth and better linearity than a corresponding tuned common-source LNA. But they also tend to have lower gain and worse noise performance: the noise figure is usually greater than 3 dB. Therefore, they are typically limited to applications where linearity is more important than sensitivity. Positive feedback may allow for improved noise figure [4] but requires careful stability analysis. An LC ladder matching network, either integrated on-chip or off-chip, can also provide broadband matching [1]. In these implementations, one or more inductors

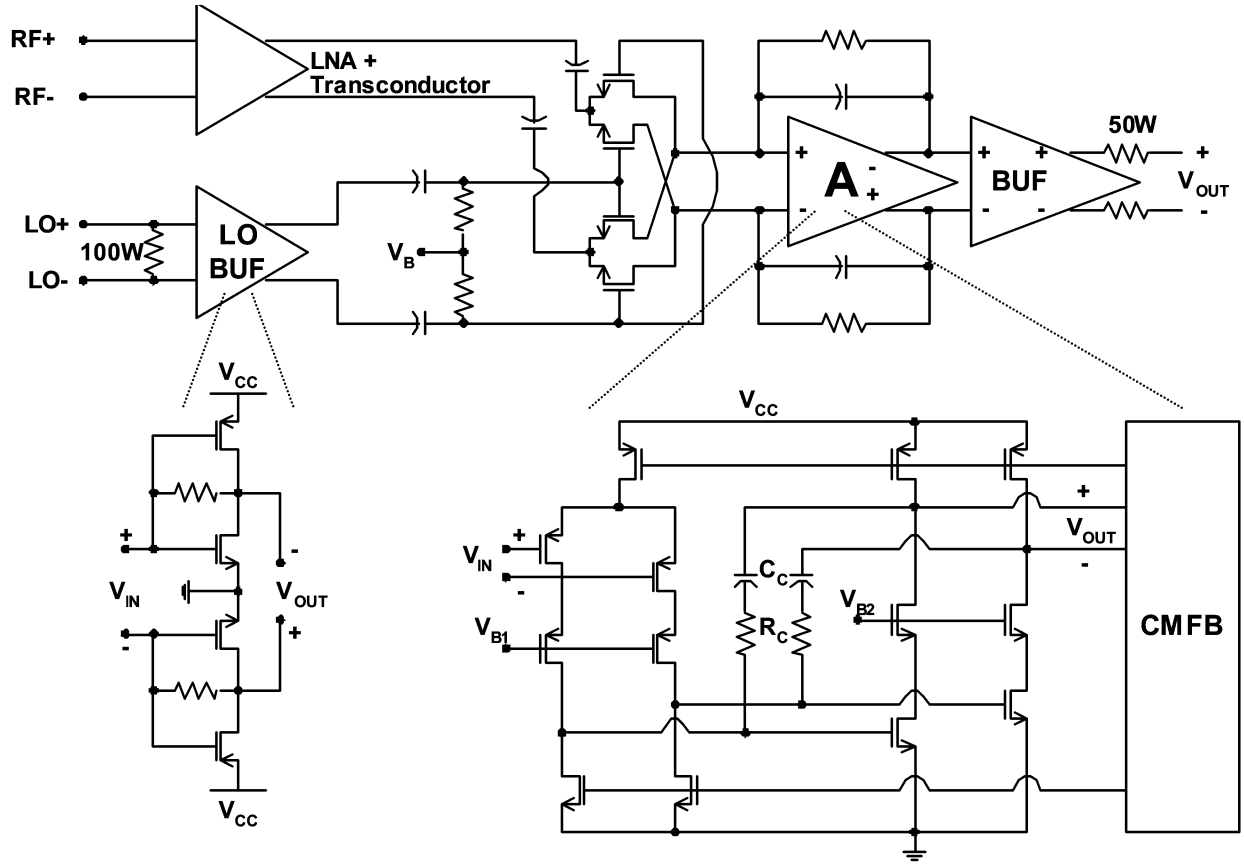

Fig. 1. Simplified schematic of the prototype receiver.

are used. Using inductors usually increases cost, especially when the required number of transceivers is high. Additionally, using inductors may cause pattern density issues in advanced CMOS processing during chemical-mechanical polishing (CMP), and may require several design iterations to achieve the desired frequency tuning, even when EM simulators are used. These LNA's are less preferable for low-cost, multi-frequency applications, particularly if implemented in a low-cost digital technology. Alternatively, a resistive feedback LNA taking advantage of aggressively scaled CMOS can be used [5]. In addition to its small footprint, feedback also improves the linearity of the LNA. Because this type of LNAs does not use high-Q inductors, no additional process steps are necessary for thick top-metal fabrication; for example, the LNA reported in [5] was fabricated in a process which is used for microprocessor mass production. Recent development of resistive feedback LNAs also show that they can operate at low-voltage and low-power while achieving very promising performance [6]–[8].

B. Receiver Components

The prototype receiver front-end is shown in Fig. 1. It consists of a broadband LNA, a transconductor, a passive mixer, a transimpedance amplifier that forms a continuous time active low-pass filter, and 50 Ω output drivers [5] for testing. All circuits are differential or pseudo-differential. Self-biased LO buffers maintain 50% duty cycle and improve the LO edge transition [4], reducing flicker noise from the mixer switching quad. The transimpedance amplifier (TIA) is composed of a two stage op amp with a 2.8 GHz unity gain bandwidth. The high gain of the op amp creates a virtual ground at its input, reducing input voltage swing. Nonlinearity caused by channel resistance is reduced accordingly with smaller voltage swing across the switching quad. Better receiver linearity can be achieved compared to an active Gilbert cell mixer. The broadband equivalent input noise voltage of the TIA in the receiver was reduced by employing very large input devices biased at moderately high current. The input transistors are biased in weak inversion to reduce flicker noise. RC feedback is applied around the op amp to produce a 10 MHz pole frequency.

The resistive feedback LNA reported in [5] is modified to combine DC/AC feedback paths to further reduce area, and with a slight increase in sensitivity to process, voltage and temperature variations. An on-chip low dropout (LOD) regulator, although not implemented in this prototype, could be employed to reduce these sensitivities. The schematic of the LNA is shown in Fig. 2. It could be shown that the noise factor of the LNA can be approximated by

$$F \cong 1 + \frac{R_g}{R_S} + \frac{4}{(g_m R_S)\cdot(g_m R_L)} + \frac{R_S}{R_F}\gamma_{g_m}\frac{f}{f_T}. \quad (1)$$

Here, $R_{\rm g}$ is the equivalent series resistance (gate poly, interconnect/routing, and non-quasi-static resistance), $R_{\rm S}$ is the source impedance (typically 50 Ω, $R_{\rm F}$ is the feedback impedance, f is the operating frequency, $f_{\rm T}$ is the transistor transit frequency, and γ_{g_m} is the excess noise factor for g_m [12]. The five terms on the right hand side of (1), from left to right, represent the

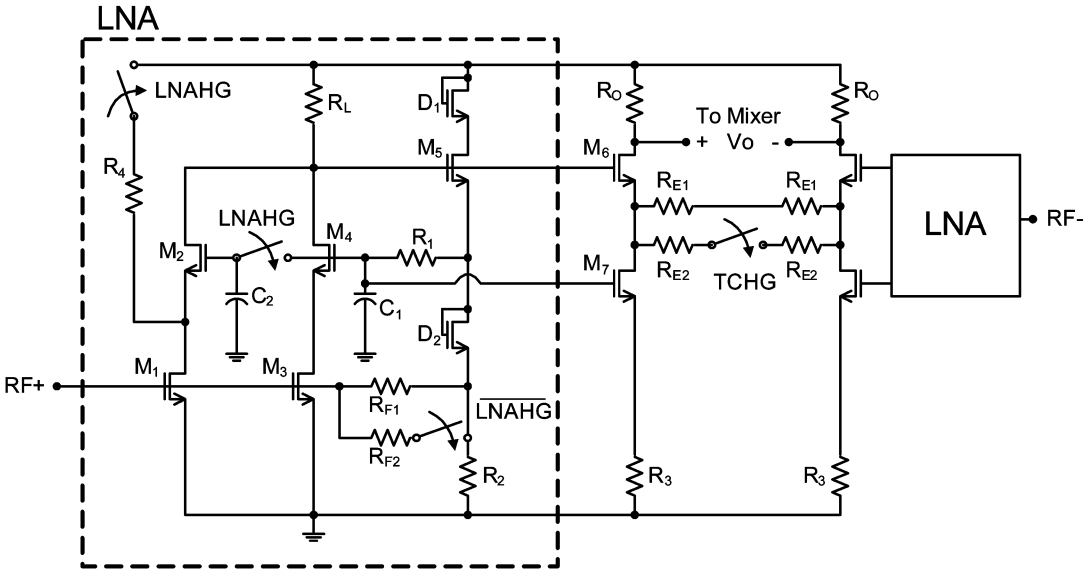

Fig. 2. Simplified LNA schematic.

noise from the source resistance, the equivalent input series resistance, the output load resistance, the feedback resistance, and the transistor channel noise. This LNA topology benefits from technology scaling as $f_{\rm T}$ increases.

In the high-gain mode, LNAHG is set to high (switch closed). M1, M2, M3, M4, RL and R4 constitute a gm-enhanced cascode amplifier. R1, C1 and C2 serve as low-pass filters for biasing. The source follower M5 provides the DC bias voltage for M2 and M4. Level shifter D2 sets the bias point of M1 and M3, and also completes the signal feedback path for input matching. The input matching is achieved by choosing $\mathrm{R_{F1}/A_V} = 50\Omega$, where $\mathrm{A_V}$ is the voltage gain. In the low-gain mode, LNAHG is set to low (switch open). M1, M2 and R4 are disabled to save power. The feedback resistance is reduced from RF1 to RF1||RF2 for acceptable input matching. To maintain correct biasing in both gain modes, the device sizing is chosen appropriately. D1 is included to avoid excessive voltage across M5 for reliability. To improve linearity, the technique for bandwidth extension by positive feedback [5], and the technique of using second order resonance for better input matching [5] are not used. M5 is biased with a resistor instead of a current source transistor to avoid the associated nonlinear output resistance.

The LNA sensitivity is further discussed below. Noise factor is determined by the ratio of resistors and the term $\gamma_{g_m}(f/f_T)$ in (1). Therefore, the LNA noise factor is relatively insensitive to PVT as long as a high $f/f_{\rm T}$ is maintained. The input matching, given by

$$S_{11} = \frac{Z_{\rm in} - R_S}{Z_{\rm in} + R_S} \cong \frac{\frac{1}{g_m}\frac{R_F}{R_L} - R_S}{\frac{1}{g_m}\frac{R_F}{R_L} + R_S} \tag{2}$$

is also not sensitive to PVT if $\mathrm{g_m}$ is reasonably controlled. This is because $\mathrm{R_F/R_L}$ can be well matched by on-chip resistor geometry. Even with a $+-25\%\mathrm{g_m}$ variation, input matching better than -10 dB is still achievable according to (2). The LNA gain is more prone to corner variations. As previously discussed, an on-chip regulator could be used to reduce this sensitivity.

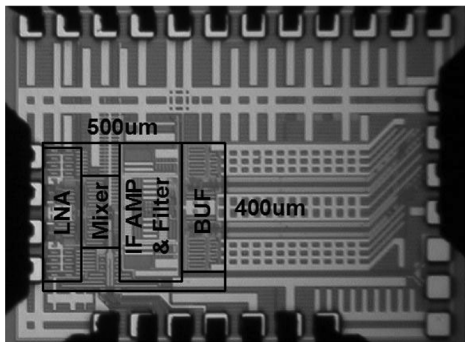

Fig. 3. Die photo of the prototype.

Although it is possible to take the output current of M5 and feed it to the mixer to save current and area, the LO leakage to the LNA input may be larger than desired. Simultaneously achieving input matching and gain switching of the transconductor also becomes more difficult if M5 is employed. Therefore, an additional transconductor stage, comprised of M6, RE1, RE2 and R0, is included. The degenerated current source M7 is also biased by M5. The transconductor has two gain settings. In high gain mode, TCHG is set to high, and the corresponding transconductance is approximately 1/(RE1||RE2). Similarly, in low gain mode, TCHG is set to low, and the corresponding transconductance is approximately 1/RE1. The output current is AC coupled to the passive mixer. This reduces flicker noise to an acceptable level.

III. Measurement

The receiver was fabricated in a high-resistivity substrate (50 Ω-cm), 7 metal, 90 nm CMOS process. Inter-digitated capacitors are used to reduce cost. All measurements reported are on-wafer probing. The chip die photo is shown in Fig. 3. The total active area is 0.2 $\mathrm{mm^2}$ (0.16 $\mathrm{mm^2}$ excluding the 50 Ω buffer). Below 2 GHz, accurate measurement is limited by the hybrid coupler available (2–8 GHz) to the authors, but

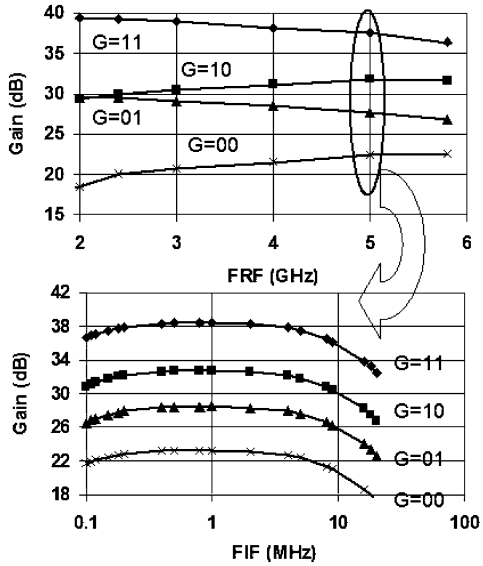

Fig. 4. Conversion gain versus RF and IF frequencies.

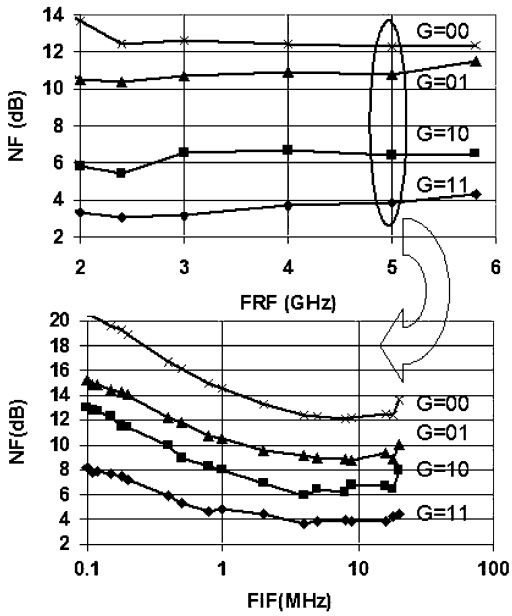

Fig. 5. Noise figure versus RF and IF frequencies.

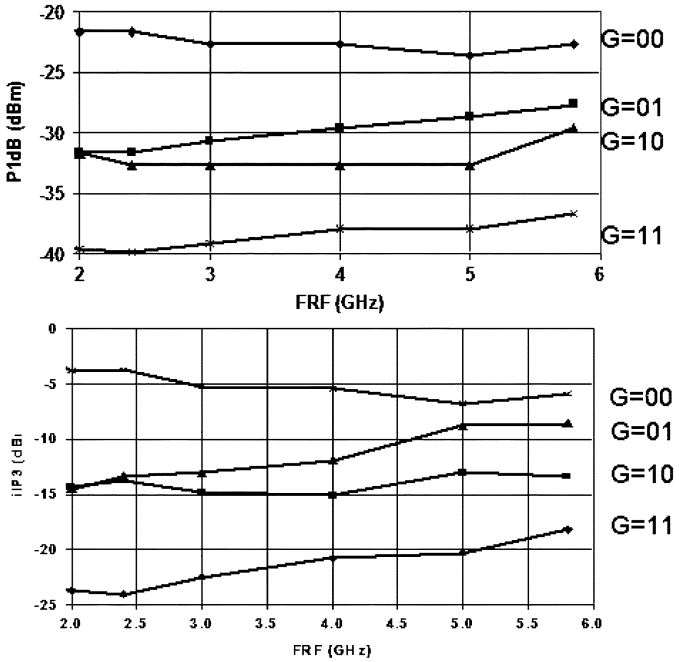

Fig. 6. Linearity versus frequencies.

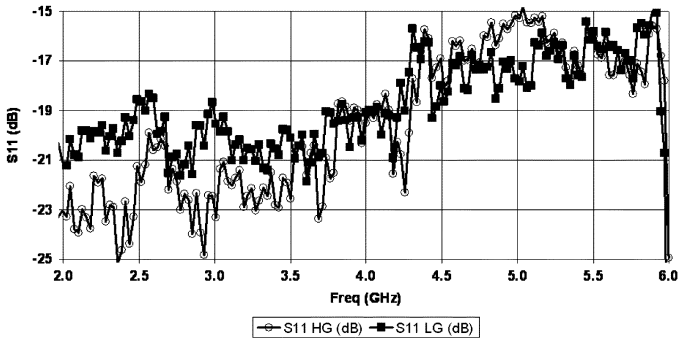

Fig. 7. Input matching versus frequencies.

standalone single-ended LNA measurements verify the low frequency performance. A 2.7 V supply was chosen to allow for the required headroom, and slightly better linearity. All transistors are biased with V_{DS} less than the rated 1.2 V in this process for reliability. Similarly, all routing metal widths, even in critical signal paths, are designed to comply with electrical migration rules.

Fig. 4 shows the conversion gain versus RF (at 5 MHz IF) and IF (at 5 GHz RF) frequencies. The gain control was coded as $\mathrm{G} = [\mathrm{LNAHG}, \mathrm{TCHG}]$. The conversion gain shown in Fig. 4 de-embeds the $\sim$7 dB insertion loss from the standalone 50 Ω buffer. The highest gain setting provides 44 dB of receiver gain. The low pass filter pole can be observed to be 10 MHz. The gain roll off close to DC is due to the output AC coupling capacitors used in the measurement. In the modes with $\mathrm{TCHG} = 0$, the conversion gain increases with RF frequency. This is due to the parasitic capacitance of the switch to connect/disconnect RE2. Fig. 5 shows the double side band noise figure versus RF (at 5 MHz IF) and IF (at 5 GHz RF). The 50 Ω output driver noise contribution is negligible due to the high gain of the receiver. The noise figure in the highest gain mode is 3.9 dB at 5 GHz with a spectrum analyzer (3.4 dB with a NF meter), and the 1/f noise corner is below 200 kHz.

The linearity of the receiver in different gain settings is measured and plotted in Fig. 6. In low gain mode, the gain of the receiver front-end is reduced to improve the linearity of the subsequent blocks. In this mode the linearity of the receiver front-end is also improved. This is desirable for large input signals but is accompanied by some degradation in NF. The input matching for the LNA operating in the high/low gain modes is plotted in Fig. 7. The proposed gain switching technique for the LNA maintains input matching better than -15 dB across 2 GHz to 6 GHz, while maintaining the self-biasing property of the LNA.

The receiver bit error rate (BER) at 5.8 GHz is also verified with 54 Mb/s OFDM 64-QAM signals. Because the I/Q signals required for the BER calculation cannot be produced

TABLE I
PERFORMANCE COMPARISON WITH RECENT PUBLICATIONS

	Freq (GHz)	Gain (dB)	NF (dB)	Output IP3 (dBm)	Power	Process
This Work	< 2-5.8	44	<4.5	20	85mW@2.7V	90nm CMOS
[2]	5	29	5.3	8	NA (18mA)	0.18um CMOS
[3]	5-5.8	26	3.5	24	72mW@1.2V	0.13um CMOS
[9]	5-6	31.5	2.5	21	40mW@2.5V	0.25um SiGe
[10]	2-8	23	4.5	16	51mW@1.2V	65nm CMOS
[11]	1.8 & 5-6	90	4	-9dBm iIP3 (unknown gain)	84mW@1.2V (RX FE only)	0.13um CMOS

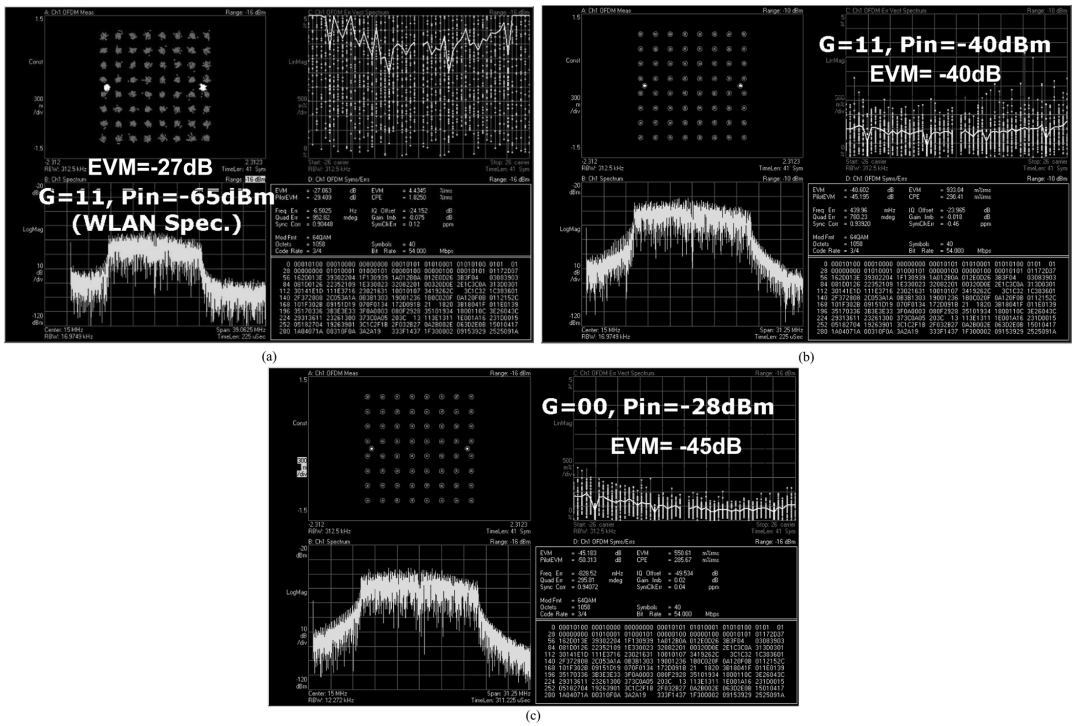

Fig. 8. Example EVM measurement results for 64 QAM in (a) highest gain mode, input $\mathrm{power} = -65$ dBm; (b) highest gain mode, input $\mathrm{power} = -40$ dBm; and (c) lowest gain mode, input $\mathrm{power} = -28$ dBm.

directly in a direct conversion receiver with one channel, a low IF (at 15 MHz) measurement was performed. The roll-off after 10 MHz due to the TIA pole slightly degrades the actual performance of this receiver front-end with this measurement setup. The results are shown in Fig. 8 for three different signal strengths and gain settings: (a) when the signal is at the sensitivity level, -65 dBm, for 802.11 a/b/g, in the highest gain mode; (b) when the signal is -40 dBm in the highest gain mode; and (c) when the signal is at -28 dBm in the lowest gain mode. The best EVM achievable is less than -40 dB. Before the receiver starts compressing, the EVM improves approximately 1 dB per 1 dB of input power increase, as shown in Fig. 9. The two gain modes $\mathrm{G} = 11$ and $\mathrm{G} = 10$ meet 802.11 a/b/g sensitivity requirement. The receiver provides approximately 40 dB of dynamic range in each gain setting mode. The wide dynamic range allowed a very simple gain switching algorithm. The gain switching point does not have to

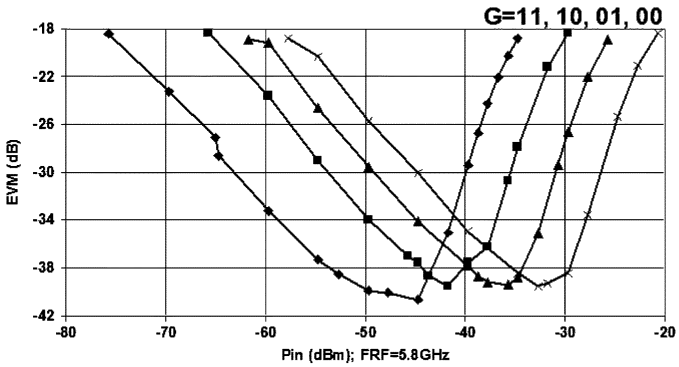

Fig. 9. EVM versus input power at 5.8 GHz (single sideband measurement).

be accurate for the receiver to maintain signal integrity due to the robust performance of the prototype front-end. The LNA

consumes 63 mW and 27 mW in the high and low gain modes, respectively. The LO buffer uses 11 mW at 2 GHz and 13 mW at 5 GHz while the baseband amplifier/filter consumes 13 mW. The 50 Ω output driver consumes 110 mW and is only employed for testing. At 5 GHz, the receiver consumes 85 mW in the highest gain mode. Table I summarizes the performance of this prototype and compares it with recent published broadband receiver front-ends.

IV. Conclusion

An inductor-less prototype receiver fabricated in 90 nm CMOS demonstrates concepts to exploit scaled CMOS technology: direct-conversion simplifies the bandwidth and sampling requirements for subsequent blocks; a resistive feedback LNA provides broadband matching and gain in a small die area; a current mode passive mixer achieves high linearity and produces low flicker noise in an aggressively scaled CMOS process. The prototype provides state-of-the-art performance while occupying only 0.2 mm^2, which is suitable for low-cost, multi-band / standard applications.

Acknowledgment

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Jing-Hong Conan Zhan (S'97–M'98) received the B.S. degree and M.S. degree in electrical engineering from Tsing-Hua University, HsinChu, Taiwan, R.O.C., in 1996 and 1997, respectively. His M.S. thesis focused on side-polished fiber fabrication and theoretical analysis.

After completing compulsory services in the Taiwanese Army as a secondary lieutenant from 1997 to 1999, he joined MediaTek, HsinChu, Taiwan as a logic design engineer until 2001. He developed the data path and spindle motor control circuitry for MediaTek's optical storage products. He then pursued his Ph.D. degree in electrical engineering and computer science in Cornell University, Ithaca, NY, focusing on VCO and high-speed clock and data recovery circuitry using BiCMOS and CMOS. He received the Ph.D. degree in 2004 and joined Intel Communication Circuit Lab in Hillsboro, OR, as a Senior Design Engineer. His research focused on fabricating low-cost radios on CMOS technologies for microprocessors production. In 2006, he joined MediaTek RF division as a technical manager, where he led a silicon tuner front-end design team. He co-developed an all-digital PLL for wireless applications. His recent interest is in millimeter-wave circuit design.

Brent R. Carlton (S'01–M'02) was born in Gillette, WY. He received the B.S. and M.S. degrees in electrical engineering from Brigham Young University, Provo, UT, in 2003.

He has been a Wireless Circuits Researcher with Intel's Corporate Technology Group, Hillsboro, OR, since 2002. While working for Intel he has worked with wireless receiver design, testing and architecture. Some of the circuits he has designed and tested include both wideband and narrowband LNA circuits, receive mixers, baseband amplifiers, and mixed signal circuits.

Stewart S. Taylor (S'74–M'94–SM'99–F'08) received the Ph.D. degree in electrical engineering from the University of California at Berkeley in 1978.

He is a Senior Principal Design Engineer at Intel, where he has been employed since January 2003. His current research focus is on radio architecture and circuit design that leverages the strengths and compensates for the weaknesses of CMOS technology. Before joining Intel, he was with Tektronix, TriQuint, and Maxim. He has taught part-time at Portland State University, Oregon State University, and the Oregon Graduate Institute for 29 years. He has developed high-speed analog, data converter, and wireless/RF integrated circuits. He has 42 issued patents, and 22 pending.

Dr. Taylor served on the program committee of the IEEE International Solid-State Circuits Conference for ten years, chairing the Analog Subcommittee for four years. He was the conference Program Chair in 1999. He was an Associate Editor of the IEEE Journal of Solid-State Circuits, and the recipient of the IEEE Third Millennium Medal for Outstanding Achievements and Contributions from the Solid-State Circuits Society.