Analog Circuit Design Using Symbolic Math Toolboxes: Demonstrative Examples

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***Abstract*— In this article, a synthesis methodology for analog circuit design is presented. This methodology utilizes symbolic math tools to systematically and exhaustively search for candidate analog circuits avoiding tedious manual work. The two-port network matrix representation of active devices, such as MOS transistors, paves the way for efficiently using advanced symbolic math toolboxes (e.g., in MAPLE or MATLAB) to automate the generation of new analog circuits and further investigate the effects of nonidealities and parasitics. Using this synthesis methodology new amplifiers, filters, and oscillators can be obtained starting from a predefined structure. This article aims to motivate and provide an overview of the current status of research in this area. In addition, two detailed design examples of a family of differential filters and a family of differential oscillators along with their simulations and measurement results are provided to illustrate and verify the synthesis methodology.**

***Index Terms*— Amplifiers, analog circuits, analog filters, CAD tools, circuit synthesis, oscillators, two-port networks.**

I. Introduction

DESPITE the extremely rapid advances in digital design, analog circuits will continue to play a crucial role in future electronic systems [1]. Analog circuits are essential and irreplaceable for example in communication systems. In a typical transmitter/receiver circuit, a digital-to-analog converter, an oscillator, a power amplifier, and a low noise amplifier are all essential blocks. Analog filters are used to select between different channels or to suppress interference [2]. However, the increasing demand for high-data-rate communication systems has promoted the investigation of new architectures in the fifth-generation (5G) communication standards [3]–[6]. Many millimeter-wave bands have been chosen for 5G such as 24.25–26.25, 26–28, 27.5–29.5, and 28–31 GHz [5], [7]. At these frequencies, beamforming networks are used to increase antenna directivity and overcome path losses[1] [3]. In wide-band beamformers, all-pass filters (APFs) are key building blocks, since they function as true-time-delay (TTD) cells [4], [8]–[21].

Given the above, innovations in analog circuits including filters, oscillators, and amplifiers are always needed in order to provide better performance, particularly at these high frequencies, and to overcome other design challenges. Investigating new analog circuits is exhausting when it comes to examining all possible circuits of any given well-defined structure due to the tremendous amount of time needed to perform hand analysis in order to obtain valid circuits. For example, assume that it is required to find all possible second-order voltage-mode filters that can be obtained using a single-transistor common-source amplifier topology with three impedances: a source impedance, a load impedance, and one extra impedance. Any of these three impedances can contain series or parallel combinations of R, L, and C components provided the dc biasing of the transistor remains valid. Such a problem is clearly difficult to solve manually. However, with the power of the symbolic math toolboxes available nowadays, and with the help of two-port network models, this problem can be solved in an automated manner with all possible valid circuits found. It is important to note that employing CAD tools in analog circuit design is not a new idea since a lot of work has been reported on using CAD tools in sizing of analog integrated circuits as well as in the IC layout generation [22]–[29]. Moreover, there are many artificial intelligence-based techniques that have been used in the literature to design analog circuits [30]–[32]. However, these contributions are mostly optimization-based and do not employ symbolic math toolboxes; which greatly limits their circuit synthesis value (see [32] and the references therein). By contrast, the methodology described here relies on symbolic math tools to automate the process of synthesizing new analog circuits including filters, oscillators, and amplifiers.

Recently, the authors of this work have been successful in proposing numerous new analog circuits using the two-port network modeling technique and the outstanding symbolic math capabilities available in MAPLE [13], [15], [18], [33]–[38]. This article seeks to promote this circuit synthesis method and share it with a wider audience of the circuits and systems society aided

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[1]The space loss factor = $(\lambda/4\pi R)^2$. For $R = 1$ m at 30 GHz, this factor is equal to -62 dB.

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with demonstrations using three different design examples. Section II describes the transmission matrix model of an MOS transistor essential for circuit analysis of any possible topology. Section III provides the necessary algorithms needed to perform an exhaustive search for new analog circuits. Section IV demonstrates the design methodology by three design examples: a fully differential filter structure, a differential oscillator structure, and a common-gate amplifier analysis example. This article is concluded in Section V.

II. MOSFET Transmission Matrix

The optimum circuit analysis technique that can exploit the power of symbolic math CAD tools has to rely on using matrices. In this regard, two-port networks arise as the most suitable candidate. Classical textbooks [39]–[41] tend to analyze transistor-based analog circuits using mesh and nodal equations and rarely use two-port network based analysis. However, for automating the synthesis of analog circuits, the use of two-port networks is crucial because the small-signal equations describing the transistor are presented in matrix form. The most convenient matrix to be used is the transmission matrix $[T]$, which is also known as the $ABCD$ matrix [40]. The reason is that this matrix has all the input variables on one side and the output variables on the other side and it is cascadable such that the output of one network can be directly connected as an input to a subsequent network [38]. The general two-port network transmission matrix is defined by

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} = [T] \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{1}$$

where V_1 and I_1 are the voltage and current at the input port, while V_2 and I_2 are those at the output port of a linear system. The current I_2 is always considered to be leaving the network, and the transmission parameters are determined as

$$\begin{aligned} A &= a_{11} = \left.\frac{V_1}{V_2}\right|_{I_2=0}, \quad B = a_{12} = -\left.\frac{V_1}{I_2}\right|_{V_2=0} \\ C &= a_{21} = \left.\frac{I_1}{V_2}\right|_{I_2=0}, \quad D = a_{22} = -\left.\frac{I_1}{I_2}\right|_{V_2=0}. \end{aligned} \tag{2}$$

Note that a_{11} and a_{22} are dimensionless voltage and current gains respectively, a_{12} is the negative short-circuit transfer impedance and a_{21} is the open-circuit transfer admittance. Fig. 1 shows the NMOS transistor symbol along with three small-signal equivalent circuits with different parasitic elements. Fig. 1(b) shows the simplest small-signal model where g_m is the small-signal transconductance. The output resistance r_o in Fig. 1(c) is used to model the channel-length modulation. Fig. 1(d) shows a more sophisticated model that also includes the parasitic gate-to-source capacitance C_{gs} and gate-to-drain capacitance C_{gd}. Of course, more sophisticated equivalent circuits exist and can also be used. Even without knowing the equivalent circuit, the transmission matrix can be experimentally measured under specific biasing condition using a network analyzer. Therefore, there is no limitation on the level of the model complexity that can be incorporated in the two-port matrix. In this work, we will consider a three-terminal two-port network to represent the NMOS transistor model where the input port is between the *Gate (G)* and *Source (S)* terminals, and the output port is between the *Drain (D)* and *Source (S)* terminals. The transmission matrix of the models in Fig. 1(b)–(d) is given in the following equations:

$$[T] = \begin{bmatrix} 0 & -\dfrac{1}{g_m} \\ 0 & 0 \end{bmatrix} \tag{3a}$$

$$[T] = \begin{bmatrix} -\dfrac{1}{g_m r_o} & -\dfrac{1}{g_m} \\ 0 & 0 \end{bmatrix} \tag{3b}$$

$$[T] = \begin{bmatrix} \dfrac{(1/r_o)+sC_{\mathrm{gd}}}{sC_{\mathrm{gd}} - g_m} & \dfrac{1}{sC_{\mathrm{gd}} - g_m} \\ \dfrac{\left(C_{\mathrm{gd}}C_{\mathrm{gs}}r_o s + C_{\mathrm{gd}}g_m r_o + C_{\mathrm{gs}} + C_{\mathrm{gd}}\right)s}{sC_{\mathrm{gd}} - g_m} & \dfrac{\left(C_{\mathrm{gs}}+C_{\mathrm{gd}}\right)s}{sC_{\mathrm{gd}} - g_m} \end{bmatrix}. \tag{3c}$$

Note that the bias quantities (I_D and $V_{\mathrm{gs}} - V_{\mathrm{TH}}$) and the physical parameter W/L are selected so that the transistors operate in saturation and provide the desired small-signal parameter g_m. Hence, this is already taken into consideration in the two-port matrix models [(3a)–(3c)] as g_m.

Matrices of other types of semiconductor devices such as BJT, SiGe, and GaN transistors can be found in a similar manner. We can even consider complex building blocks such as operational amplifiers and current conveyors.

III. Symbolic Math Tools for Analog Circuit Synthesis

This section illustrates the utilization of the symbolic math tools in analog circuit design by providing the general steps to be followed by detailed design examples. The automated generation process has the following steps.

1) Decide the required function of the circuits (e.g., filters and oscillators).
2) Select a general architecture employing transistors and replace them with their two-port network models. Chosen architectures might be based for example on a single transistor, a differential-pair, a cross-coupled pair or any other basic cell.
3) Decide on the number and location of impedances that surround the basic cell in step 2.
4) Carefully decide all suitable sets of components for each impedance in step 3 to exclude any invalid possibility. For example, having an inductor connected between drain and source terminals of a transistor is not permitted.
5) Write down all nodal and/or mesh equations of the architecture in step 2.
6) Enter the following to the symbolic math tool.
   a) The transmission matrices [see (3a)–(3c)] to be used.
   b) The list of all suitable sets of impedances determined in step 4.
   c) The circuit equations obtained in step 5.
7) Solve for the general transfer function (or any other frequency domain relation) based on step 1 for the

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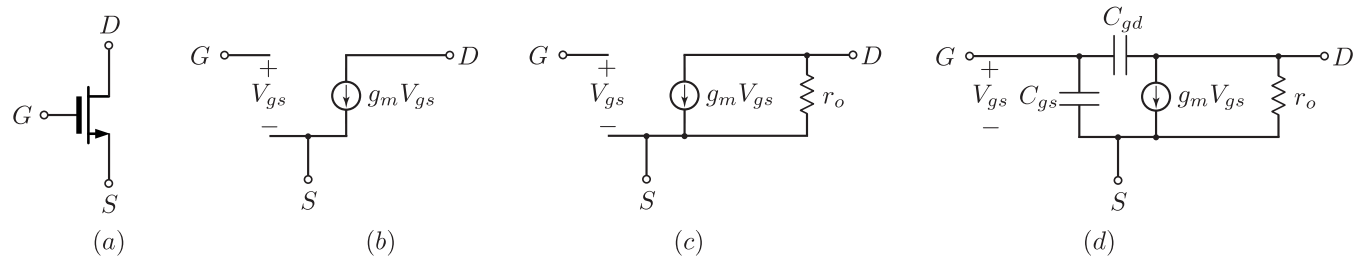

Fig. 1. (a) NMOS transistor symbol. (b) Basic MOS small-signal model. (c) Channel-length modulation effect represented by a resistor r_o. (d) MOS small-signal model including the major parasitic capacitors C_{gs} and C_{gd}.

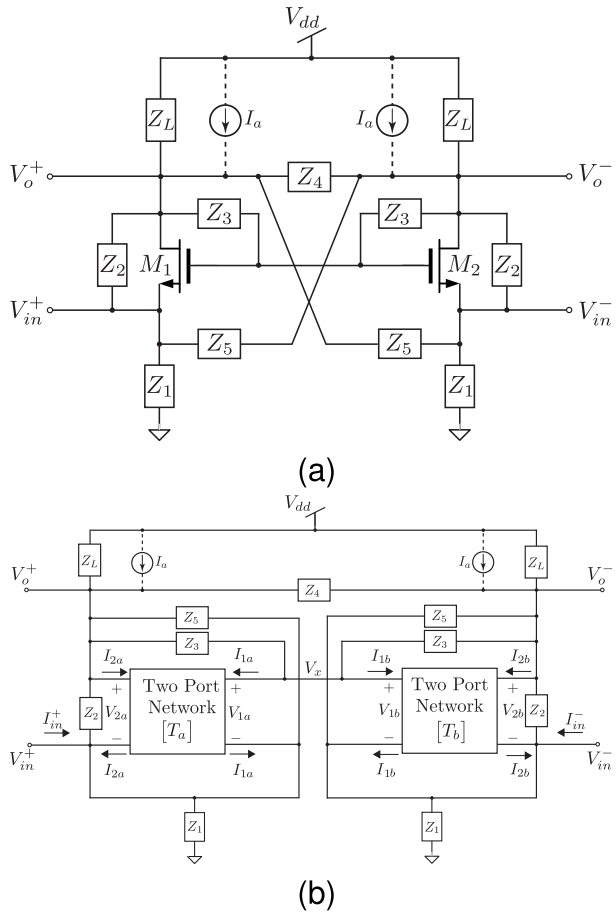

Fig. 2. Schematic of (a) fully differential filter structure based on the common-gate differential-pair surrounded by passive impedances and (b) its two-port network representation used in the symbolic analysis.

architecture then examine all possible circuits by iterating all the impedance combinations provided in step 4.

Note that it is always better to start with the simple transmission matrix in (3a), identify the candidate circuits for which the effects of nonidealities are to be determined and then rerun the code with more complex matrices like (3c) or experimentally measured ones.

IV. Design Examples

The above steps were applied in [34] to generate 876 fully differential second-order active filters based on the two-transistor *common-source* differential-pair cell. Here, we explain how to generate all possible fully differential second-order filters albeit using a *common-gate* differential-pair cell.

A. Common-Gate Differential Filters

1) Synthesis: Referring to step 3, we decide to include six impedances ($Z_{1\to 5}$, and Z_L) in the surrounding of a two-transistor common-gate cell, as shown in Fig. 2(a). An optional current source I_a is placed around Z_L to ensure proper biasing conditions. Referring to step 4, we provide a list of all possible impedances while allowing the transistors to be biased properly in Table I. As seen, these impedances might be individual components or series/parallel combinations. According to step 5, we derive the following set of nodal and mesh equations for the circuit in Fig. 2(b) where the two transistors have been replaced by two-port network representations:

$$0 = I_{\text{in}}^+ + I_{1a} + I_{2a} + \frac{(0 - V_{\text{in}}^+)}{Z_1} + \frac{(V_o^+ - V_{\text{in}}^+)}{Z_2} + \frac{(V_o^- - V_{\text{in}}^+)}{Z_5} \tag{4a}$$

$$0 = I_{\text{in}}^- + I_{1b} + I_{2b} + \frac{(0 - V_{\text{in}}^-)}{Z_1} + \frac{(V_o^- - V_{\text{in}}^-)}{Z_2} + \frac{(V_o^+ - V_{\text{in}}^-)}{Z_5} \tag{4b}$$

$$I_{2a} = \frac{(V_{\text{in}}^+ - V_o^+)}{Z_2} + \frac{(V_x - V_o^+)}{Z_3} + \frac{(V_o^- - V_o^+)}{Z_4} + \frac{(V_{\text{in}}^- - V_o^+)}{Z_5} + \frac{(0 - V_o^+)}{Z_L} \tag{4c}$$

$$I_{2b} = \frac{(V_{\text{in}}^- - V_o^-)}{Z_2} + \frac{(V_x - V_o^-)}{Z_3} + \frac{(V_o^+ - V_o^-)}{Z_4} + \frac{(V_{\text{in}}^+ - V_o^-)}{Z_5} + \frac{(0 - V_o^-)}{Z_L} \tag{4d}$$

$$I_{1a} = \frac{(V_o^+ - V_x)}{Z_3} + \frac{(V_o^- - V_x)}{Z_3} - I_{1b}$$

$$V_o^+ = V_{\text{in}}^+ + V_{2a}, \quad V_o^- = V_{\text{in}}^- + V_{2b} \tag{4e}$$

$$V_{\text{in}}^+ = V_x - V_{1a}, \quad V_{\text{in}}^- = V_x - V_{1b} \tag{4f}$$

$$V_{1a} = a_{11}V_{2a} - a_{12}I_{2a}, \quad V_{1b} = b_{11}V_{2b} - b_{12}I_{2b} \tag{4g}$$

$$I_{1a} = a_{21}V_{2a} - a_{22}I_{2a}, \quad I_{1b} = b_{21}V_{2b} - b_{22}I_{2b} \tag{4h}$$

where $a_{11} \to a_{22}$ (respectively, $b_{11} \to b_{22}$) are the parameters of the two transistor transmission matrices. At this stage the designer has the option of using identical transistors or different transistors. Of course, having two identical transistors is more practical and hence $b_{11} \to b_{22}$ in the above equations can be replaced by $a_{11} \to a_{22}$.

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Limit the len of Z_array to 2-3

Z = (Zi, ZL) for all i

TABLE I

POSSIBLE IMPEDANCES THAT ALLOW THE TRANSISTORS IN FIG. 2(A) TO BE PROPERLY BIASED. THE + SIGN REFERS TO A SERIES CONNECTION AND THE // SIGN REFERS TO A PARALLEL CONNECTION

Impedance	Possibilities
Z_1	R_1 plus all the combos in Z3,4,5,L
Z_2	R_2, C_2, $R_2//C_2$, R_2+C_2, L_2+C_2, $R_2+L_2+C_2$, $R_2+(L_2//C_2)$, $R_2//(L_2+C_2)$
$Z_{3,4,5,L}$	R_i, C_i, L_i, $R_i//C_i$, R_i+C_i, L_i+C_i, $L_i//C_i$, $R_i+L_i+C_i$, $R_i//L_i//C_i$, $R_i+(L_i//C_i)$, $R_i//(L_i+C_i)(i=3,4,5,L)$

We now proceed to use MAPLE to solve the set of equations given above and find the transfer function $H(s) = (V_o^+ - V_o^-)/(V_{\text{in}}^+ - V_{\text{in}}^-)$, as shown in Algorithm 1. When we include all six impedances, the transfer function is found to be

$$H(s) = \frac{Z_3 Z_4 Z_L [Z_2 Z_5 (a_{11} - 1) + a_{12}(Z_5 - Z_2)]}{Z_A \left[a_{11} + \frac{a_{12}}{Z_L} + \frac{a_{12}}{Z_5} + \frac{2a_{12}}{Z_4} + \frac{a_{12}}{Z_3} + \frac{a_{12}}{Z_2} \right]} \tag{5}$$

where $Z_A = Z_2 Z_3 Z_4 Z_5 Z_L$. Note that this transfer function is independent of Z_1 and hence, this topology can operate with a differential input current signal to provide transimpedance filters with $H(s) = (V_o^+ - V_o^-)/(I_{\text{in}}^+ - I_{\text{in}}^-)$. Also, this topology can operate in a fully differential current mode if needed. However, we focus here only on fully differential voltage-mode filters and restrict $Z_1 = R_1$ to insure a path for dc bias current of $M_{1,2}$ to flow to ground.

Using the simplified transistor transmission matrix in (3a), the above general transfer function simplifies to

$$H(s) = \frac{Z_3 Z_4 Z_L (Z_2 Z_5 g_m - Z_2 + Z_5)}{Z_A \left[\frac{1}{Z_L} + \frac{1}{Z_5} + \frac{2}{Z_4} + \frac{1}{Z_3} + \frac{1}{Z_2} \right]}. \tag{6}$$

Table II presents five possible subset transfer functions obtained from (6) by reducing the number of impedances along with the number and type of possible filters from each transfer function. Note that straightforward combinational analysis $C(5,1) = 5$, $C(5,2) = 10$, $C(5,3) = 10$, $C(5,4) = 5$, and $C(5,5) = 1$ yields a total of 31 possible transfer functions that can be derived from the topology in Fig. 2. The first row in Table II shows that if the topology is used with the two impedance Z_3 and Z_L only, this would result in 17 bandpass (BP) filters, four bandstop (BS) filters and four APFs. Alternatively, if the two impedances Z_5 and Z_L are used, this would result in two BP filters, two BS filters, and eight AP filters, as shown in the second row of Table II. The strength of the symbolic synthesis technique is very clear from these results since it is impossible using hand calculation to discover all these different possibilities which accumulate to 69 BP filters, 16 BS filters and 42 AP filters using at most three impedances. Of equal importance is the discovery of no possible lowpass (LP) or highpass (HP) filters.

Algorithm 2 computes the filter parameters from any of the $H(s)$ found in Algorithm 1. If the search space is restricted to second-order filters, then the corresponding standard form is known to be

$$H(s) = K \frac{N_{XY}(s)}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2} \tag{7}$$

where ω_o is the pole frequency, K is the filter gain ($K \in \{K_{\text{LP}}, K_{\text{BP}}, K_{\text{HP}}, K_{\text{BS}}, K_{\text{GE}}\}$), Q is the pole quality factor, $N_{XY}(s) \in \{N_{\text{BS}}(s), N_{\text{BP}}(s), N_{\text{HP}}(s), N_{\text{LP}}(s), N_{\text{GE}}(s)\}$ with $N_{\text{BS}}(s) = s^2 + \omega_o^2$, $N_{\text{BP}}(s) = (\omega_o/Q)s$, $N_{\text{HP}}(s) = s^2$, $N_{\text{LP}}(s) = \omega_o^2$, and $N_{\text{GE}}(s) = s^2 + (\omega_o/Q_z)s + \omega_o^2$, each representing BS, BP, HP, LP, and gain equalizer (GE) filters, respectively. For $Q_z = -Q$ an AP filter is generated. The different filter types are determined and classified in Algorithm 3. Table III provides samples of obtained filters based on various choices of impedances taken from rows 1, 2, and 5 in Table II, respectively. A flowchart of the filter synthesis process is shown in Fig. 3. Note that the average execution time for Algorithms 1–3 using three impedances (e.g., $Z = [Z_2, Z_5, Z_L]$) is 14.76 s on laptop with a 2.5-GHz Intel Core i5 processor and 4 GB of RAM.

TABLE II

LIST OF POSSIBLE TWO AND THREE IMPEDANCE SETTINGS AND CORRESPONDING TRANSFER FUNCTIONS. THE NUMBER AND TYPE OF POSSIBLE FILTERS FROM EACH TRANSFER FUNCTION ARE ALSO LISTED

Impedances	No	$H(s)$	BP	BS	GE/AP
Z_3, Z_L	1	$\frac{g_m Z_3 Z_L}{Z_3+Z_L}$	17	4	4
Z_5, Z_L	2	$\frac{Z_L(g_m Z_5 - 1)}{Z_5+Z_L}$	2	2	8
Z_2, Z_4, Z_L	3	$\frac{Z_4 Z_L (g_m Z_2 + 1)}{Z_2(Z_4+2Z_L)+Z_4 Z_L}$	24	4	8
Z_2, Z_5, Z_L	4	$\frac{Z_L(Z_2 Z_5 g_m - Z_2 + Z_5)}{Z_2(Z_5+Z_L)+Z_L Z_5}$	2	2	12
Z_3, Z_5, Z_L	5	$\frac{Z_3 Z_L (g_m Z_5 - 1)}{Z_3(Z_5+Z_L)+Z_L Z_5}$	24	4	10

TABLE III

SAMPLE OF POSSIBLE FILTERS BASED ON VARIOUS CHOICES OF IMPEDANCES TAKEN FROM TABLE II

Z impedances	Filter	K	ω_o
		Q	Q_z
$L_5 + C_5, R_L$	AP1	$g_m R_L$	$\sqrt{\frac{1}{L_5 C_5}}$
		$\frac{1}{R_L}\sqrt{\frac{L_5}{C_5}}$	$-g_m\sqrt{\frac{L_5}{C_5}}$
$L_3, R_L//C_L$	BP1	$g_m R_L$	$\sqrt{\frac{1}{L_3 C_L}}$
		$R_L\sqrt{\frac{C_L}{L_3}}$	–
$L_3 + C_3, R_5, R_L$	BS1	$\frac{R_L(g_m R_5 - 1)}{R_5+R_L}$	$\frac{1}{\sqrt{L_3 C_3}}$
		$\frac{R_5+R_L}{R_5 R_L}\sqrt{\frac{L_3}{C_3}}$	–

2) Verification: The accuracy of the reported results here was tested on the APF AP1 listed in the first row of Table III which is depicted in Fig. 4(a). The transfer function of this filter using the matrix of (3a) is given by

$$H(s) = g_m R_L \frac{s^2 - \left(\frac{1}{g_m L_5}\right)s + \frac{1}{L_5 C_5}}{s^2 + \left(\frac{R_L}{L_5}\right)s + \frac{1}{L_5 C_5}}. \tag{8}$$

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Algorithm 1 Computing the Transfer Function $H(s)$ for the Common-Gate Differential Filter in Fig. 2(b)

Input T-matrix from equations:
if T=1 **then** transmission matrix in (3a) **end if**:
if T=2 **then** transmission matrix in (3b) **end if**:
if T=3 **then** transmission matrix in (3c) **end if**:
Input impedance matrix $m \times n$ **Z:**
Zz1:=<row #1 from Table I >:
Zz2:=<row #2 from Table I >:
Zz3:=<row #3 from Table I with $i = 3$>:
Zz4:=<row #3 from Table I with $i = 4$>:
Zz5:=<row #3 from Table I with $i = 5$>:
ZzL:=<row #3 from Table I with $i = L$>:
Input nodal and mesh equations:
Eqs={(4a)-(4h)}
Output: Transfer function $H(s)$
for $i = 1 : m$ **do**
  $Z_1 = Z[i, 1]$:
  $Z_2 = Z[i, 2]$:
  $Z_3 = Z[i, 3]$:
  $Z_4 = Z[i, 4]$:
  $Z_5 = Z[i, 5]$:
  $Z_L = Z[i, 6]$:
% Solve for the variables
  soln=solve({Eqs},{V_{in}^+, V_{in}^-, V_o^+, V_o^-, I_{1a}, I_{2a}, V_{1a}, V_{2a}, V_{1b}, V_{2b}, I_{1b}, I_{2b}, I_{in}^+, I_{in}^-}):
% Assign the variables
  assign(soln):
% Compute the transfer function
  $H(s)_i$ =($V_o^+ - V_o^-$)/($V_{in}^+ - V_{in}^-$):
end for

Remark 1. Note that $n = 6$ while m depends on the selected impedances to be included in the analysis and the number of possible choices from the combinations in Table I. For example, if three impedances are selected such that $Z = [Z_2, Z_5, Z_L]$, then $m = 8 \times 11 \times 11 = 968$. In the previous example we assume the remaining impedances Z_3, Z_4 are open circuit ($= \infty$).

The pole/zero frequency (ω_o, ω_z), pole and zero quality factors (Q, Q_z) are given in Table III. Note that the dimensions and bias current of $M_{1,2}$ should be selected to satisfy the condition $g_m = 1/R_L$ which is necessary to ensure that $Q_z = -Q$ for correct APF transfer function. From the Q expression of AP1, it can be easily shown that this circuit is able to generate complex conjugate poles ($Q > 1/2$) with a unity gain since $K = g_m R_L = 1$. The phase shift $\phi(\omega)$, group delay $\tau_g(\omega)$, and input impedance are given, respectively, by

$$\phi(\omega) = -2\tan^{-1}\left[\frac{\tau_{go}}{2} \times \frac{\omega}{1 - \left(\frac{\omega}{\omega_o}\right)^2}\right] \tag{9}$$

$$\tau_g(\omega) = \tau_{g_o} \times \frac{(\omega^2/\omega_o^2 + 1)}{(\omega^2/\omega_o^2 - 1)^2 + \frac{\tau_{go}^2\omega^2}{4}} \tag{10}$$

$$Z_{\text{in}}(s) = \frac{g_m R_1}{g_m R_1 + 1} \frac{s^2 + \left(\frac{R_L}{L_5}\right)s + \frac{1}{L_5 C_5}}{s^2 + \left[\frac{(g_m R_1 R_L + R_1 + R_L)}{L_5(g_m R_1 + 1)}\right]s + \frac{1}{L_5 C_5}} \tag{11}$$

Algorithm 2 Determining the Filter Parameters From the Numerator and Denominator Coefficients of (7)

Input: Transfer function $H(s)$
Outputs: Filter parameters (Q, Q_z, ω_o, K_{HP}, K_{LP}, K_{BP})
Initialization: FL $= 0$ % temporary variable acting as a flag
for $i = 1 : m$ **do**
% find H(s) order
  TOrder(i)=degree(denom(i),s)+degree(numer(i),s) :
% Determine the coefficients of the denominator of H(s)
  a2(i)=coeff(denom,s,2) :
  a1(i)=coeff(denom,s,1):
  a0(i)=coeff(denom,s,0):
  if a2(i)=0 or a1(i)=0 or a0(i)=0 or TOrder(i)>=5 **then**
  FL $= 1$
    a2(i)=1, a1(i)=1, a0(i)=1 % Invalidate the results
  end if
% Start of computations for ω_o, Q, Bandwidth
  wo(i)=sqrt(a0(i)/a2(i)): Q(i) :=(a2(i)/a1(i))·wo(i):
  Bandwidth(i):=(wo(i)/Q(i))
% Determine the coefficients of the numerator of H(s)
  b2(i)=coeff(numer,s,2) :
  b1(i)=coeff(numer,s,1):
  b0(i)=coeff(numer,s,0):
% Start of computations for ω_z, Q_z
  wz(i)=sqrt(b0(i)/b2(i)): Qz(i)=(b2(i)/b1(i))·wz(i):
% Start of computations for the filter gains
  K_HP(i):=b2(i)/a2(i):
  K_BP(i):=b1(i)/a2(i)/Bandwidth(i):
  K_LP(i):=b0(i)/a2(i)/wo(i)^2:
end for

where $\tau_{\text{go}} = 2R_L C_5$ is the delay at dc. Note that implementing C_5 by a varactor provides continuous tunability over the low-frequency delay values. For $Q = 1/\sqrt{3}$, the maximum flat group delay response is achieved and for $Q > 1/\sqrt{3}$, the delay response will have a peak at a frequency of $\omega_{\text{peak}} = \omega_o((4 - Q^{-2})^{1/2} - 1)^{1/2}$ which can be used to extend the delay bandwidth. Examining the input impedance expression in (11), we note that at very low and very high frequencies, $Z_{\text{in}} \approx (1/g_m)//R_1$. It is worth mentioning that using resistor R_1 to provide the dc bias current for the common-gate transistors $M_{1,2}$ is more noise efficient compared to using a simple current source.

The transmission matrix in (3b) can be used to further study the nonidealities of the circuit. Using this matrix reveals that r_o has no effect on the pole/zero frequency. However, it changes the filter gain to $\hat{K} = ((R_L(g_m r_o + 1))/(R_L + r_o))$, and the pole and zero quality factors to

$$\hat{Q} = \frac{R_L + r_o}{R_L r_o}\sqrt{\frac{L_5}{C_5}}, \quad \hat{Q}_z = -\frac{g_m r_o + 1}{r_o}\sqrt{\frac{L_5}{C_5}} \tag{12}$$

respectively. Conveniently, the condition $g_m = 1/R_L$ still holds to satisfy $\hat{Q}_z = -\hat{Q}$. The effect of the transistor parasitic capacitances (C_{gs}, C_{gd}) can be found using the matrix in (3c). Two additional poles at $\omega_{p1} \approx 1/[(R_s//(1/g_m))C_{\text{in}}]$ and $\omega_{p2} \approx 1/(R_L C_L)$ result where $C_{\text{in}} = C_{\text{gs}} + C_{\text{sb}}$ and $C_L = C_{\text{gd}} + C_{\text{db}}$ (C_{sb} is the source

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Algorithm 3 Determining the Filter Type From Coefficients K_{LP}, K_{HP} and K_{BP} of Transfer Function $H(s)$. Inputs Are ω_o, Q, Q_z, K_{LP}, K_{HP}, K_{BP} and Empty Matrices of Filter Type_Result. Output Filter Type Is Stored in Matrices Indicated by <<>>

Inputs: Filter parameters (Q, Q_z, ω_o, K_{HP}, K_{LP}, K_{BP})
% Compute all Highpass filter results
if FL $= 0$ and K_BP(i)=0 and K_LP(i)=0 **then**
HPresult:=<HPresult,<Z|wo|Q|K_HP>>:
CountHP:=CountHP+1:
end if

% Compute all Bandpass filter results
if FL $= 0$ and K_HP(i)=0 and K_LP(i)=0 **then**
BPresult:=<BPresult,<Z|wo|Q|K_BP>>:
CountBP:=CountBP+1:
end if

% Compute all Lowpass filter results
if FL $= 0$ and K_HP(i)=0 and K_BP(i)=0 **then**
LPresult:=<LPresult,<Z|wo|Q|K_LP>>:
CountLP:=CountLP+1:
end if % Compute all Bandstop filter results

if FL $= 0$ and K_BP(i)=0 and K_HP(i)<>0 and K_LP(i)<>0 **then**
BSresult:=<BSresult,<Z|wo|Q|K_HP|K_LP>>:
CountBS:=CountBS+1:
end if

% Compute all Gain Equalizer filter results
if FL $= 0$ and K_LP(i)=K_HP(i) and K_BP(i)<>0 and K_LP(i)<>0 **then**
GE_APresult:=<GE_APresult,<Z|wo|Q|Qz|K_LP>>:
CountGE_AP:=CountGE_AP+1:
end if

to bulk capacitance, C_{db} is the drain to bulk capacitance and R_s is the internal source resistance). Note that we assume the bulk of the NMOS transistors is connected to ground.

The circuit was designed in a 65-nm CMOS process to achieve a group delay of 50 ps, with pole/zero at $|\omega_{o,z}| = 2\pi \times$ 10 GHz. The filter quality factor was set to $Q = 0.6 > 1/\sqrt{3}$ to introduce a small peak in the delay response and thus extend the delay bandwidth. The aspect ratios of $M_{1,2}$ were selected to be 32 μm/60 nm. Resistors R_1 and R_L were implemented using *rppoly_rf* and their values were 400 and 50 Ω, respectively. The capacitor $C_5 = 500$ fF was implemented using a metal–insulator–metal (MIM) capacitor while the inductor $L_5 = 461$ nH was selected form the standard design kit with a quality factor of 15.3 at 7 GHz. Fig. 4(b) shows the circuit layout which occupies an area of 0.0529 mm^2. At $V_b = 1.2$ V, the circuit consumes 3.2 mA from a 1.2-V supply. The postlayout simulated gain, phase, and delay responses of the circuit are compared to the theoretical results in Fig. 5 showing very good agreement. Simulations show that the delay response achieves a flat delay of approximately 49 ps with a 10% bandwidth of 9.77 GHz.

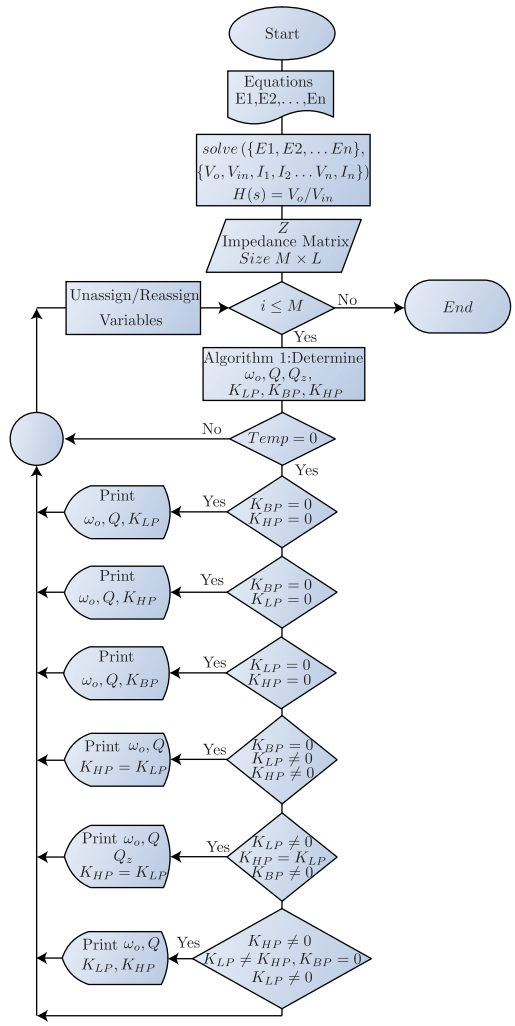

Fig. 3. Flowchart of the filter synthesis procedure.

B. Common-Source APF Design Example

In [15], we used similar design steps to investigate the common-source filter topology while focusing only on APFs. A total of 180 APFs were found and the operation of some filters was verified with measurements and simulation results. A selected circuit [see Fig. 6(a)] with tunable peak delay is designed and fabricated in a 65-nm CMOS process as a proof of concept, particularly, with regards to the very high operating frequency. Neglecting the circuit parasitics, the transfer function of this filter is given by

$$H_{\mathrm{APF}}(s) = -\frac{s^2 - \frac{g_m}{C_3}s + \frac{1}{L_3C_3}}{s^2 + \frac{1}{R_LC_3}s + \frac{1}{L_3C_3}} \tag{13}$$

from which it is seen that the filter has a pole frequency $\omega_o = 1/(L_3C_3)^{1/2}$, pole quality factor $Q = R_L(C_3/L_3)^{1/2}$ and zero quality factor $Q_z = -(1/g_m)(C_3/L_3)^{1/2}$. In [15], we provided comprehensive analysis for the all-pass circuit including nonidealities, noise figure, input, and output impedances. The component values used were $L_3 = 84$ pH with a quality factor of 30.9 at 31 GHz and $C_3 = 265.5$ fF. The current source I_b was implemented with NMOS transistor and a dc bias voltage V_b while the load resistors R_L were implemented as active

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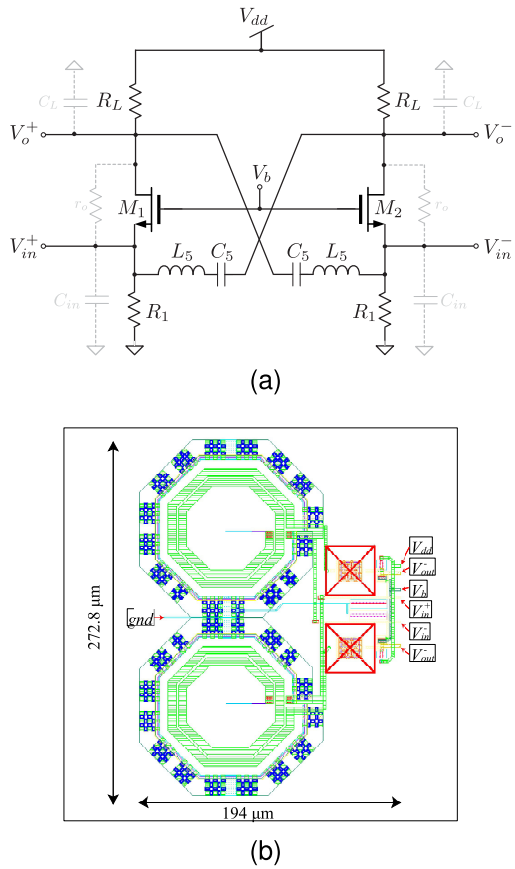

Fig. 4. AP1 circuit. (a) Schematic along with the transistor parasitics and (b) layout.

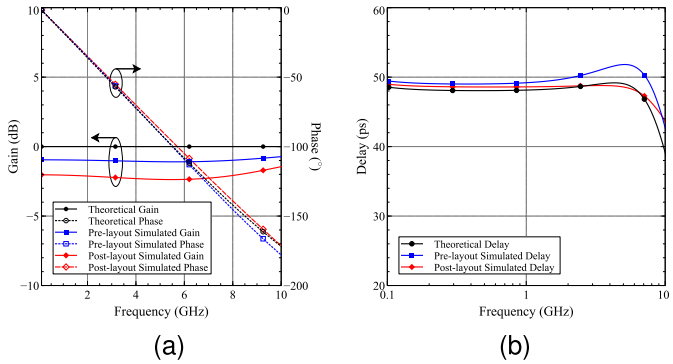

Fig. 5. Postlayout simulation results of AP1 circuit. (a) Gain and phase responses. (b) Delay response of AP1 circuit.

resistors with PMOS transistors and a dc bias voltage V_c. The circuit was tested with 50-GHz ZPROBE 150-μm pitch GSGSG wafer probes on a Rohde & Schwarz ZVA67 4Ports vector analyzer. The measured phase and gain responses are provided in Fig. 7(a) compared to postlayout simulation results.[2] The gain error is less than 1 dB up to 20 GHz and is 6.3 dB at 31 GHz, which is expected at resonance due to the nonideal behavior of the on-chip inductors. Fig. 7(b) shows the delay response of the circuit where the peak delay of 88.4 ps at 31 GHz is less than the postlayout simulated value of 96 ps at 32.8 GHz. The measured value of delay Q-factor (Q_D) is

[2] RC parasitics extraction was done using the *Assura* tool.

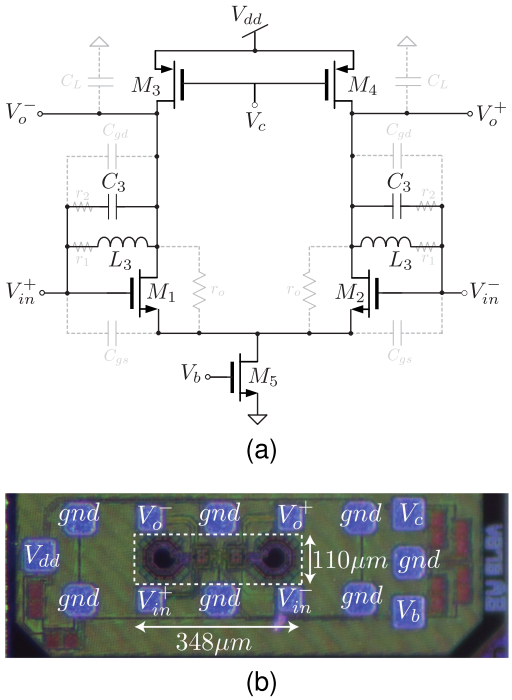

Fig. 6. a) Schematic of a selected APF along with major devices parasitics. (b) Microphotograph of the fabricated filter [15].

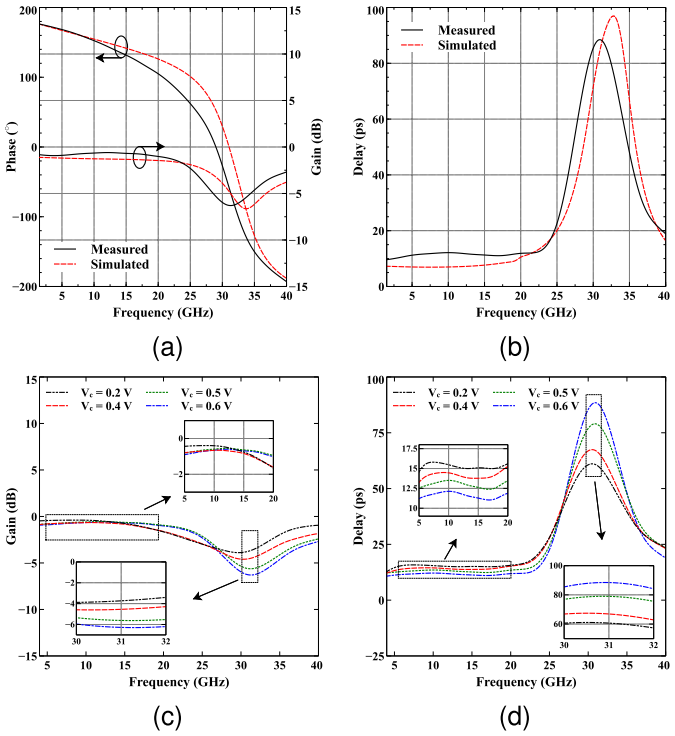

Fig. 7. Simulated versus measured (a) gain and phase responses and (b) delay response of filter APF1. Measured response of filter APF1 for different control voltage V_c values demonstrating the tunability of (c) gain and (d) delay [15].

3.74 compared to the 4.63 of the postlayout simulated value. Fig. 7(c) and (d) shows the measured magnitude and delay responses, respectively, for different values of V_c which results in different Q values as expected. These results confirm the wideband operation from 5 to 20 GHz with a flat delay slightly varying from 11 to 15 ps and the narrowband operation from

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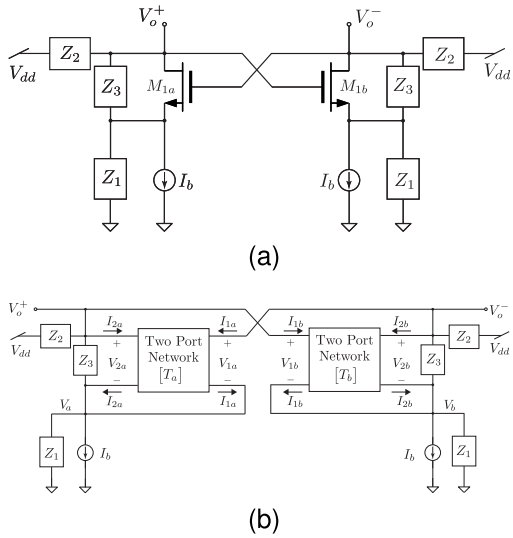

Fig. 8. Schematic of (a) differential oscillator structure with cross-coupled transistors and (b) its two-port network representation used in the symbolic analysis [37].

30 to 32 GHz with delay varying between 60 and 88 ps. This filter achieves the highest Q_D value of any published second-order all-pass known to the authors and is a direct result of the automated search process.

C. Oscillator Design Example

We used symbolic math tools to investigate many new oscillator circuits in previous works [37], [42]–[44]. In [44], we experimentally verified the operation of a new quadrature-phase oscillator family based on two cross-coupled differential pair cells.

In this section, the work in [37] is used as the basis for demonstration of the synthesis steps mentioned above in oscillator design. Our target is to obtain differential oscillators and we adopt a cross-coupled transistor pair cell. We select an impedance network formed of six impedances symmetrically distributed around the cross-coupled transistor pair in order to ensure a balanced structure, as shown in Fig. 8. Note that the dc current I_b ensures proper biasing but it may not be required depending on the nature of Z_1. Referring to step 4 of the design process, we provide in Table IV a list of the possible impedance combinations that do not hinder dc biasing of the transistors. We then derive the following set of nodal and mesh equations for the circuit in Fig. 8(b):

$$0 = \frac{\left(V_{\text{in}}^{+} - V_o^{+}\right)}{Z_2} + \frac{\left(V_a - V_o^{+}\right)}{Z_3} - I_{2a} - I_{1b} \quad (14a)$$

$$0 = \frac{\left(V_{\text{in}}^{-} - V_o^{-}\right)}{Z_2} + \frac{\left(V_b - V_o^{-}\right)}{Z_3} - I_{2b} - I_{1a} \quad (14b)$$

$$0 = \frac{\left(V_o^{+} - V_a\right)}{Z_3} + \frac{(0 - V_a)}{Z_1} + I_{1a} + I_{2a} \quad (14c)$$

$$0 = \frac{\left(V_o^{-} - V_b\right)}{Z_3} + \frac{(0 - V_b)}{Z_1} + I_{1b} + I_{2b} \quad (14d)$$

$$V_o^{+} = V_a + V_{2a},\ \ V_o^{-} = V_a + V_{1a} \quad (14e)$$

$$V_o^{+} = V_b + V_{1b},\ \ V_o^{-} = V_b + V_{2b} \quad (14f)$$

Algorithm 4 Algorithm for Computing the Characteristic Equation of the Differential Oscillator Structure

Input T-matrix from equations:
a11:=0: a12:=-1/gm: a21:=0: a22:=0:
b11:=a11: b12:=a12: b21:=a21: b22:=a22:
Input impedance matrix Z from Table I:
Zz1:=<row #1 from Table I>:
Zz2:=<row #2 from Table I>:
Zz3:=<row #3 from Table I>:
Input nodal and mesh equations:
Eqs={(14a)-(14h)}
output: The characteristic equation
1: **for** $i = 1 : m$ **do**
2: $Z_1 = Z[i, 1]$
3: $Z_2 = Z[i, 2]$
4: $Z_3 = Z[i, 3]$
% Solve for the variables
5: soln=solve({Eqs},{V_o^+, V_o^-, I_{1a}, I_{2a}, V_{1a}, V_{2a}, V_{1b}, V_{2b}, I_{1b}, I_{2b}, V_{in}^+, V_{in}^-, V_a, V_b}):
% Assign the variables
6: assign(soln):
% Compute the characteristic equation
7: $T(s)_i$ =($V_o^+ - V_o^-$)/($V_{in}^+ - V_{in}^-$):
8: **end for**

Remark 2. Note V_{in}^+ and V_{in}^- are V_{dd} nodes and they are used in deriving the characteristic equation. Note that $n = 3$ while m depends on the selected impedances to be included in the analysis from the combinations in Table IV.

TABLE IV
TABLE OF POSSIBLE IMPEDANCE COMBINATIONS USED ON THE OSCILLATOR DESIGN EXAMPLE

Impedance	Possibilities
Z_1	R_1, C_1, L_1, $R_1//C_1$, $R_1 + C_1$, $L_1 + C_1$, $L_1//C_1$
Z_2	R_2, C_2, L_2, $R_2//C_2$, $L_2 + C_2$, $L_2//C_2$
Z_3	R_3, C_3, L_2, $R_3//C_3$, $L_3 + C_3$

$$V_{1a} = a_{11}V_{2a} - a_{12}I_{2a},\ \ V_{1b} = b_{11}V_{2b} - b_{12}I_{2b} \quad (14g)$$

$$I_{1a} = a_{21}V_{2a} - a_{22}I_{2a},\ \ I_{1b} = b_{21}V_{2b} - b_{22}I_{2b}. \quad (14h)$$

Algorithms 4 is used to symbolically obtain the oscillator's characteristic equation as

$$Z_1 + Z_2 + Z_3 + g_m Z_3(Z_1 - Z_2) = 0 \quad (15)$$

using the transmission matrix in (3a). Note that we assumed here again that the two transistors are identical and hence, they have the same transmission matrix. This is, however, not a necessary assumption [42]. It is worth mentioning that the above characteristic equation is unique and capable of generating differential oscillators that are not possible to obtain from a Colpitts oscillator, for example. Algorithm 5 is used to find out all the possible oscillators and calculate the startup condition and oscillation frequency. A total of ten differential oscillator circuits are obtained and are listed in Table V. The theoretical startup value of g_m and oscillation frequency ω_o are also given in Table V. Half of these circuits are LC-based oscillators and the other half are RC-based ones.

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Algorithm 5 Algorithm to Find All Possible Oscillators, Their Oscillation Frequencies and Startup Conditions

Input: The characteristic equations from 4
Outputs: ω_o and the start-up value of g_m
Initialization: $FL = 0$ % temporary variable acting as a flag
1: **for** $i = 1 : m$ **do**
% find $Ts(i)$ order
2: TOrder(i)=degree(denom(i),s)+degree(numer(i),s)
% Determine the coefficients of the denominator of H(s)
3: a(i)=coeff(denom,s,2)
4: b(i)=coeff(denom,s,1)
5: c(i)=coeff(denom,s,0)
6: **if** a(i)=0 or b(i)=0 or c(i)=0 or TOrder(i)>=5 **then**
7: $FL = 1$
8: a(i)=1, b(i)=1, c(i)=1 % Invalidate the results
9: **end if**
% Start of computations for ω_o
10: wo(i)=sqrt(c(i)/a(i));
% Determine the start-up value of g_m
11: B(i):=simplify(b(i)/a(i));
12: solve(B(i)=0,{gm});
13: test:=coulditbe(gm>0) assuming positive;
14: **if** test=true **then**
% Store and print results
15: Osc_result:=<<Z_select|wo|gm>>:
16: Print(Osc_result) %results are presented in Table V
17: **end if**
18: **end for**

TABLE V
TEN DIFFERENTIAL OSCILLATORS POSSIBLE FROM FIG. 8

Z_1, Z_2, Z_3	$\omega_o =$	$g_m =$
R_1, L_2, C_3	$\frac{\sqrt{1+(R_1^2C_3/L_2)}}{\sqrt{L_2C_3}}$	$\frac{R_1C_3}{L_2}$
$R_1, L_2, R_3//C_3$	$\frac{\sqrt{1+\frac{2R_1}{R_3}+\frac{R_1^2C_3}{L_2}}}{\sqrt{L_2C_3}}$	$\frac{1}{R_3}+\frac{R_1C_3}{L_2}$
$R_1, L_2//C_2, R_3$	$\frac{1}{\sqrt{L_2C_2}}$	$\frac{1}{R_3}$
C_1, R_2, C_3	$\frac{\sqrt{1+(C_1/C_3)}}{R_2C_1}$	$\frac{1+\frac{C_3}{C_1}}{R_2}$
$C_1, R_2, R_3//C_3$	$\frac{\sqrt{2+\frac{R_3}{R_2}(1+\frac{C_3}{C_1})}}{\sqrt{R_2R_3C_1C_3}}$	$\frac{1+\frac{R_2}{R_3}+\frac{C_3}{C_1}}{R_2}$
$C_1, R_2//C_2, R_3$	$\frac{\sqrt{\frac{2+(R_3/R_2)}{1-(C_2/C_1)}}}{\sqrt{R_2R_3C_1C_2}}$	$\frac{1+\frac{R_2}{R_3}+\frac{C_2R_2}{C_1R_3}}{R_2(1-\frac{C_2}{C_1})}$
$C_1, R_2//C_2, C_3$	$\frac{1/R_2C_2}{\sqrt{\left(\frac{C_1}{C_2}-1\right)\left(1+\frac{C_1C_3/C_2}{C_1+C_3}\right)}}$	$\frac{1+\frac{C_3}{C_1}}{R_2(1-\frac{C_2}{C_1})}$
$L_1, L_2, R_3//C_3$	$\frac{1}{\sqrt{(L_1+L_2)C_3}}$	$\frac{L_1+L_2}{R_3(L_2-L_1)}$
R_1+C_1, R_2, C_3	$\frac{1}{C_1\sqrt{\frac{C_1C_3}{C_1+C_3}(R_2^2-R_1^2)}}$	$\frac{C_1+C_3}{C_1(R_2-R_1)}$
L_1+C_1, R_2, R_3	$\frac{1}{\sqrt{L_1C_1}}$	$\frac{R_2+R_3}{R_2R_3}$

There are only two canonical members in the ten oscillators. We restricted our search space to second-order oscillators with a maximum of four resistors.

For verification, the LC oscillator circuit shown in Fig. 9(a) obtained from the last row of Table V was designed to oscillate at 27 MHz with $C_1 = 220$ pF, $L_1 = 0.15$ μH, $R_2 = 1$ kΩ and $R_3 = 3$ kΩ. The experimental results are shown in Fig. 9(b)

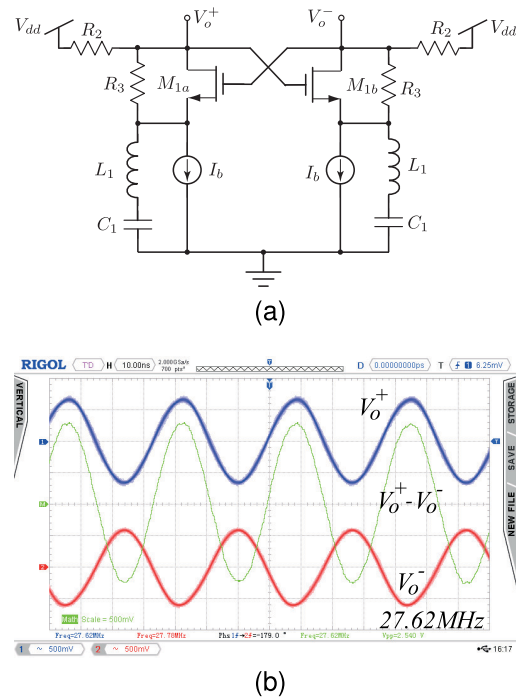

Fig. 9. Designed LC oscillator from row 10 of Table V. (a) Schematic and (b) experimental results using discrete components (Y-axis: 500 mV/div) [37].

where the measured oscillation frequency is 27.62 MHz with a differential output amplitude of $2.54V_{\text{pp}}$ obtained from a discrete realization using BS170 NMOS transistors biased from $V_{\text{dd}} = 5$ V and with $I_b = 5$ mA.

D. Amplifier Analysis Example

In Sections IV-A–IV-C, the focus on the synthesis of new circuits was clear. Here, we provide an example where the focus is more toward the analysis of a well-known circuit; a common-gate amplifier. The structure of this amplifier is depicted in Fig. 10 where the transistor is represented by a two-port network surrounded by three impedances in addition to a source impedance. The governing equations of this structure can be shown to be

$$-I_1 = I_2 + \frac{(V_{\text{in}} - V_x)}{Z_s} + \frac{(0 - V_x)}{Z_1} \tag{16a}$$

$$+\frac{(V_o - V_x)}{Z_2} \tag{16b}$$

$$I_2 = \frac{(V_x - V_o)}{Z_2} + \frac{(0 - V_o)}{Z_3} \tag{16c}$$

$$V_o = V_x + V_2 \tag{16d}$$

$$0 = V_x + V_1 \tag{16e}$$

$$V_1 = a_{11}V_2 - a_{12}I_2 \tag{16f}$$

$$I_1 = a_{21}V_2 - a_{22}I_2. \tag{16g}$$

With symbolic math, the amplifier voltage gain transfer function $H(s) = (V_o/V_{\text{in}})$ is possible to obtain in the general form of

$$H(s) = \frac{a_{12} + Z_2(a_{11} - 1)}{D_1 + D_2 + D_3 + D_4} \tag{17}$$

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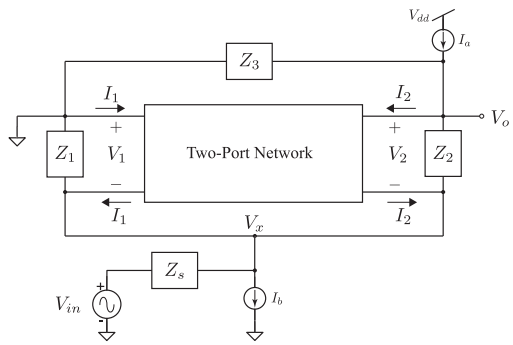

Fig. 10. Common-gate single-ended amplifier.

where

$$D_1 = a_{11}Z_2\left(1 + \frac{Z_s}{Z_1} + \frac{Z_s}{Z_3}\right) \tag{18a}$$

$$D_2 = a_{12}\left(1 + \frac{Z_s}{Z_1} + \frac{Z_s}{Z_3} + \frac{Z_2}{Z_3} + \frac{Z_2Z_s}{Z_1Z_3}\right) \tag{18b}$$

$$D_3 = a_{22}Z_s\left(1 + \frac{Z_2}{Z_3}\right) \tag{18c}$$

$$D_4 = Z_sZ_2\left(a_{21} - \frac{a_{11}a_{22}}{Z_3} + \frac{a_{12}a_{21}}{Z_3} - \frac{1}{Z_3}\right) \tag{18d}$$

which if (3a) is used reduces to

$$H(s) = \frac{(1 + g_mR_L)}{1 + \frac{R_L}{Z_3}(1 + g_mR_s) + R_s\left(\frac{1}{Z_3} + \frac{1}{Z_1} + \frac{R_L}{Z_1Z_3}\right)} \tag{19}$$

after setting $Z_2 = R_L$ and $Z_s = R_s$.

V. Conclusion

There is always a growing demand for new analog circuits to meet the challenges of emerging technologies, especially in communication systems. Traditional methods for synthesizing analog circuits rely on considerable designer experience and automated alternative methods are the way forward in the future. This article provides a design process for synthesizing analog circuits using the two-port network modeling technique and available symbolic math toolboxes. In the last few years, this methodology has succeeded in systematically discovering hundreds of new circuits most of which were never known before. It is up to the analog designers to restrict the search space in order to select the optimum circuits for their desired applications. This can be easily done in the algorithms by restricting the choice of impedances (e.g., inductor-less circuits and canonical minimum component circuits) or by restricting the order of the found circuits to being second-order or third-order for example. As a future work direction, the automation of step 5 in the design process will enable the node/mesh equations to be found directly from a given circuit schematic.

References

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2017.

[2] B. Razavi, *RF Microelectronics*, 2nd ed. London, U.K.: Pearson, 2012.

[3] Y. Yin, B. Ustundag, K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "Wideband 23.5–29.5-GHz phased arrays for multistandard 5G applications and carrier aggregation," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 1, pp. 235–247, Jan. 2021.

[4] C. Wijenayake, Y. Xu, A. Madanayake, L. Belostotski, and L. T. Bruton, "RF analog beamforming fan filters using CMOS all-pass time delay approximations," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 5, pp. 1061–1073, May 2012.

[5] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A low-cost scalable 32-element 28-GHz phased array transceiver for 5G communication links based on a 2×2 beamformer flip-chip unit cell," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, Jan. 2018.

[6] S. M. Perera *et al.*, "Wideband N-beam arrays using low-complexity algorithms and mixed-signal integrated circuits," *IEEE J. Sel. Topics Signal Process.*, vol. 12, no. 2, pp. 368–382, May 2018.

[7] B. Ustundag, K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A wideband high-power multi-standard 23–31 GHz 2×2 quad beamformer chip in SiGe with >15 dBm OP1dB per channel," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 60–63.

[8] P. Ahmadi, B. Maundy, A. S. Elwakil, L. Belostotski, and A. Madanayake, "A new second-order all-pass filter in 130-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 3, pp. 249–253, Mar. 2016.

[9] M. H. Ghazizadeh and A. Medi, "A 125-ps 8–18-GHz CMOS integrated delay circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 1, pp. 162–173, Jan. 2019.

[10] S. K. Garakoui, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "Compact cascadable gm-C all-pass true time delay cell with reduced delay variation over frequency," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 693–703, Mar. 2015.

[11] M. B. Elamien, B. J. Maundy, L. Belostotski, and A. S. Elwakil, "Single-transistor second-order allpass filters," in *Proc. IEEE 62nd Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2019, pp. 369–372.

[12] P. Ahmadi, M. H. Taghavi, L. Belostotski, and A. Madanayake, "A 0.13-μm CMOS current-mode all-pass filter for multi-GHz operation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 12, pp. 2813–2818, Dec. 2015.

[13] M. B. Elamien, B. J. Maundy, L. Belostotski, A. S. Elwakil, and S. A. Mahmoud, "A wideband delay-tunable fully differential allpass filter in 65-nm CMOS technology," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2019, pp. 1–5.

[14] M. B. Elamien, A. S. Elwakil, B. J. Maundy, and L. Belostotski, "8-GHz low-power voltage-mode second-order allpass filter in 65-nm CMOS," in *Proc. 26th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Nov. 2019, pp. 146–149.

[15] M. B. Elamien, B. J. Maundy, L. Belostotski, and A. S. Elwakil, "Synthesis of wideband high-quality factor delay-tunable fully differential all-pass filters," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 10, pp. 4348–4360, Oct. 2020.

[16] I. Mondal and N. Krishnapura, "A 2-GHz bandwidth, 0.25–1.7 ns true-time-delay element using a variable-order all-pass filter architecture in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2180–2193, Aug. 2017.

[17] M. B. Elamien, B. J. Maundy, L. Belostotski, and A. S. Elwakil, "An ultra-low power wide-band single-transistor second-order allpass filter in 65 nm CMOS," in *Proc. IEEE 62nd Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2019, pp. 373–376.

[18] B. J. Maundy, A. S. Elwakil, L. Belostotski, and N. Herencsar, "Single transistor RC-only second-order allpass filters," *Int. J. Circuit Theory Appl.*, vol. 48, no. 2, pp. 162–169, Feb. 2020.

[19] S. R. Aghazadeh, H. Martinez, A. Saberkari, and E. Alarcon, "Tunable active inductor-based second-order all-pass filter as a time delay cell for multi-GHz operation," *Circuits, Syst., Signal Process.*, vol. 38, no. 8, pp. 3644–3660, Aug. 2019.

[20] M. B. Elamien, B. J. Maundy, L. Belostotski, and A. S. Elwakil, "Wideband third-order single-transistor all-pass filter," *Int. J. Circuit Theory Appl.*, vol. 48, no. 7, pp. 1201–1208, Jul. 2020.

[21] P. J. Osuch and T. Stander, "A millimeter-wave second-order all-pass delay network in BiCMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 10, pp. 912–914, Oct. 2018.

[22] D. Shahhosseini, E. Zailer, L. Behjat, and L. Belostotski, "Method of generating unique elementary circuit topologies," *Can. J. Elect. Comput. Eng.*, vol. 41, no. 3, pp. 118–132, 2018.

[23] B. A. A. Antao, "Trends in CAD of analog ICs," *IEEE Circuits Devices Mag.*, vol. 12, no. 5, pp. 31–41, Sep. 1996.

Authorized licensed use limited to: UNIVERSITY OF SHARJAH. Downloaded on October 30,2022 at 10:20:56 UTC from IEEE Xplore. Restrictions apply.

[24] W. Daems, G. Gielen, and W. Sansen, "Simulation-based generation of posynomial performance models for the sizing of analog integrated circuits," *IEEE Trans. Comput.-Aided Design Integr.*, vol. 22, no. 5, pp. 517–534, May 2003.

[25] P. C. Maulik, L. R. Carley, and D. J. Allstot, "Sizing of cell-level analog circuits using constrained optimization techniques," *IEEE J. Solid-State Circuits*, vol. 28, no. 3, pp. 233–241, Mar. 1993.

[26] S. K. Gupta and M. M. Hasan, "KANSYS: A CAD tool for analog circuit synthesis," in *Proc. 9th Int. Conf. VLSI Design*, 1996, pp. 333–334.

[27] G. G. E. Gielen, "CAD tools for embedded analogue circuits in mixed-signal integrated systems on chip," *IEE Proc.-Comput. Digit. Techn.*, vol. 152, no. 3, pp. 317–332, May 2005.

[28] J. R. Koza, F. H. Bennett, D. Andre, M. A. Keane, and F. Dunlap, "Automated synthesis of analog electrical circuits by means of genetic programming," *IEEE Trans. Evol. Comput.*, vol. 1, no. 2, pp. 109–128, Jul. 1997.

[29] G. G. E. Gielen and R. A. Rutenbar, "Computer-aided design of analog and mixed-signal integrated circuits," *Proc. IEEE*, vol. 88, no. 12, pp. 1825–1854, Dec. 2000.

[30] B. Nayak, B. Misra, and T. R. Choudhury, "Meta-heuristic optimization algorithms for design of gain constrained state variable filter," *AEU-Int. J. Electron. Commun.*, vol. 93, pp. 7–18, Sep. 2018.

[31] P. Lalbakhsh, B. Zaeri, and A. Lalbakhsh, "An improved model of ant colony optimization using a novel pheromone update strategy," *IEICE Trans. Inf. Syst.*, vol. 96, no. 11, pp. 2309–2318, 2013.

[32] H. Tang, H. Zhang, and A. Doboli, "Refinement-based synthesis of continuous-time analog filters through successive domain pruning, plateau search, and adaptive sampling," *IEEE Trans. Comput.-Aided Design Integr.*, vol. 25, no. 8, pp. 1421–1440, Aug. 2006.

[33] A. S. Elwakil and B. J. Maundy, "Single transistor active filters: What is possible and what is not," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 9, pp. 2517–2524, Sep. 2014.

[34] B. J. Maundy, A. S. Elwakil, and L. Belostotski, "Automatic generation of differential-input differential-output second-order filters based on a differential pair," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 39, no. 6, pp. 1258–1271, Jun. 2020.

[35] B. J. Maundy, A. S. Elwakil, and S. J. G. Gift, "On a class of cross coupled fully differential filters," *Int. J. Circuit Theory Appl.*, vol. 44, no. 7, pp. 1425–1436, Jul. 2016.

[36] B. J. Maundy, A. S. Elwakil, S. Ozoguz, and H. A. Yildiz, "Minimal two-transistor multifunction filter design," *Int. J. Circuit Theory Appl.*, vol. 45, no. 11, pp. 1449–1466, Nov. 2017.

[37] B. J. Maundy, A. S. Elwakil, M. B. Elamien, and A. Al-Hammadi, "Synthesis of a family of differential cross-coupled oscillators and design application," in *Proc. IEEE 61st Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2018, pp. 13–16.

[38] A. S. Elwakil and B. Maundy, "On the two-port network analysis of common amplifier topologies," *Int. J. Circuit Theory Appl.*, vol. 38, no. 10, pp. 1087–1100, Dec. 2010.

[39] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*. New York, NY, USA: Oxford Univ. Press, 2016.

[40] C. K. Alexander, N. O. Matthew, and M. Sadiku, *Fundamentals of Electric Circuits*. New York, NY, USA: McGraw-Hill, 2009.

[41] R. C. Jaeger and T. N. Blalock, *Microelectronic Circuit Design*. New York, NY, USA: McGraw-Hill, 2003.

[42] A. S. Elwakil, "Design of non-balanced cross-coupled oscillators with no matching requirements," *IET Circuits, Devices Syst.*, vol. 4, no. 5, p. 365, 2010.

[43] A. S. Elwakil, "On the two-port network classification of Colpitts oscillators," *IET Circuits, Devices Syst.*, vol. 3, no. 5, pp. 223–232, Oct. 2009.

[44] M. B. Elamien, B. J. Maundy, L. Belostotski, and A. S. Elwakil, "On chip 0.5 V 2 GHz four-output quadrature-phase oscillator," *AEU-Int. J. Electron. Commun.*, vol. 126, Nov. 2020, Art. no. 153393.

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