Jetson Nano Interface Tuning and Compliance Guide

Application Note

DA-09704-001_v1.2 | April 2022

Document History

DA-09704-001_v1.2

Version	Date	Description of Change
1.0	October 16, 2019	Initial Release
1.1	April 29, 2020	• Added new chapter, "Jetson Nano Ethernet Compliance Test Guide" • Added an attachment for Realtek Linux Waveform tool
1.2	April 20, 2022	• Minor addition to the "PCIe Compliance Testing" section • Added two file attachments

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Jetson Nano USB2.0 Tuning Guide

This chapter describes the registers and steps needed to tune the USB2.0 high speed eye diagram for NVIDIA® Jetson Nano™. NVIDIA typically uses Tektronix oscilloscopes; however, customers are free to use oscilloscopes from other vendors when performing the USB characterization. Refer to the vendor's website for complete test specification and instructions for high-speed host and device mode testing.

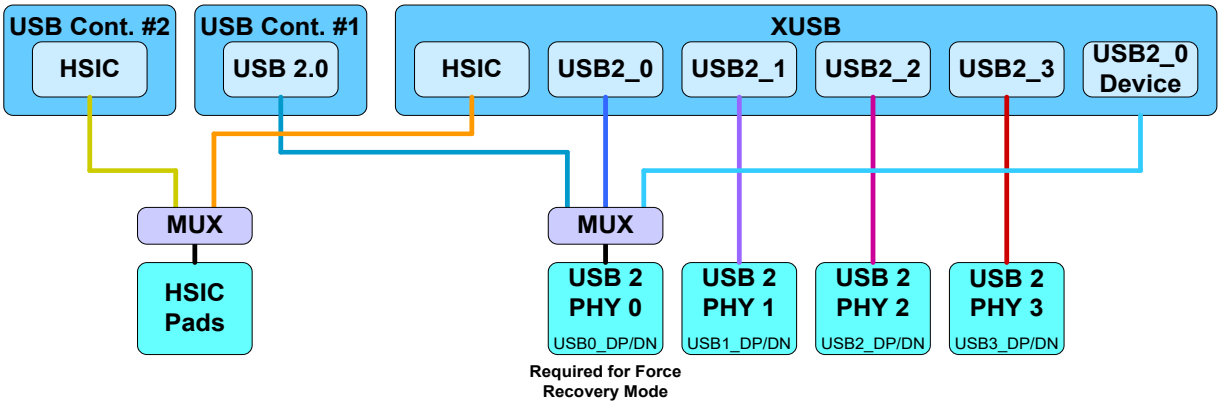
Required Equipment

- Tektronix TDS694C or faster digital sampling oscilloscope
- Tektronix P6247 or P6248 or equivalent differential probe * 1
- High-speed USB Electrical Test Fixture
- Oscilloscope USB test Software
- Tool to access register/memory space in NVIDIA system on chip (SoC) or build a special image to force USB Test mode enabled

Registers for Host Mode Testing

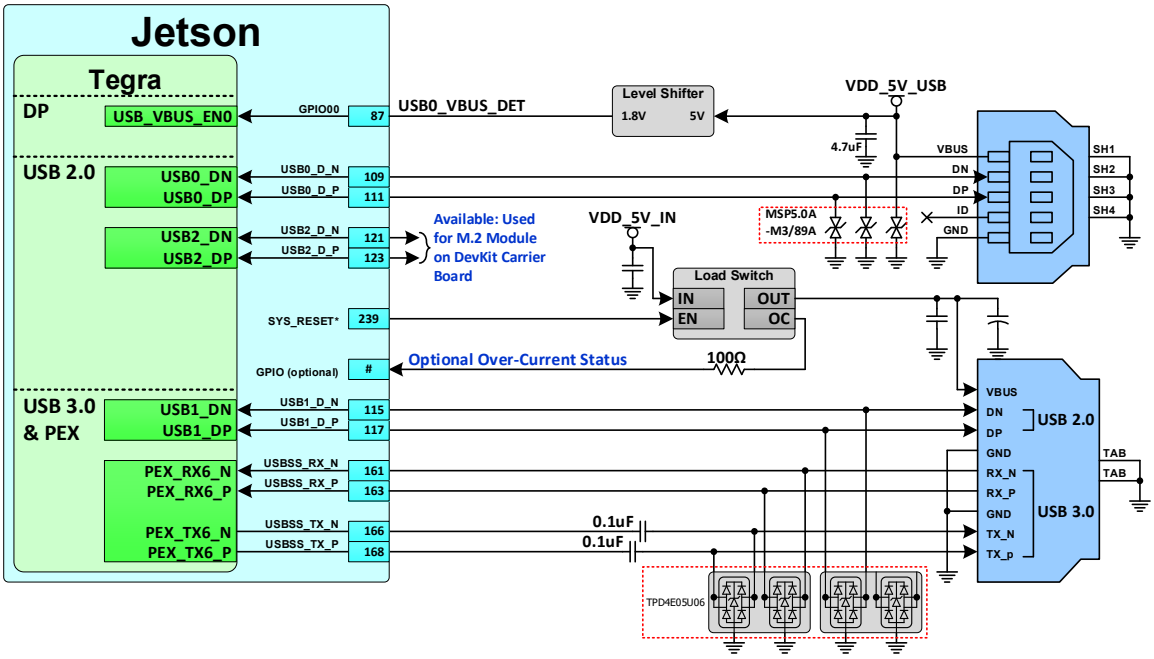
Figure 1 shows the USB2.0 PHY and HSIC multiplexing options.

Figure 1. Jetson Nano Controllers and Interfaces Routing Map



Note: For Jetson Nano, USB0_DP/DN routing comes from xUSB Controller only.

Figure 2. Jetson Nano Connection Example



Toggle the Jetson Nano USB registers listed in Table 1 to force Test J, Test K, Test SE0 NAK, and test packet on USB2.0 ports from the xUSB controller.

Table 1. xUSB USB2.0 Port Test Control Registers

Description	Register Name and Setting
Normal operations	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] =0000b
Test J	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] =0001b
Test K	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] =0010b
Test SE0 NAK	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] =0011b
HS Test packet	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] =0100b
Force enable	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] =0101b

Test Mode Programming Sequence

The programming sequence for enabling USB2.0 test mode is as follows:

1. Connect any USB device to the port (this will prevent the controller from entering power down mode).

Note: "Any USB device" refers to any real device, such as HS uDISK or LS mouse.

2. Disable the auto-suspend for the controllers:

   echo on > /sys/bus/usb/devices/usb1/power/control

   echo on > /sys/bus/usb/devices/usb2/power/control

   echo on > /sys/bus/usb/devices/usb3/power/control

3. Set PP (Port Power) in Disabled state by XUSB_XHCI_OP_PORTSC* bit [9] = 0.

   USB0: 0x70090460: XUSB_XHCI_OP_PORTSC_4

   USB1: 0x70090470: XUSB_XHCI_OP_PORTSC_5

   USB2: 0x70090480: XUSB_XHCI_OP_PORTSC_6

4. Set RS (Run/Stop) bit in the XUSB_XHCI_OP_USBCMD bit [0] = 0.

   0x70090020: XUSB_XHCI_OP_USBCMD

5. Wait for HCHalted (HCH) bit in the XUSB_XHCI_OP_USBSTS bit [0] = 1.

   0x70090024: XUSB_XHCI_OP_USBSTS

6. Set the xUSB USB2.0 Port Test Control Registers in PORTPMSCHS register to enable test patterns (refer to Table 1 for additional information).

   USB0: 0x70090464: XUSB_XHCI_OP_PORTPMSCHS_4

   USB1: 0x70090474: XUSB_XHCI_OP_PORTPMSCHS_5

   USB2: 0x70090484: XUSB_XHCI_OP_PORTPMSCHS_6

Note: Per the USB2.0 Specification, only a single downstream facing port can be in test_mode at any given time.

7. Disable Pad PD (Power Down) by clearing the XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0 bit [27:26] = 0b'00.

   USB0: 0x7009F088: XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0

   USB1: 0x7009F0C8: XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0

   USB2: 0x7009F108: XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0

8. Plug in the test fixture to start USB2.0 eye diagram test.

Note: In Step 3, Step 6, and Step 7, USB0 is USB0_D_P/N (111/109), USB1 is USB1_D_P/N (117/115), and USB2 is USB2_D_P/N (123/121).

Registers to Adjust High Speed USB2.0 Eye Diagram

The following registers are Jetson Nano USB registers that may be needed to tune the USB2.0 eye diagram. Refer to the "Tuning Procedure" section on how to use these registers during characterization.

Table 2. xUSB Registers

Register Name	Bit Fields	Description
XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0: Address 0x7009F088 for USB0, 0x7009F0C8 for USB1, and 0x7009F108 for USB2		
HS_SLEW	8:6	HS slew rate control
HS_CURR_LEVEL	5:0	HS driver output setup control
XUSB_PADCTL_USB2_OTG_PADx_CTL_1_0: Address 0x7009F08C for USB0, 0x7009F0CC for USB1, and 0x7009F10C for USB2		
RPD_CTRL	30:26	RPD_CTRL (15K host pull down)
TERM_RANGE_ADJ	6:3	HS termination control

Register Name	Bit Fields	Description
XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 (device RX testing): Address 0x7009F284		
HS_SQUELCH_LEVEL	2:0	HS SQUELCH control

Note: The USBx is based on the module pin name, so USB0 is USB0_D_P/N (111/109), USB1 is USB1_D_P/N (117/115), and USB2 is USB2_D_P/N (123/121).

Tuning Procedure

During manufacturing chip production, each NVIDIA SoC is calibrated and the fuses corresponding to USB drive strength (HS_CURR_LEVEL), HS termination (TERM_RANGE_ADJ), and 15K host pull down (RPD_CTRL) are burnt on each chip.

Before making any USB measurements, ensure that the values programmed during manufacturing are loaded for HS_CURR_LEVEL, TERM_RANGE_ADJ and RPD_CTRL into the pad configuration inputs.

To find the default values, read from Fuse FUSE_USB_CALIB and Fuse FUSE_USB_CALIB_EXT. See Table 3 for details.

Table 3. FUSE_USB Registers

Register Name	Bit Fields	Description
FUSE_USB_CALIB_0 (Address 0x7000F9F0)		
USB_CALIB	22:17	HS_CURR_LEVEL for USB2
USB_CALIB	16:11	HS_CURR_LEVEL for USB1
USB_CALIB	10:7	TERM_RANGE_ADJ for all USB ports
USB_CALIB	5:0	HS_CURR_LEVEL for USB0
FUSE_USB_CALIB_EXT_0 (Address 0x7000FB50)		
USB_CALIB_EXT	4:0	RPD_CTRL for all USB ports

During the characterization stage, manually adjusting HS_CURR_LEVEL value must be enough to fulfill compliance requirements. It is possible to try and increase termination as a last resort.

Note: NVIDIA does not recommend customers adjusting termination values. Do note that if the TERM_RANGE_ADJ needs to be adjusted, it may result in an impedance mismatch on the board and further attention may be needed.

It must be emphasized that if any HS_CURR_LEVEL modification is needed, it must be done as an offset to the default fused value in order to take into account silicon process differences. Never apply a global overwrite HS_CURR_LEVEL value for all silicon. There is a mechanism provided in software to read fused USB drive strength and add an offset to it. Consult an NVIDIA Software Support Engineer for additional information.

Software Verification

A functional check is recommended. Connect the DUT to USB hosts and devices to perform a check on functionality.

To check if software implements the tuned offset step properly, load new software with offset included into another DUT and check to ensure:

For xUSB:

HS_CURR_LEVEL = USB_CALIB + tuned offset steps

Jetson Nano USB SS Compliance Test Guide

This chapters serves as the high-level guide to compliance testing of the SuperSpeed USB (5 Gbps) PHY in Jetson Nano. The Jetson Nano has been tested for specification compliant and passed under worst case scenarios. Therefore, no tuning will be required if customer designs follow our routing guidelines published in our design guides.

Compliance Testing

The *Electrical Compliance Test Specification for SuperSpeed Universal Serial Bus* Rev 0.79 provides the compliance criteria and test descriptions for SuperSpeed USB devices, hubs, and host controllers that conform to the *Universal Serial Bus 3.0 Specification*, Rev 1.0. Customers should refer to the document for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

Placing Jetson Nano in Compliance Mode

To run the TX electrical compliance test, the Jetson Nano must be placed in compliance mode. Perform the following 2 steps to achieve this.

1. Disable runtime power management for USB Host Controller.
2. Set CTE = 1 in PORTSC.

Note: All occurrences of "L4T Image" refers to the NVIDIA Jetson Linux driver package supporting the Jetson Nano for which compliance testing is being performed.

L4T Image

1. Boot up the DUT (ensure the USB3.0 Host Test Fixture is not connected to the DUT).
2. Install the latest L4T Image.

3. Run the following script to disable power management for USB Host Controller.

```
#!/bin/sh
for hub in $(ls -d /sys/bus/usb/devices/usb?); do
echo on > $hub/power/control
done
```

4. Install the devmem tool by running the following command.

```
$ sudo apt-get install devmem2
```

5. Set CTE = 1 in PORTSC by writing Ah to XUSB_XHCI_OP_PORTSC[8:5].

```
devmem2 0x70090420 w 0x10340  // USB_SS#0
```

Notes:

Jetson Nano contains one USB-SS port. Its PORTSC offsets and pin # is USB_SS#0 from USBSS (pins 161/163/166/168), offset = 0x420

Refer to software release documentation for information on supported mapping configuration.

Writing 0x10340 will change the internal state of XUSB. Therefore, it is not expected to read back the same value.

If devmem2 commands result in a "bus error," try other versions or other register read/write tools.

6. Connect the USB3.0 Host Test Fixture to the DUT and start compliance test.
7. Confirm DUT is in compliance mode by checking XUSB_XHCI_OP_PORTSC[8:5] = Ah

Placing Jetson Nano in Loopback Mode

To run the RX electrical compliance test, Jetson Nano must be placed in loopback mode. To achieve this, disable runtime power management for USB Host Controller.

L4T Image

1. Boot up the DUT (ensure the USB3.0 Host Test Fixture is not connected to the DUT).
2. Install the latest L4T Image.
3. Run the following script to disable power management for USB Host Controller.

```
#!/bin/sh
for hub in $(ls -d /sys/bus/usb/devices/usb?); do
echo on > $hub/power/control
done
```

4. Connect the USB3.0 Host Test Fixture to the DUT and start compliance test.

Equipment Selection for RX Tolerance Tests

NVIDIA SuperSpeed USB PHY RX tolerance tests have been conducted with the Tektronix BERTScope, Agilent JBERT, and LeCroy PeRT3 platforms. During the testing process it was found that the SuperSpeed USB PHY passes with both Tektronix and Agilent equipment but not the LeCroy test setup.

The *Universal Serial Bus 3.0 Specification*, Revision 1.0 defines loopback mode to facilitate RX Jitter Tolerance testing. Entry to loopback mode is achieved by sending a specific sequence of patterns. Error rate tester sets the loopback bit in TS2 ordered sets while training the link for loopback entry sequence. Section 6.8.4.1 of the USB3.0 specification clearly states that during loopback the receiver processes the BERT ordered sets BRST, BDAT, and BERC. However, this sequence is not being followed by many testers. The fundamental assumption with Agilent and LeCroy testers is that loopback mode is immediately entered after TS2 handshake with loopback bit set. However, the XUSB design implemented in Jetson Nano looks for BRST ordered set to complete loopback in compliance with Section 6.8.4.1 of the USB3.0 specification.

Table 4. Loopback Entry + Checking Sequences

Tektronix BERTScope	Agilent JBERT	LeCroy PeRT#
Polling.LFPS	Polling.LFPS	Polling.LFPS
TSEQ	TSEQ	TSEQ
TS1	TS1	TS1
TS2	TS2	TS2
BRST+CP0	COM	COM+D10.2
CP0 error checking	CP0 error checking	CP0 error checking

Different vendors use different sequences. Jetson Nano USB3.0 controller follows the Tektronix sequence for loopback entry and error checking. Tektronix BERTScope introduces BRST for jitter tolerance testing and we can successfully enter loopback without modifications to the sequence. Since the Agilent JBERT and LeCroy PeRT3 testers do not introduce BRST and we consequently fail to start loopback testing because loopback is not achieved.

This incompatibility does not affect USB3.0 functionality in any way.

It is possible to modify the Agilent JBERT sequence to introduce BRST, as shown in Table 5 by inserting a “pause” in the JBERT automation software after COM has been transmitted and manually running BRST sequence before completing the error checking sequence.

Table 5. Modified JBERT Sequence

Agilent JBERT
Polling.LFPS
TSEQ
TS1
TS2
COM
BRST
CP0 error checking

Jetson Nano XUSB loopback sequence is incompatible with this pattern and it puts Jetson Nano PHY into a bad state causing LeCroy PeRT3 to lose sync. It is not possible to transmit a modified sequence to put the Jetson Nano USB3.0 controller back into loopback after the COM+D10.2 pattern because LeCroy PeRT3 is not able to re-sync. Therefore, it is currently not possible to test Jetson Nano SuperSpeed USB PHY receiver using LeCroy PeRT3.

The Jetson Nano SuperSpeed USB PHY passes RX tolerance tests with both Tektronix and Agilent platforms, and therefore, NVIDIA recommends designers use Tektronix or Agilent (with modified sequence) equipment for their testing. The behavior described in this application note is due to a different interpretation of the USB3.0 specification and does not affect USB3.0 operational performance nor does it cause compliance failures. It only affects the sequence required for loopback entry.

Jetson Nano PCIe Compliance Testing Reference

NVIDIA Jetson Nano includes the Peripheral Component Interconnect Express (PCIe) interface. The implementation in Jetson Nano supports both 2.5 G (PCIe Gen1) and 5.0 G (PCIe Gen2) transfer rates.

This chapter describes the test equipment, software, and setup required to run the PCI Express (PCIe) Gen1 and Gen2 electrical compliance tests. Jetson Nano has been tested under worst case scenarios and the hardware can adapt to the compliant devices and channel automatically. The hardware calibrates the termination impedance for both PCIe transmitter and receiver, and the receiver adapts its internal parameters to optimize signal characteristics. The hardware is designed to directly work with compliant devices and compliant channels automatically. Therefore, no tuning will be required if customer designs follow the routing guidelines published in our design guide.

The lane mappings for the configurations are internal to the PCIe root port controller. For the supported configurations, refer to the product design guide for Jetson Nano.

Equipment

The components required to perform PCIe compliance testing include:

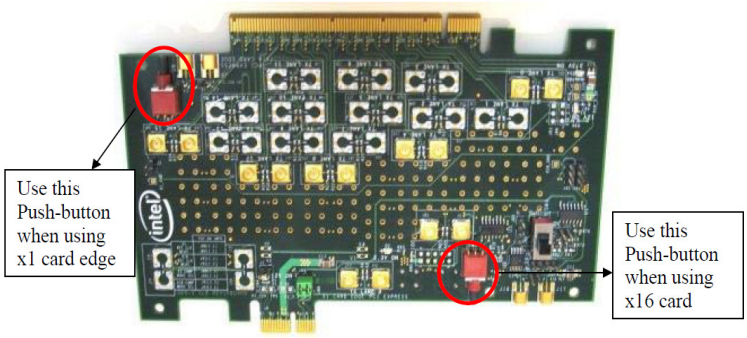
- Test Fixture
- Oscilloscope
- Probe
- Cables
- Termination Load/Adapter
- Software
  - PCI-SIG Clock Jitter Tool
  - SigTest 3.2.0

There are many tools currently available to help with compliance testing. The following sections list some of the equipment available. Items marked with an asterisk (*) indicate equipment that NVIDIA has used in its testing.

Test Fixtures

Test fixtures are used to connect the probes to the TX pins of the PCIe interface. Fixtures of different interface types are available and are recommended as opposed to using adapters to convert the interface type. Whichever fixture is selected, it must have SMP interconnects to avoid impedance mismatches due to discontinuities.

Table 6. Partial List of PCIe Test Fixtures

Product	Image and Description
PCIe Gen2 CLB v2 (for desktop CEM) See Notes	

Notes:
CLB is Revision 2.0 Compliance Board.
There are two different versions of CLB:

- x1/x16 which has x1 and x16 card edges for testing x1 and x16 motherboard slots
- x4/x8 which has x4 and x8 card edges for testing x4 and x8 motherboard slots

The compliance load board (CLB) version(s) needed for testing a motherboard depend on the slot widths on the motherboard. All slots on the motherboard must be tested. Ordering information for the CLB can be found on PCI-SIG website at: http://pcisig.com/pci-express-compliance-load-board-clb

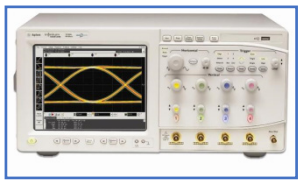
Oscilloscope

An oscilloscope is used to measure the signals.

PCIe Gen1

For PCIe Gen1, the PCIe specification requires that the oscilloscope have at least 6 GHz of bandwidth.

Table 7. Partial List of Instruments for PCIe Gen1

Company	Product	Image and Description
Tektronix*	TDS6604B or better	
Agilent	DSO/DSA91304A or better	

PCIe Gen2

For PCIe Gen2, the PCIe specification requires that the oscilloscope have at least 12 GHz of bandwidth.

Table 8. Partial List of Instruments for PCIe Gen2

Company	Product	Image and Description
Tektronix*	DSA71254 or better	
Agilent	DSO81304B or better	

Probes

Probes are used to connect the oscilloscope to the test fixture; oscilloscope probes must be a minimum of 8 GHz of bandwidth.

Table 9. Partial List of Probes

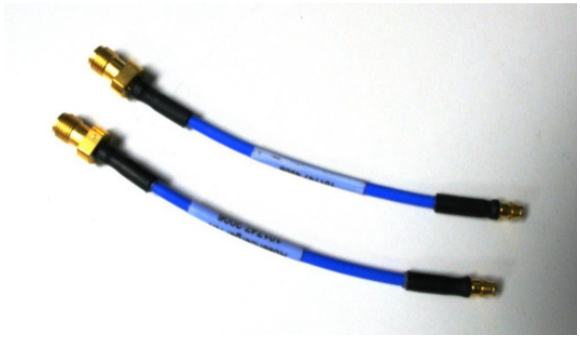
Company	Product	Image and Description
Tektronix*	1169A Requires Agilent N5380A	

Cables

Cables are used to measure signal quality.

Table 10. Partial List of Cables

Company	Product	Image and Description
Tektronix*	174-4944-xx Two pairs of matched SMA-SMA cables (skew <1ps)	

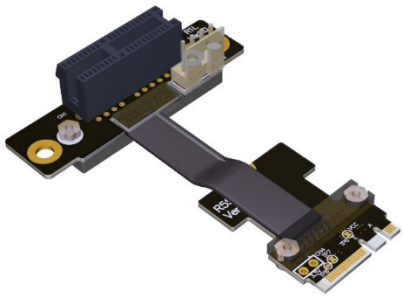
Company	Product	Image and Description
Pasternack*	P/N PE9514 Two pairs matched SMA-SMP adapters	
Tektronix*	Two pairs matched SMA-SMP cables	

Termination Load and Adapter

The following table is a list of termination load and adapters.

Table 11. Partial List of Termination Load and Adapters

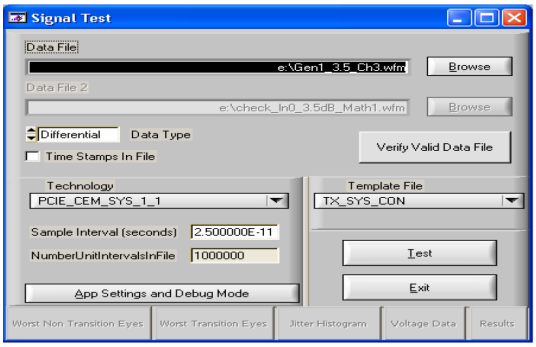
Product	Image and Description
50 Ohm Termination Load*	

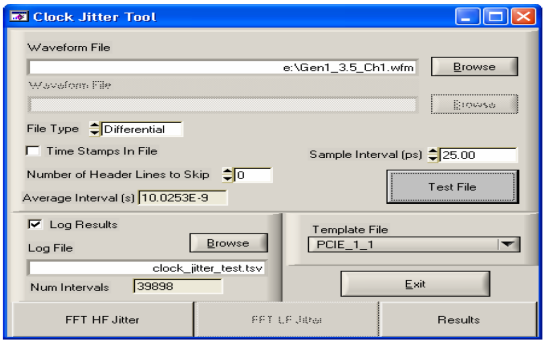
Product	Image and Description
PCIe convert to M.2 Key E adapter	

Software

Use of official compliance test software is recommended, but not required. While manually measuring the signal might be just as effective, it must ultimately pass with the compliance software at the compliance house.

Table 12. Recommended Test Software

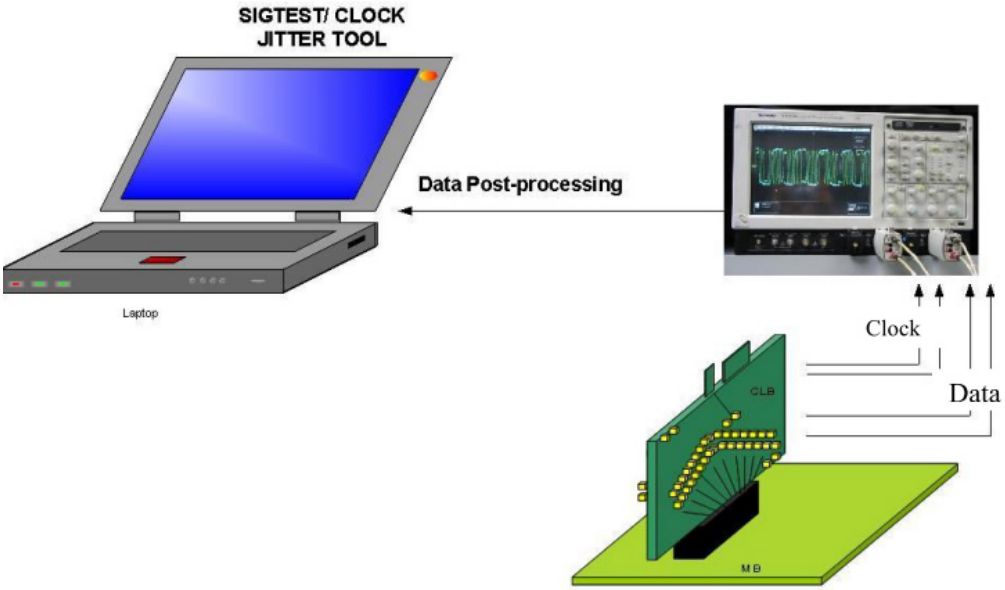
Company	Product	Image and Description
PCI-SIG	SIGTEST 3 2.0	SIGTEST post processing analysis tool (Version 3.2.0 or later) http://pcisig.com/developers/compliance-program 
PCI-SIG	Clock Jitter Tool 1.3.0	Clock Jitter Tool (version 1.3.0 or later): http://pcisig.com/developers/compliance-program

Company	Product	Image and Description
		

Setup Example

The following figure is an example of a testing setup.

Figure 3. Setup Example



Notes:

1. Post processing tools Sigtest and Clock Jitter Tool can also be run on the scope.

Problem with reference. If system shows “in Error! Reference source not found.” Both reference clock and data lane under test must both be sampled simultaneously to carry out measurements as described in the *PCI Express Card Electromechanical Specification Revision 2.0.*

PCIe Compliance Testing

PCI-SIG provides the compliance standards and test descriptions for system boards and add-in cards that comply with *PCI Express Card Electromechanical Specification Revision 2.0*. Customers should refer to the document for an overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

PCI Express specification require devices to have a built-in mechanism for testing the electrical characteristics. Therefore, when the transmit lanes of the device are terminated with a 50-ohm load, the transmit lanes will automatically be forced into compliance mode.

To keep the PCIe controller enabled, the patch (rel-28_TegraX1_TegraX2.diff or rel-32_TegraX1_TegraX2.diff) attached to this application note should be applied.

1. The kernel source code can be downloaded from the L4T archive page (https://developer.nvidia.com/embedded/linux-tegra-archive). Choose the L4T version and download the code from the "Sources."
2. Apply the patch to the kernel source and follow the "Kernel customization" section from the developer guide (link can be found within the L4T archive) to build the kernel.
3. To update the kernel image, place the newly built image to the BSP directory (for example, Linux_for_Tegra/kernel/). To update loadable kernel modules, ensure the correct BSP path was specified (INSTALL_MOD_PATH=<top>/Linux_for_Tegra/rootfs/) when running Step 2.
4. To flash the board, follow the "Quick Start" section from the developer guide. A full flash should be completed to ensure all files gets updated.

To access the attached patch files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the files.

Debugging

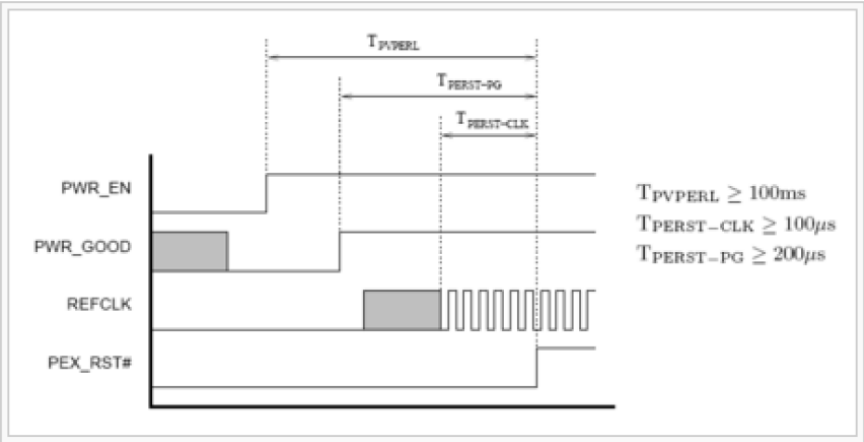
High speed I/O design is difficult to debug and will get harder as speeds increase. The following are a few common PCI Express issues.

If PCI Express Does Not Work

If PCI Express does not respond or no signals are being sent out, verify the following:

- Check the applied power for expected value.
- Check that clocks are on.
- Check for chip reset de-assertion.
- Check the power sequencing.

Figure 4. Power Sequence



Device Fails at ASPM L0 and L1 Enabled

Connect device to a PCIe bus analyzer (for example, LeCroy Protocol Analyzer) to assist with the debug.

1. Configure analyzer to trigger on root repeatedly sending PM_Request_Ack DLLPs.
2. Capture the bus traffic at the time the bus failure occurs.

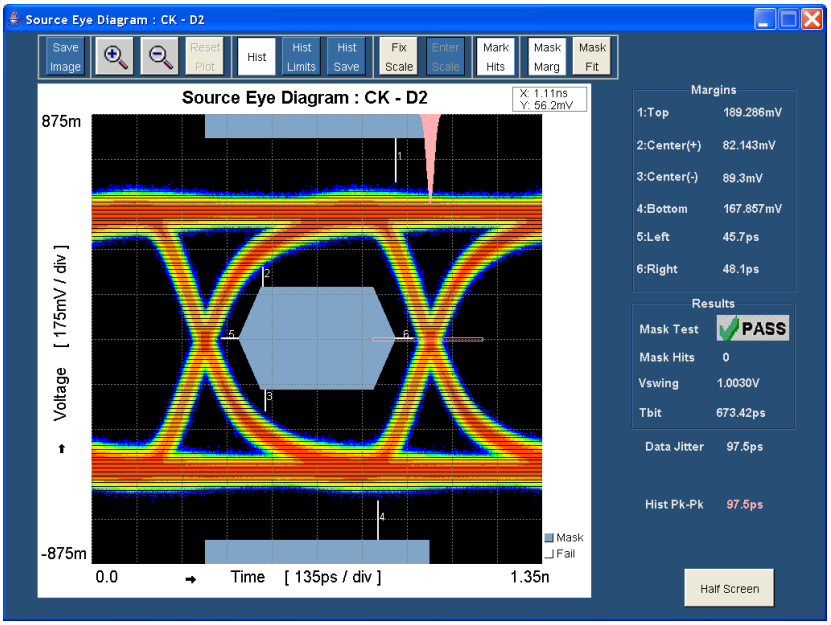
Jetson Nano HDMI Tuning Guide

This chapter describes the registers and steps needed to tune the HDMI™ technology interface for Jetson Nano.

Note: Prior to any tuning, scope and probes must be calibrated. Refer to the documentation for your scope and probe for instructions on how to calibrate.

In order to meet HDMI compliance, tuning is required to adjust the TMDS signal such that the voltage swing is as close to 500 mV ± 100 mV, single-ended, or 1000 mV ± 200 mV differentially. This is to ensure the signal integrity is clean, meets the HDMI specifications, and the device is optimized for low power consumption.

Figure 5. Source Eye Diagram



Abbreviations and Definitions

Table 13 lists the abbreviations that may be used throughout this chapter and their definitions.

Table 13. Abbreviations and Definitions

Abbreviation	Definition
DUT	Device Under Test
EMI	Electromagnetic Interface
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
RF	Radio Frequency
SOR	Serial Output Resource – Module naming referring to the HDMI block
Source	Any type of transmitter such as NVIDIA SoC
TMDS	Transition-Minimized Differential Signaling

Setup

This section describes the setup for HDMI tuning.

Required Equipment

There are many tools currently available to perform the HDMI tuning.

- Test fixture
- Oscilloscope
- Probes
- DC power supply
- Software
  - HDMI compliance software
  - Tool to access register space in NVIDIA SoC

The following subsections partially list acceptable equipment that can be used. The highlighted items indicate which ones this guide will refer to for the rest of this chapter.

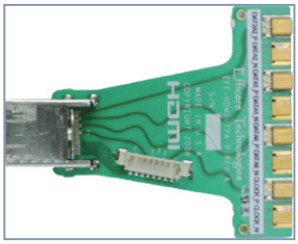
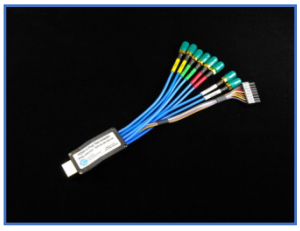
Test Fixtures

Test fixtures are used to connect the probes to the output of the HDMI interface. The following example fixtures listed use the Type-A interface for HDMI 1.4b compliance. Fixtures of different interface types are available and are recommended instead of using adapters to convert the interface type.

For HDMI 2.0 compliance, ensure that the test fixture can support the higher bitrate with minimal insertion loss, as well to meet the differential impedance test.

However, whichever fixture is selected, it must have SMA interconnects to avoid impedance mismatches due to discontinuities.

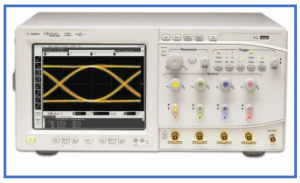
Table 14. Partial List of Acceptable HDMI Test Fixtures Type-A

Brand	Model	HDMI Test Fixtures Type A
Efficere	EFF-HDMI-TPA-P	
Agilent	N1080A	
Wilder Tech	HDMI-TPA-Pro	

Oscilloscope

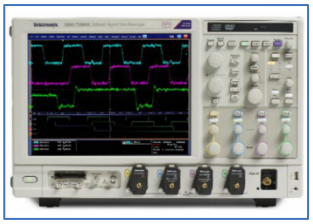
The scope is used to display and measure the signals. The HDMI 1.4 specification requires that the scope have at least 8 GHz of bandwidth and a sampling rate of at least 10 GS/s if the pixel clock is equal to or less than 165 MHz, or sampling rate of at least 20 GS/s if the pixel clock is greater than 165 MHz.

Table 15. Partial List of Acceptable Oscilloscopes for HDMI 1.4 Tuning

Brand	Model	Oscilloscope for HDMI 1.4
Tektronix	TDS6804B or better	
Agilent	DSO80000B or better	

For HDMI 2.0, a scope with at least 16 GHz of bandwidth is recommended.

Table 16. Partial List of Acceptable Oscilloscopes for HDMI 2.0 Tuning

Brand	Model	Oscilloscope for HDMI 2.0
Tektronix	DPO/MSO 7000 or better	
Agilent	Infiniium 9000 series 160 GHz or better	

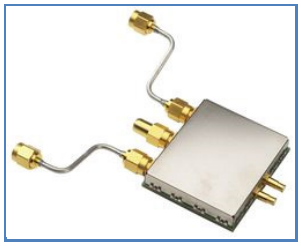
Probes

Probes are used to connect the scope to the test fixture. It must have at least 8 GHz of bandwidth for HDMI 1.4b testing and at least 12 GHz of bandwidth for HDMI 2.0 testing.

At least two (2) probes are required for tuning. However, four (4) probes are ideal.

Untested lanes must be terminated appropriately. See the following subsection, "DC Power Supply" for details.

Table 17. Partial List of Acceptable Probes

Brand	Model	Probe
Tektronix	P7313SMA	
Agilent	1169A - Requires Agilent N5380A Probe Head	
Agilent	N5380A Probe Head. Used with Agilent 1169A	

DC Power Supply

Any power supply that can supply a constant voltage of 3.3V is needed to terminate the HDMI signals. Refer to the probe's instruction manual on how to supply this termination voltage to the probes.

Notes: On Jetson Nano, untested lanes must be terminated to 3.3V using 50Ω terminators.

Whichever tools are used, it is imperative that they are calibrated and meet industry standards to ensure the most accurate measurements are taken.

On Tektronix scopes, the probe and scope can be configured such that the scope can internally apply 3.3V to the probes. This is acceptable for compliance testing.

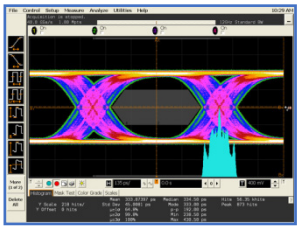
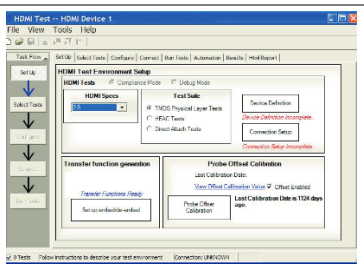
Software

The compliance test software and access register space describe the tools available to perform the HDMI tuning.

Compliance Test Software

It is recommended that the official compliance test software be used to ensure accurate results. While manually measuring the signal may be just as effective, it must ultimately pass with the compliance software at the compliance house.

Table 18. Partial List of Acceptable Test Software

Brand	Model	HDMI 1.4b Testing	HDMI 2.0 Testing
Tektronix	TDSHT3 or later		Not applicable
Tektronix	TekExpress HDM or later	Not applicable	
Agilent	N5399A or later		Not applicable
Agilent	N5399C or later	Not applicable	

Jetson Nano Software Tools

You will need to consult your software team tools that can access the register space in the NVIDIA® Tegra® X1 on Jetson Nano.

Method of Tuning

Tuning will be done by running the eye diagram tests on each of the data lanes while shmoo'ing the applicable registers. The objective is to keep the voltage swing as close to 1000 mV, while providing the eye diagram enough margin to meet specifications.

Drive Strength

Each lane has individual drive strength control. Higher settings increase the overall voltage swing of the non-transition bits. Lower settings decrease the overall voltage swing.

Pre-Emphasis

Each lane has individual pre-emphasis control. Higher settings increase the overall voltage swing of the transition bits while lowering the voltage swing of the non-transition bits.

Procedures

Before anything is done, the scope and probes must be calibrated. Refer to your scope and probe user manuals on how to calibrate.

DUT

This chapter will not be of assistance in detailing how to setup HDMI at the desired resolution. Work with your software team in preparing the DUT for testing.

1. Apply the appropriate EDID module into the test fixture for the desired resolution to be tuned.
2. [Optional] Disable Hot Plug Detect. Use this option if no EDID module is available. The driver or Operating System may disable HDMI if it detects the HDMI panel is being disconnected and a test fixture with no EDID is swapped in. To prevent this use one of the following methods.

   a). Method 1: Disable the HPD interrupt via software by setting the HPD pin to TRISTATE.

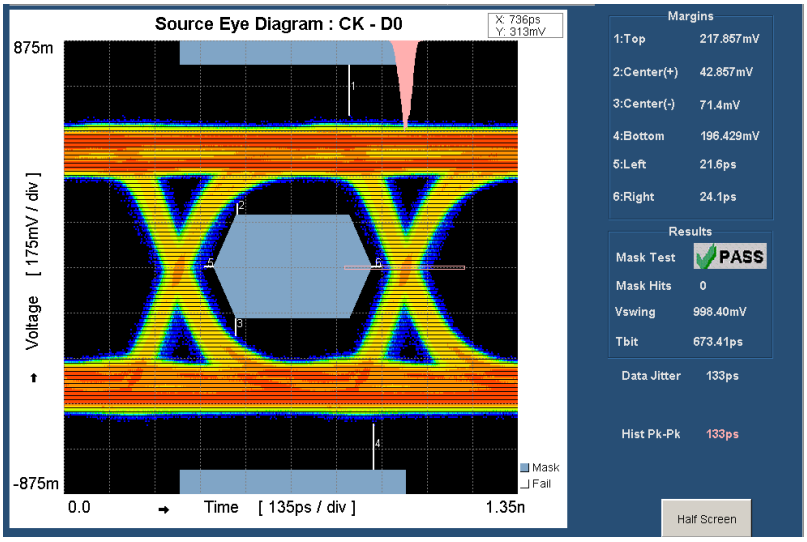
   b). Method 2: Disconnect the HPD circuit from the HDMI connector.

   Refer to the DUT schematics. If this method is chosen, the circuit must be restored before performing the HDMI certification tests.
3. Configure the DUT to drive HDMI at the supported resolutions: 480p (27 MHz), 720p (74.25 MHz), 1080p (148.5 MHz), 2160p/30 (297 MHz), or 2160p/60 (HDMI 2.0).

4. Attach the test fixture to the DUT.
5. Attach the probe-ends to the test fixture, and properly connect the termination voltage to the probes. Untested lanes must be properly terminated.
6. Attach the probes to the scope. After seeing a valid HDMI waveform on the scope, proceed to the following oscilloscope section.

Oscilloscope

1. Ensure the probes are using the termination voltage of 3.3V.
2. Start the HDMI compliance software.
3. Set up the HDMI compliance software to take the eye diagram and configure the probes to the proper clock and data assignments.
4. Run the eye diagram test.
5. Record the voltage swing and margins:



6. If the eye diagram fails, adjust the drive strengths and pre-emphasis settings. Refer to the registers section.
7. Repeat for all data lanes, using different register settings, at all supported resolutions.

> **Tips:** When shmoo'ing drive strengths or pre-emphasis, keep the same value across each data lane. The HDMI pads for each of the data pairs and the clock are the same and should have very minor variation.
>
> Because the clock does not have as many transitions, the settings can be weaker than the data lanes. This can slightly reduce power consumption and lower noise or EMI issues.

Objectives

While there is no margin specification, a good rule of thumb is to provide the following:

- At least 40 mV of margin above and below the eye mask.
- Voltage swing of around 1000 mV, differential.
- Find settings for the following:
  - 480p
  - 720p
  - 1080p
  - 2160p/30
  - 2160p/60 (should be used for all HDMI 2.0 modes)

Tips: The lower the drive strength, I/O peak current, and pre-emphasis settings, the lower the power consumption.

The stronger the termination, more current is needed and therefore consumes higher power.

Fast rising and falling edges will contribute to an increase EMI.

Voltage Swing Target

This chapter targets a differential voltage swing of 1000 mV. This target can be lower to help reduce EMI and RF related issues.

Note: By doing so, you agree to accept all responsibility and waive any rights to hold NVIDIA and their representatives responsible for any issue caused by going against this guide. You agree to test random parts to ensure that HDMI compliance is still being met after new settings have been tuned.

Registers

The registers listed in this section are applicable to Jetson Nano.

Note: HDMI is only supported out of SOR1.

Table 19. HDMI_DP1 (SOR1)

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_PLL1_1 (Address: 0x54580060)			
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_TERM	08:08	Internal Termination Enable: •0x0 = Disable •0x1 = Enable	Enables the internal pull-ups.
TMDS_TERMADJ	12:09	Internal Termination Resistance Control	Must use calibration procedures mentioned in Internal Termination subsection. •0000 -> 31Ω •0001 -> 33Ω •0010 -> 36Ω •0011 -> 38Ω •0100 -> 42Ω •0101 -> 45Ω •0110 -> 50Ω •0111 -> 56Ω •1000 -> 63Ω •1001 -> 71Ω •1010 -> 83Ω •1011 -> 100Ω •1100 -> 126Ω •1101 -> 167Ω •1110 -> 250Ω •1111 -> 500Ω
RESERVED	31:13	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_PLL3_1 (Address: 0x54580068)			
RESERVED	23:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
BG_VREF_LEVEL	27:24	Bandgap Voltage Level	Default is 0x8. 2160/60 is 0xC. Bit 0 is not used.

Register Name	Bit Fields	Description	Notes
RESERVED	31:28	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_1 (Address: 0x54580138)			
LANE0_DP_LANE2	07:00	Drive Strength Controls for Lane 0	DRIVE_CURRENT has priority over IO_PEAK. At higher DRIVE_CURRENT settings, IO_PEAK drivers are used, decreasing IO_PEAK's effectiveness. Only lower 7 bits are used.
LANE1_DP_LANE1	15:08	Drive Strength Controls for Lane 1	
LANE2_DP_LANE0	23:16	Drive Strength Controls for Lane 2	
LANE3_DP_LANE3	31:24	Drive Strength Controls for Lane 3	
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_1 (Address: 0x54580148)			
LANE0_DP_LANE2	07:00	Pre-Emphasis Controls for Lane 0	DRIVE_CURRENT has priority over IO_PEAK. At higher DRIVE_CURRENT settings, IO_PEAK drivers are used, decreasing IO_PEAK's effectiveness. Only lower 7 bits are used.
LANE1_DP_LANE1	15:08	Pre-Emphasis Controls for Lane 1	
LANE2_DP_LANE0	23:16	Pre-Emphasis Controls for Lane 2	
LANE3_DP_LANE3	31:24	Pre-Emphasis Controls for Lane 3	
SOR_NV_PDISP_SOR_DP_PADCTL0_1 (Address: 0x54580170)			
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU_VALUE	15:08	TX pull-up current source drive	Refer to default settings for recommended values.
RESERVED	21:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU	22:22	Transmitter pull-up resistors. •0x0 = Disable •0x1 = Enable	Enables TX_PU_VALUE.
RESERVED	31:23	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

Default Register Settings

These are the default settings that passed HDMI compliance on internal reference design boards at PVT. Refer to Table 20 for register descriptions.

Table 20. Default Register Settings

Pixel Clock Frequency	27 MHz	74.25 MHz	148.5 MHz	297 MHz	HDMI 2.0
SOR_NV_PDISP_SOR_PLL1_1 (Address: 0x54580060)					
TMDS_TERM	0x1	0x1	0x1	0x1	0x1
TMDS_TERMADJ	0x9	0x9	0x9	0x9	0x9
SOR_NV_PDISP_SOR_PLL3_1 (Address: 0x54580068)					
BG_VREF_LEVEL	0x8	0x8	0x8	0xA	0x8
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_1 (Address: 0x54580138)					
LANE0_DP_LANE2	0x33	0x33	0x33	0x33	0x33
LANE1_DP_LANE1	0x3A	0x3A	0x3A	0x3F	0x3F
LANE2_DP_LANE0	0x3A	0x3A	0x3A	0x3F	0x3F
LANE3_DP_LANE3	0x3A	0x3A	0x3A	0x3F	0x3F
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_1 (Address: 0x54580148)					
LANE0_DP_LANE2	0x00	0x00	0x00	0x00	0x00
LANE1_DP_LANE1	0x00	0x00	0x00	0x17	0x00
LANE2_DP_LANE0	0x00	0x00	0x00	0x17	0x00
LANE3_DP_LANE3	0x00	0x00	0x00	0x17	0x00
SOR_NV_PDISP_SOR_DP_PADCTL0_1 (Address: 0x54580170)					
TX_PU	0x1	0x1	0x1	0x1	0x1
TX_PU_VALUE	0x10	0x40	0x66	0x66	0x66

Final Steps

This section describes the final steps for HDMI tuning Jetson Nano.

Sanity Check

After tuning is completed, the settings should be sanity-checked to make sure it has not violated any other parts of the HDMI specifications and that there is a comfortable amount of margin.

The DUT should go through the battery of electrical tests outlined in the HDMI CTS document to ensure that the DUT will pass HDMI certification.

If there are any failures, the settings must be tuned again until there is a passing result.

Note: Higher power consumption is expected if the new settings are stronger than the default settings. It may be due to, but not limited to, longer traces, EMI chokes on the signal paths, or signal integrity issues.

Updating the Software

After the tuned settings have been verified, they need to be updated into the OS or the driver. Work with your software team to incorporate the new tuned settings.

- The 480p settings apply to pixel clock frequencies ⩽ 54 MHz
- The 720p settings apply to pixel clock frequencies between > 54 MHz to ⩽ 111 MHz
- The 1080p settings apply to pixel clock frequencies between > 111 MHz to ⩽ 223 MHz
- The 2160p/30 settings apply to pixel clock frequencies between > 223 MHz to ⩽ 297 MHz
- The 2160p/60 settings apply to all HDMI 2.0 resolutions

Note: Ranges can be adjusted according to design and use-cases. More ranges can also be defined if proper tuning and the software implementation are performed.

Final Check

After the settings have been updated in the driver, verify that the tuned settings are applied for each of the requested modes.

A visual check-out is recommended as well. Connect the DUT to an HDMI panel or monitor capable of the resolutions supported by the DUT and visually verify that there is no corruption at any of the supported bitrates.

Jetson Nano DisplayPort and Embedded DisplayPort Tuning

This chapter describes the registers and steps needed to tune the VESA® DisplayPort™ (DP) and Embedded DisplayPort (eDP) interfaces for Jetson Nano.

Note: Prior to any tuning, scope and probes must be calibrated. Refer to the documentation for your scope and probe for instructions on how to calibrate.

Tuning is needed to make sure the DP interface can meet the specification for each of the different combinations of voltage and frequency outputs, while keeping power consumption as low as possible.

Design choices such as, but not limited to, long routing and layer transitions, can heavily affect the signal integrity, requiring some adjustments to overcome the loss.

Abbreviations

Table 21 lists the abbreviations that may be used throughout this application note and their definitions.

Table 21. Abbreviations and Definitions

Abbreviation	Definition
CTS	Compliance Test Specification
DP	DisplayPort
eDP	Embedded DisplayPort
DUT	Device Under Test
RBR	Reduced Bit Rate (1.62 Gbps)
HBR	High Bit Rate (2.7 Gbps)
HBR2	High Bit Rate 2 (5.4 Gbps)
Link Training	Establishing a link between source and sink before normal operation

Abbreviation	Definition
SSC	Spread Spectrum Clock, will reduce EMI
Sink	Any type of receiver, such as a display or panel
SOR	Serial Output Resource – Module naming referring to the DP and eDP block
Source	Any type of transmitter such as NVIDIA SoC

Setup

This section describes the setup for the DisplayPort and embedded DisplayPort tuning.

Required Equipment

There are many tools currently available to perform the DP tuning. These are the required components:

- DP Plug Test Fixture, corresponding to the plug type
- Oscilloscope and Probes
- Software
  - DisplayPort Compliance Test Software
  - Debug Tools to access registers
  - AUX channel automation (optional)

The following subsections partially list acceptable equipment that can be used. The highlighted items indicate which ones this chapter refers to.

Test Fixture

Test fixtures are used to connect the probes to the SOR output of the DUT. It is recommended that a native fixture be selected and that no adapters are to be use between the DP connector and the DP test fixture, as it will heavily affect the signal integrity.

Following is a list of test fixture vendors:

- WilderTech
- VPrime
- Keysight

Oscilloscope

The oscilloscope and probes are used to measure the signal electrically. The equipment must be able to accurately measure up to 5.4 Gbps (HBR2).

The following are examples of testing solutions:

- Tektronix:
  - https://www.tek.com/displayport-0
  - https://www.tek.com/datasheet/displayport-14-and-type-c-compliance-debug-solution
  - https://www.tek.com/oscilloscope/dpo70000-mso70000
  - https://www.tek.com/oscilloscope/dpo70000sx
  - https://www.tek.com/datasheet/displayport%28tm%29-14-sink-calibration-and-test-software-%28dp-sink-bsx-dp-sink%29
- Keysight:
  - https://www.keysight.com/en/pd-2858984-pn-U7232E/displayport-14-compliance-and-validation-test-software
  - https://literature.cdn.keysight.com/litweb/pdf/5991-1784EN.pdf?id=2295383

Software

The compliance test software should be used to guarantee an accurate result for compliance. Debug tools to access register space are necessary to fine-tune the settings. AUX channel automation can help make testing hands-free. Contact your test equipment dealer for more information.

Method for Tuning

There are several settings that can be tuned in the DP PHY to meet all the specifications in CTS. Following is the list of the major controls to be tuned for characterization. Tuning consists of adjusting the settings below to meet each voltage swing, pre-emphasis, and maximum differential voltage tests for each driver configuration.

Drive Strength

Drive strength controls the amount of drive current of each of the four lanes and can be configured individually, affecting the overall voltage swing. This control has higher priority over pre-emphasis, meaning if the settings are maxed out, there will be no current drivers for the other controls.

To save power, this setting can be reduced until it can pass with enough margin (roughly 20 to 30%).

Pre-Emphasis

Pre-emphasis controls affect the voltage swing of the transition bit. There needs to be distinct levels of pre-emphasis to meet specifications. Increasing pre-emphasis also affects non-transition bits, effectively lowering the voltage swing of the non-transition bits.

To save power, this setting can be reduced until it can pass with enough margin (roughly 20 to 30%).

Post Cursor2

Post Cursor2 is deprecated and should always be set to 0.

Headroom Relief (TX_PU)

Due to the low input voltage for the interface, an additional source is needed for high voltage swing operation. **TX_PU** should be enabled for all drive levels. Note that **TX_PU_VALUE** is generally low for 400 mV and 600 mV swing levels and higher for 800 mV and 1200 mV levels.

Procedures

Before anything is done, the scope and probes must be calibrated. Refer to your scope and probe user manuals on how to calibrate.

DUT

Configure the DUT to output the appropriate output configuration, such as bitrate, swing levels, and test patterns. Then connect the test fixture to the DUT and the test fixture to probes to the scope. Any untested lanes are to be terminated with 50Ω to **GND**.

Oscilloscope

After calibration, initialize the compliance test software and configure it for all the modes supported by the DUT.

Objectives

Settings for drive strength, pre-emphasis, post cursor2, and **TX_PU**, must be found for the following output configurations.

DisplayPort

The tuned settings must work across all bitrates supported by the DUT: RBR, HBR, and HBR2 (optional).

Table 22. DP Tuned Settings

Drive Level	Pre-Emphasis Level	Post Cursor2
400 mV	0.0 dB	0
400 mV	3.5 dB	0
400 mV	6.0 dB	0
400 mV	9.5 dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
600 mV	0.0 dB	0
600 mV	3.5 dB	0
600 mV	6.0dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
800 mV	0.0 dB	0
800 mV	3.5 dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
1200 mV	0.0 dB	0

Embedded DisplayPort

The following settings are required for fast link training. Since there is no specification for the other bit rates or voltage levels, this guide will not cover them.

Table 23. eDP Tuned Settings

Bit Rate	Drive Level	Pre-Emphasis Level	Post Cursor2 Level
RBR	400 mV	0.0 dB	0
HBR	400 mV	0.0 dB	0
HBR2	400 mV	0.0 dB	0

Registers

The Serial Output Resource (SOR) module can be configured to output HDMI or DisplayPort (DP). Tegra X1 has two instances of the SOR module and two sets of **HDMI_DP** pins. SOR0 controls the **HDMI_DP0** pins and SOR1 controls **HDMI_DP1**. To select which SOR to access, simply replace the trailing number with the SOR number. For example; SOR_NV_PDISP_SOR_DP_PADCTL0_0 for the first SOR and SOR_NV_PDISP_SOR_DP_PADCTL0_1 for the second SOR.

Table 24. SOR Registers

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_0 (Address: 0x54540138) **SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_1 (Address: 0x54580138)**			
LANE3_DP_LANE3	31:24	Drive Strength Controls for Lane 3	Only lower 7 bits used. Higher values equal to stronger settings.
LANE2_DP_LANE0	23:16	Drive Strength Controls for Lane 2	
LANE1_DP_LANE1	15:08	Drive Strength Controls for Lane 1	
LANE0_DP_LANE2	07:00	Drive Strength Controls for Lane 0	
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_0 (Address: 0x54540148) **SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_1 (Address: 0x54580148)**			
LANE3_DP_LANE3	31:24	Pre-Emphasis Controls for Lane 3	Only lower 6 bits used. Higher values equal to stronger settings.
LANE2_DP_LANE0	23:16	Pre-Emphasis Controls for Lane 2	
LANE1_DP_LANE1	15:08	Pre-Emphasis Controls for Lane 1	
LANE0_DP_LANE2	07:00	Pre-Emphasis Controls for Lane 0	
SOR_NV_PDISP_SOR_POSTCURSOR0_0 (Address: 0x54540158) **SOR_NV_PDISP_SOR_POSTCURSOR0_1 (Address: 0x54580158)**			
LANE3_DP_LANE3	31:24	Post-Cursor Controls for Lane 3	Only lower 5 bits used. Higher values equal to stronger settings.
LANE2_DP_LANE0	23:16	Post-Cursor Controls for Lane 2	
LANE1_DP_LANE1	15:08	Post-Cursor Controls for Lane 1	
LANE0_DP_LANE2	07:00	Post-Cursor Controls for Lane 0	
SOR_NV_PDISP_SOR_DP_PADCTL0_0 (Address: 0x54540170) **SOR_NV_PDISP_SOR_DP_PADCTL0_1 (Address: 0x54580170)**			
RESERVED	31:23	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

Register Name	Bit Fields	Description	Notes
TX_PU	22:22	Headroom Relief Enable	Enable = 1, Disable = 0
RESERVED	21:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU_VALUE	15:08	Headroom Relief Value	Only bits 14:12 are used.
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

Tegra X1 Register Settings

The following tables show the tuning results achieved on NVIDIA internal reference boards. Tuning results on other platforms may differ.

Table 25. Drive Strength, Pre-Emphasis, and Post Cursor Settings for DP

Levels			Register Settings				
Drive	**Pre-Emphasis**	**Post-Cursor2**	**DRIVE_CURRENT**	**PREEMPHASIS**	**POSTCURSOR**	**TX_PU_VALUE**	**TX_PU**
400mV	0	0	0x13	0x0	0x0	0x2	**0x1**
400mV	1	0	0x19	0x8	0x0	0x3	**0x1**
400mV	2	0	0x1E	0x12	0x0	0x4	**0x1**
400mV	3	0	0x28	0x24	0x0	0x6	**0x1**
600mV	0	0	0x1E	0x1	0x0	0x3	**0x1**
600mV	1	0	0x25	0xE	0x0	0x4	**0x1**
600mV	2	0	0x2D	0x1D	0x0	0x6	**0x1**
800mV	0	0	0x28	0x1	0x0	0x4	**0x1**
800mV	1	0	0x32	0x13	0x0	0x6	**0x1**
1200mV	0	0	0x3C	0x0	0x0	0x6	**0x1**

Table 26. Settings for eDP

Register	RBR	HBR	HBR2
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_0 (Address: 0x54540138)	0x13131313	0x13131313	0x19191919
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_1 (Address: 0x54580138)	0x13131313	0x13131313	0x19191919
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_0 (Address: 0x54540148)	0x00000000	0x00000000	0x09090909
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_1 (Address: 0x54580148)	0x00000000	0x00000000	0x09090909
SOR_NV_PDISP_SOR_POSTCURSOR0_0 (Address: 0x54540158)	0x00000000	0x00000000	0x00000000
SOR_NV_PDISP_SOR_POSTCURSOR0_1 (Address: 0x54580158)	0x00000000	0x00000000	0x00000000
SOR_NV_PDISP_SOR_DP_PADCTL0_0.TX_PU (Address: 0x54540170)	0x0	0x0	0x0
SOR_NV_PDISP_SOR_DP_PADCTL0_0.TX_PU_VALUE (Address: 0x54540170)	0x0	0x0	0x0
SOR_NV_PDISP_SOR_DP_PADCTL0_1.TX_PU (Address: 0x54580170)	0x0	0x0	0x0
SOR_NV_PDISP_SOR_DP_PADCTL0_1.TX_PU_VALUE (Address: 0x54580170)	0x0	0x0	0x0

Final Steps

This section describes the final steps for DP and eDP tuning on the Jetson Nano.

Sanity Check

After tuning is completed, the settings should be sanity-checked to make sure they do not violate any other parts of the DisplayPort specifications and that there is a comfortable amount of margin based on the user's analysis.

The DUT should go through the battery of electrical tests outlined in the DP CTS document to ensure that the DUT will pass DP certification.

If there are any failures, the settings must be tuned again until there is a passing result.

Updating the Software

After the tuned settings have been verified, they need to be updated into the OS or the driver.

Final Check

After the settings have been updated in the driver, verify that the tuned settings are applied for each of the requested modes.

A visual check-out is recommended as well. Connect the DUT to a DP or eDP panel and visually verify that there is no corruption at any of the supported bitrates.

Jetson Nano Ethernet Compliance Test Guide

This chapter serves as the high-level guide to compliance testing of the 1000Base-T interface for Jetson Nano. The Jetson Nano have been tested for specification compliance; therefore, no tuning will be required if customer designs follow the routing guidelines published in our design guides.

Compliance Testing

The *IEEE Standard for Ethernet* defined by IEEE802.3ab provides the compliance criteria and test descriptions for 1000Base-T. Customers should refer to the document for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

Placing Jetson Nano in Compliance Mode

The Jetson Nano integrates a Realtek RTL9119I Gigabit Ethernet controller. Therefore, in order to perform compliance testing on the Jetson Nano, customers will need the Realtek Linux Waveform Tool (LinuxWaveformTool_1.0.8.0.nvzip) attached to this PDF and the latest Realtek Linux Driver from https://www.realtek.com/zh-tw/component/zoo/category/network-interface-controllers-10-100-1000m-gigabit-ethernet-pci-express-software.

PDF Attachment

The Realtek Linux Waveform tool is attached to this application note as "LinuxWaveformTool_1.0.8.0.nvzip."

To access the attached files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the file(s). Files with the. nvzip extension can be extracted using 7-Zip file archive software or may be renamed to .zip and extracted with another archive software.

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