Testbench guide

Note: To use the testbench, please ensure the following:

- 1. Verify that the **entity/module name** in your design matches the one instantiated in the testbench. If not, update the name in the testbench.
- 2. Confirm that the **inputs and outputs** are in the correct order and aligned with your module declaration. If they differ, adjust the order accordingly.

Correct output:

TCL CONSOLE:

```
# }
# run 10000ns
Note: ADDER PASSED: 200 out of 200
Time: 2010 ns Iteration: 0 Process: /tb_a
```

WAVEFORM

Name	Value	L	L	1,800.000 ns		1,820.000 ns		1,840.000 ns		1,860.000 ns		1,880.000 ns		1,900.000 ns
> V act_in	b,e,1	3, f ,1	a,5,1	c,4,0	2,c,0	0,8,1	c,3,0	c,f,0	f,e,1	4,6,1	1,e,O	5,d,0	7,e,1	e,d,0
> V exp_in	b,e,1	3,f,1	a,5,1	c,4,0	2,c,0	0,8,1	c,3,0	c,f,0	f,e,1	4,6,1	1,e,O	5,d,0	7,e,1	e,d,0
> W act_out	a,1	3,1	0,1		e , 0	9,0	f,0	b,1	e,1	b,0	f,0	2,1	6,1	h,1
> W exp_out	a,1	3,1	0,1		e , 0	9,0	f,0	b,1	e,1	b,0	f,0	2,1	6,1	h,1
₩ NUM_TESTS	200							200						

ERROR

TCL CONSOLE

```
# run 10000ns
Note: ADDER FAILED: 200 out of 200
Time: 2010 ns   Iteration: 0   Process: /tb_adder/stimulus   File: C
Note: ACTUAL SUM != EXPECTED SUM : # of fail 200
Time: 2010 ns   Iteration: 0   Process: /tb_adder/stimulus   File: C
Note: ACTUAL Cout != EXPECTED Cout : # of fail 96
```

WAVEFORMS

Name	Value		lt	1,440.000 ns		1,460.000 ns		1,480.000 ns		1,500.000 ns		1,520.000 ns		1,540.000 ns
> ₩ act_in	b,e,1	7	4,e,O	d,3,0	2,3,0	d,7,1	7,3,0	c,e,0	1,5,1	c,c,0	d,4,0	d,1,1	3,8,0	7,e,0 .
> W exp_in	b,e,1	7	4,e,0	d,3,0	2,3,0	d,7,1	7,3,0	c,e,0	1,5,1	c,c,0	d,4,0	d,1,1	3,8,0	7,e,0 .
∨ V act_out	U,1	?,0	۷, ۶	۷, ?	?,0	٧, ?	υ,0	?,1	?,0	V,1	U, U	?,U		₹,₩
> ₩ .sum[3:0]	U	3		,	,	? / U		,	? ?		U	?		? (1
₩.Co	1													
> ₩ exp_out	a,1	c,0	2,1	0,1	5,0	5,1	a,0	a,1	7,0	8,1	1,1	f,0	ъ,0	5,1

HUIIIC	Tuluc	шШш		1,640.000 ns		1,660.000 ns		1,680.000 ns		1,700.000 ns	шшш	1,720.000 ns		1,740.000
> ₩ act_in	b,e,1	e,1,1	4,8,0	6,5,0	5,2,1	f,6,0	d,4,1	2,4,0	c,9,1	3,f,1	d,0,0	5,1,0	5,6,0	2,9,0
> ₩ exp_in	b,e,1	e,1,1	4,8,0	6,5,0	5,2,1	f,6,0	d,4,1	2,4,0	c,9,1	3,f,1	d,0,0	5,1,0	5,6,0	2,9,0
> W act_out	f,1	f,1	0,0	8,0	f,0	c,1	b,1	0,0	3,1	f,1	0,0	2,0	8,0	0,0
> ₩ exp_out	a,1	0,1	c,0	h,0	8,0	5,1	2,1	6,0	6,1	3,1	d,0	6,0	h,(

Additional Note:

If you're still seeing errors after running the simulation, ensure there are no active simulations currently running. In the Project Manager, click on "Simulation" and verify that the top simulation module is set to tb_adder. Also, adjust the simulation runtime to at least 10 times the number of tests you intend to run. If the expected TCL output still doesn't appear, try increasing the simulation runtime further.