Testbench guide

Note: To use the testbench, please ensure the following:

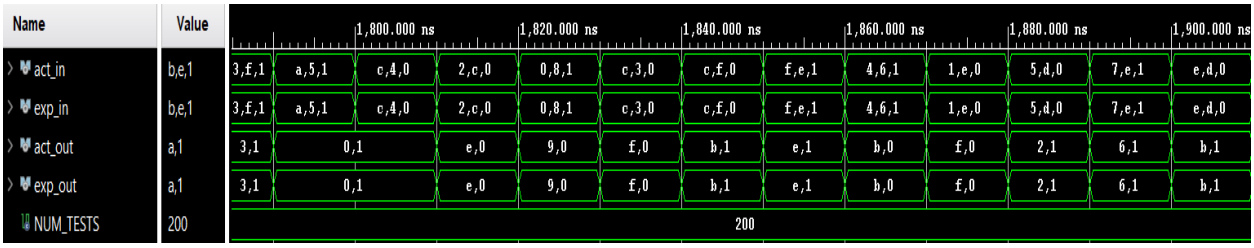
1. Verify that the **entity/module name** in your design matches the one instantiated in the testbench. If not, update the name in the testbench.
2. Confirm that the **inputs and outputs** are in the correct order and aligned with your module declaration. If they differ, adjust the order accordingly.

Correct output:

TCL CONSOLE:

```
# }
# run 10000ns
Note: ADDER PASSED: 200 out of 200
Time: 2010 ns  Iteration: 0  Process: /tb_a
```

WAVEFORM

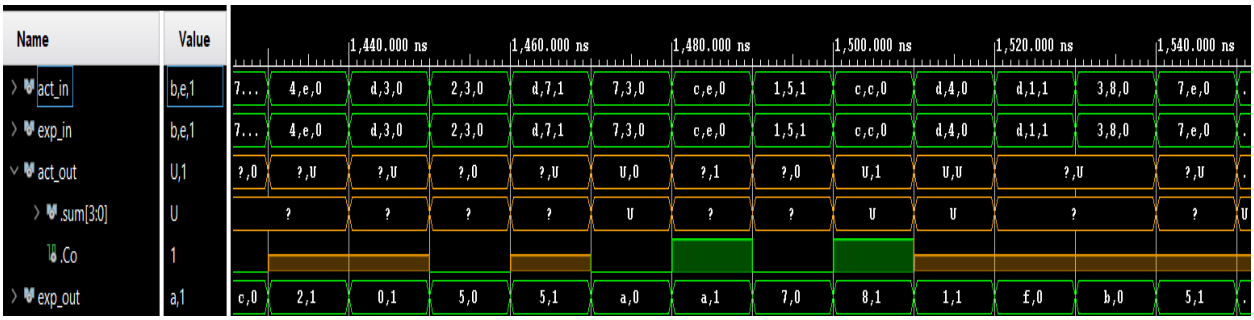


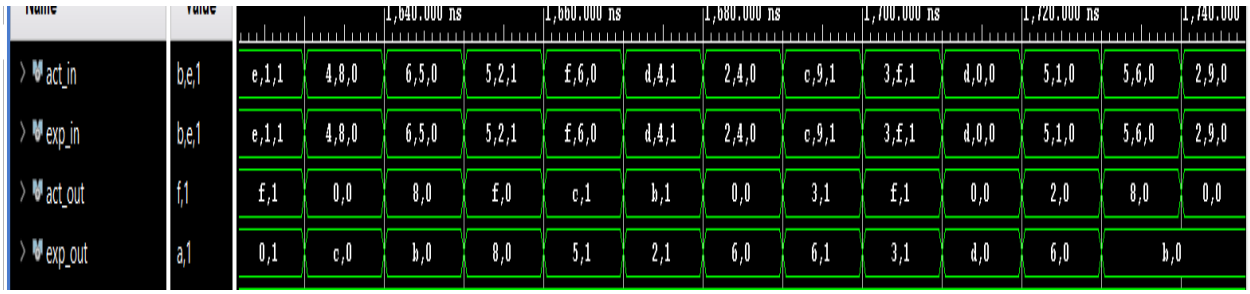
ERROR

TCL CONSOLE

```
# run 10000ns
Note: ADDER FAILED: 200 out of 200
Time: 2010 ns  Iteration: 0  Process: /tb_adder/stimulus  File: C
Note: ACTUAL SUM != EXPECTED SUM : # of fail 200
Time: 2010 ns  Iteration: 0  Process: /tb_adder/stimulus  File: C
Note: ACTUAL Cout != EXPECTED Cout :  # of fail 96
```

WAVEFORMS





Additional Note:

If you're still seeing errors after running the simulation, ensure there are no active simulations currently running. In the Project Manager, click on "Simulation" and verify that the top simulation module is set to `tb_adder`. Also, adjust the simulation runtime to at least 10 times the number of tests you intend to run. If the expected TCL output still doesn't appear, try increasing the simulation runtime further.