HDU refactor

Task: Update the input and output ports of your assigned module to use simple, **non-enum and non-record types (both in VHDL and Verilog)**. This will make the design easier for beginners to understand and trace signal flow.

If you have any questions while working on it, or once you're done, please let me know so I can review your work and give feedback.

Note: You're welcome to use your own naming conventions—just try to keep them descriptive. If you can simplify or shorten the names I've used, it's even better—but no worries if not!

Inputs:

5-bits:	id_rs1, id_rs2
1-bit:	idex_mem_read,
5-bits:	idex_rs1, idex_rs2, idex_rd
1-bit	exmem_reg_write
5-bits:	exmem _rd
1-bit	memwb_reg_write
5-bits:	memwb _rd

Outputs:

2-bits	forwA, forwB
1-bit	stall

Note: If you notice that some records are missing from the inputs and outputs, that's intentional — I've removed them because they are no longer necessary.