Decoder

Task: Convert to verilog or system verilog code.

If you have any questions while working on it, or once you're done, please let me know so I can review your work and give feedback.

Note: You're welcome to use your own naming conventions—just try to keep them descriptive. If you can simplify or shorten the names I've used, it's even better—but no worries if not!

Input:

32-bits: ID

Outputs:

The following output below are the object of ID_content :

        7-bits: op, funct7

        5-bits: rd, rs1, rs2

        3-bits: funct3

        12-bits   imm12

        20-bits   imm20

Note: This decoder is a cleaned-up version of the one I originally used in my pipelined CPU. I'm now using it in my Superscalar CPU project.