IF STAGE (IF_STA.vhd)

**Task:** Update the input and output ports of your assigned module to use **simple, non-enum and non-record types** (both in VHDL and Verilog). This will make the design easier for beginners to understand and trace signal flow.

If you have any questions while working on it, or once you're done, please let me know so I can review your work and give feedback.

**Note:** You're welcome to use your own naming conventions—just try to keep them descriptive. If you can simplify or shorten the names I've used, it's even better—but no worries if not!

Inputs:

| | |
|---|---|
| 1-bit: | clk, reset, is_bubble |
| 32-bits: | br_target |

Outputs:

| | |
|---|---|
| 1-bit: | after_flush |

The following signal below are the object of IF_STAGE

| | |
|---|---|
| 1-bits: | is_valid |
| 32-bits | instruction, pc |

Internal signals:

| | |
|---|---|
| 32-bits: | pc_fetch, pc_current, instr_reg, instr_fetched |

The following signal below are the object of temp_reg (I just broke it down for you)

| | |
|---|---|
| 32-bits: | temp_pc, temp instr |
| 1-bit: | temp_ is_valid |