MEM_WB (MEM_TO_WB.vhd)

Task: Update the input and output ports of your assigned module to use simple, **non-enum and non-record types (both in VHDL and Verilog/System Verilog)**. This will make the design easier for beginners to understand and trace signal flow.

If you have any questions while working on it, or once you're done, please let me know so I can review your work and give feedback.

Note: You're welcome to use your own naming conventions—just try to keep them descriptive. If you can simplify or shorten the names I've used, it's even better—but no worries if not!

INPUTS	# of bits
clk, reset, is_valid _in, reg_write _in, mem_read _in, mem_write _in, Z_in, V_in, N_in, C_in	1
rd _in	5
op _in	7
Instruction _in, program_counter _in, alu_result_in, store_rs2_in, mem_result_in	32

Internal signals(VHDL) or reg (verilog)	# of bits
is_valid _temp, reg_write _ temp, mem_read _ temp, mem_write _ temp	1
rd _ temp	5
op _ temp	7
Instruction _ temp, program_counter _ temp, alu _ temp_in, mem _ result_ temp	32

OUTPUTS	# of bits
is_valid _out, reg_write _ out, mem_read _ out, mem_write _ out	1
rd _ out	5
op _ out	7
Instruction _ out, program_counter _ out, alu _ out, mem _ result_ out	32