

MEM (MEM_STA.vhd)

Task: Update the input and output ports of your assigned module to use simple, **non-enum and non-record types (both in VHDL and Verilog/System Verilog)**. This will make the design easier for beginners to understand and trace signal flow.

If you have any questions while working on it, or once you're done, please let me know so I can review your work and give feedback.

Note: You're welcome to use your own naming conventions—just try to keep them descriptive. If you can simplify or shorten the names I've used, it's even better—but no worries if not!

INPUTS	# of bits
Clk, mem_read_in, mem_write_in,	1
alu_result, store_rs2_out	32

Internal signals(VHDL) or reg (verilog)	# of bits
Mem_address	10 (Note: $2^{10} = 1024$ memory addresses)

OUT PUTS	# of bits
Mem_result	32