

Writeback refactor (WB.STA.vhd)

**Task:** Convert to verilog or system verilog code.

If you have any questions while working on it, or once you're done, please let me know so I can review your work and give feedback.

**Note:** You're welcome to use your own naming conventions—just try to keep them descriptive. If you can simplify or shorten the names I've used, it's even better—but no worries if not!

Inputs:

32-bits:      mem\_data, alu\_data

1-bit:        is\_regWrite, is\_memRead

Outputs:

32-bits:      wb\_data