

Writeback refactor (WB.STA.vhd)

Task: Update the input and output ports of your assigned module to use simple, **non-enum and non-record types (both in VHDL and Verilog)**. This will make the design easier for beginners to understand and trace signal flow.

If you have any questions while working on it, or once you're done, please let me know so I can review your work and give feedback.

Note: You're welcome to use your own naming conventions—just try to keep them descriptive. If you can simplify or shorten the names I've used, it's even better—but no worries if not!

Inputs:

32-bits: memwb_mem_result, memwb_alu_result

1-bit: reg_write, mem_read

Outputs:

32-bits: result

5-bits rd

1-bit: write

- For **VHDL**, remember that all `case` and `if` statements must be placed **inside a process block**.
- Make sure **all relevant input signals are included in the sensitivity list** of each process to avoid simulation mismatches or unintended latching behavior.