ID_EX (ID_TO_EX.vhd)

Task: Update the input and output ports of your assigned module to use simple, **non-enum and non-record types (both in VHDL and Verilog/System Verilog)**. This will make the design easier for beginners to understand and trace signal flow.

If you have any questions while working on it, or once you're done, please let me know so I can review your work and give feedback.

Note: You're welcome to use your own naming conventions—just try to keep them descriptive. If you can simplify or shorten the names I've used, it's even better—but no worries if not!

INPUTS	# of bits
clk, reset, is_bubble, is_valid _in, reg_write _in, mem_read _in, mem_write _in, is_branch _in	1
funct3_in	3
rs1_in, rs2_in, rd _in	5
funct7_in, op _in	7
imm _in	12
immJ _in	20
Instruction _in, program_counter _in, br_target _in, ret_address _in, store_rs2_in	32

Internal signals(VHDL) or reg (verilog)	# of bits
is_valid _temp, reg_write _ temp, mem_read _ temp, mem_write _ temp, is_branch _ temp	1
funct3_temp	3
rs1_ temp, rs2_ temp, rd _ temp	5
funct7_ temp, op _ temp	7
imm _temp	12
immJ _ temp	20
Instruction _ temp, program_counter _ temp, br_target _ temp, ret_address _ temp, store_rs2_ temp	32

OUTPUTS	# of bits
is_valid_out, reg_write _out, mem_read _out, mem_write _out, is_branch _out	1
funct3_out	3
rs1_out, rs2_out, rd _out	5
Funct7_out, op _out	7
imm _out	12
immJ _out	20
Instruction _out, program_counter _out, br_target _out, ret_address _out, store_rs2_out	32