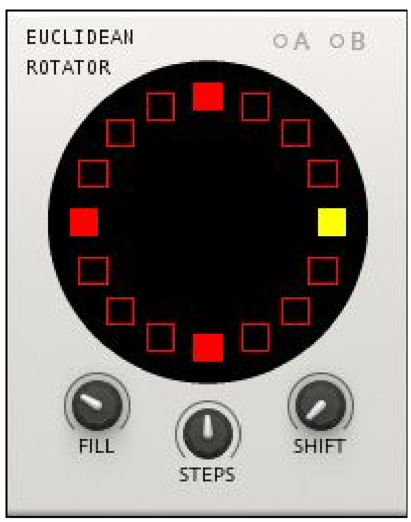
EUCLIDEAN ROTATOR

Reaktor 6 Block



EUCLIDEAN ROTATOR

The Euclidean Rotator block is based on the ‘Euclidean Rhythm’ concept.

It can be used for a variety of tasks including sequencing, clock dividing, modulation and even as an oscillator.

Controls

Steps

The number of steps from 1 to 32. The fill and shift settings are proportional to the number of steps.

Fill

How many steps are filled or active. From zero to the total number of steps.

Shift

Pattern offset from zero to the total number of steps

Inputs

Gate

A positive zero-crossing at the gate input will advance the internal clock by 1 step. If the step is ON (filled) then the incoming gate signal is converted to a boolean / logic value (0 or 1) and sent out of the Gate output.

Reset

A positive zero-crossing at the reset input will sent the internal clock back to the zero position (the first step)

Mod A / B

All modulations run at 15khz so can be used with all types of audio signal.

For example using an oscillator as a modulation source can generate interesting waves via the ‘Val’ output.

The MOD options on View B allow you to latch the modulation using the incoming Gate signal. This is effectively a Sample and Hold for the modulation signals.

Snapshot

This input allows you to recall any stored snapshots for the block.

The input range is from 0 -> 1 and is mapped to the snapshot index depending on the SNAPSHOTS : LOW / HIGH controls on the B View.

For example if you wish to select snapshots via midi notes then you can connect the Note output of a Note In block to the Snapshot input and set the LOW control to 1 and the HIGH to 121. This will give you one snapshot per midi note, starting from C -2.

Outputs

Gate

For active steps this is the logical value of the incoming clock (1 if above zero, 0 otherwise)

Reset

This is 1 when the first step is active and zero otherwise.

Val

The Val output is calculated by treating the current sequence as binary and then scaling that value between 0 and 1.

For example, if the number of steps is 4 the maximum value is 15.

A binary sequence of 1 0 0 0 as an integer value is 8.

This value of 8 is divided by the maximum 15 and the output is 0.5333…

Keeping the **Fill** and **Steps** values constant and changing **Shift** is equivalent to the binary shift left / right operator (<< and >>) and will either double or halve the value depending on the direction.

To extend the 4 bit example :

Shift 0 : 1 0 0 0 -> 0.5333..

Shift 1 : 0 1 0 0 -> 0.2666..

Shift 2 : 0 0 1 0 -> 0.1333..

Shift 3 : 0 0 0 1 -> 0.0666..

Clk Pos

Clock Position Output. Range [0..1]

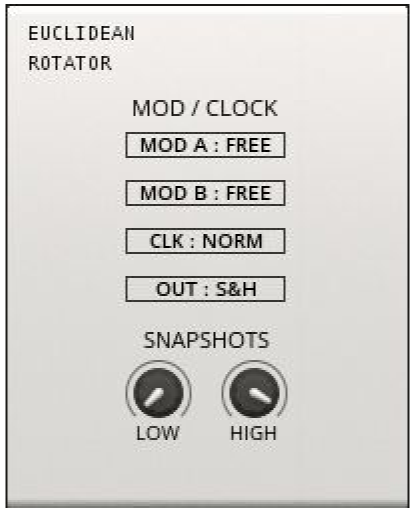
The Clock option in View B determines the output range :

CLK NORM : Normal scaling, 0 -> (Step / Total Steps)

CLK SCALE : 0 -> 1, Step / (Total Steps - 1)

For example with CLK NORM and 4 steps the values will be 0, 0.25, 0.5 and 0.75, whereas with CLK SCALE they will be 0, 0.33, 0.66 and 1.

B View



The MOD, CLK and SNAPSHOTS options are explained above.

OUT : FREE / S&H

The OUT option switches the behaviour of the output gate signal between FREE and S&H (Sample and Hold) modes.

FREE

Any changes to front panel controls or modulation signals are immediately reflected in the output gate signal.

This means that if the current step changes between on and off during the high stage of the input gate signal, the output will follow the state of the current step.

S&H (Sample and Hold)

The output gate value is sampled using the incoming gate rising edge and held until the falling edge. From the falling edge to the next rising edge the output value will remain at zero.

In other words, if a step is empty at the start of the gate signal but becomes active during the gate the output will remain at zero and similarly if a step is active at the start of the gate then the output will remain at 1 for the duration of the high stage of the incoming gate signal.